Multipath Cascaded Single Stage Distributed Power Detector; Analysis and Design

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Abstract – In this paper, a novel technique to improve the input dynamic range and bandwidth of the microwave power detectors (PDs) simultaneously is presented, which utilizes the piecewise linear approximation in conjunction with the distributed structure to achieve the goals. This is an efficient method that requires less number of active devices and therefore saves more power consumption and active chip area, rather than the previous conventional methods. The analysis of circuit based on the transmission line theory is discussed and the transfer function is extracted mathematically for the proposed model. Moreover, a transistor level design is performed using a 0.15μm PHEMT GaAs technology for 24GHz applications. The post layout simulation results are presented.

Keywords: Distributed circuit; Logarithmic amplifier; Microwave; Power detector; Transmission line.

1. Introduction

Many of applications such as wireless communication systems and test & measurement equipment need to detect radio frequency (RF) signals at very weak levels. Signal level can be detected by generating an output proportional to the power of input signal.

On the other hand, the power level of RF signals in many cases varies in the wide range of multi octave in decibel (dB). For that reason, the linear amplifiers are inefficient to detect such signals, because they have a limited dynamic range.

An alternative approach has been used is the logarithmic amplifiers (commonly known as log-amps). The log-amps are divided into the two main categories: The first, those that utilize the inherent exponential characteristic of the semiconductor devices such as p-n junction diodes [1], bipolar transistors [2], [3] and MOSFET transistors in weak inversion region [4-6]. However, they don't have a wide dynamic range usually. Furthermore, the operation of these devices is restricted at higher frequencies, because of the modification of their fundamental characteristic equation by parasitic elements [7]. To extend the total input dynamic range, the second type of log-amps employs more complex configuration with multiple parallel paths. The successive detection logarithmic amplifier (SDLA) is the most famous configuration, which uses this approach to realize the approximated logarithmic function (Fig. 1) [8-13].

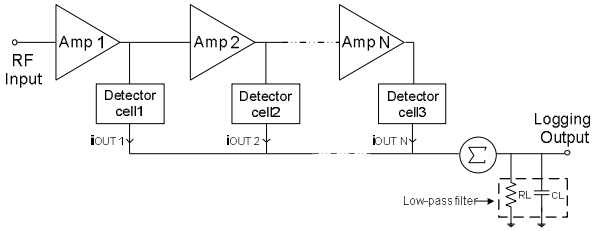

Fig.1. General block diagram of SDLA

The SDLA is conventionally made up of a number of limiting-amplifier stages in a cascaded manner. Each amplifier drives a detector cell (or rectifier cell) to convert its RF input signal to a DC voltage proportional to the amplitude of the RF input. Sum of the detector cells output forms a desired logarithmic transfer function by using the piecewise linear approximation method [14]. The more number of stages in this circuit, results in a wider dynamic

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range. However, this decreases the total bandwidth of circuit as below [15]:

$$F_T = F_S\sqrt{2^{1/N}-1} \quad (1)$$

Where F_T indicates the total bandwidth of the cascaded circuit with N gain stages and F_S is the bandwidth of a single gain stage. Therefore, a very strict trade-off between the total dynamic range and frequency of operation exists in this topology, where improving one proportionally degrades the other.

In this paper, a microwave PD based on the SDLA structure in combination with distributed circuit theory is proposed to overcome this challenge. Section II, describes the principle of PD design based on the distributed circuit concept. The analysis and design of proposed distributed PD is presented in section III. The post layout simulation results are shown in section IV, and finally a conclusion is given in section V.

2. Distributed PD concept and structure

The term 'distributed' has been used quite the opposite of the 'lumped' notion in many of literature. However, for the purposes of this paper, a distributed system is defined to be a system with multiple parallel signal paths and devices, cooperating in harmony to achieve a desired task [16]. On the basis of this definition, the distributed circuit configuration is in contrast to the conventional serial cascaded systems, which have a single signal path. In addition, the physical size of the circuit compared with the signal wavelength has no importance in this view.

As mentioned in the preceding section, the total bandwidth of an analog cascaded circuit block decreases by increasing the number of cascaded stages. This stems from this fact that the more number of stages (or sections), imposes additional poles to the circuit. In distributed systems, however, the core of a given circuit is placed in the multiple parallel paths between the two artificial transmission lines, so that the parasitic capacitances may be absorbed into the line's LC sections. The examples of such circuits has been presented previously are distributed amplifier (DA) [17-20], distributed voltage controlled oscillator (DVCO) [21] and distributed active transformer (DAT) power amplifier [22].

Generalize this idea to logarithmic detector topologies such as SDLA, necessitates exploitation of the two transmission lines (including on-chip passive lumped inductors) that the core of PD circuit is embedded between them and through which the RF input signal can travel without deterioration of the bandwidth. The parasitic capacitances will be merged with the lumped inductors in this condition and the artificial transmission lines are constructed. This technique allows the core of PD is repeated in a cascaded structure to extend the total dynamic range without sacrificing the bandwidth.

Fig. 2 shows the simplified schematic of the proposed PD core, which is suggested based on the described idea. This comprises a single stage DA as an amplifier stage followed by a simple common gate MOS as a detector cell.

The parasitic capacitances in connection with the amplifier stage are absorbed into the two artificial transmission lines, which we called them input line and inter-stage line, respectively. The detector cell parasitic capacitances at its input node are also absorbed into the inter-stage line. Because of the desired signal at the PD output is the DC portion, there is no concern associated with the parasitic capacitances at the output tips of the detector cell.

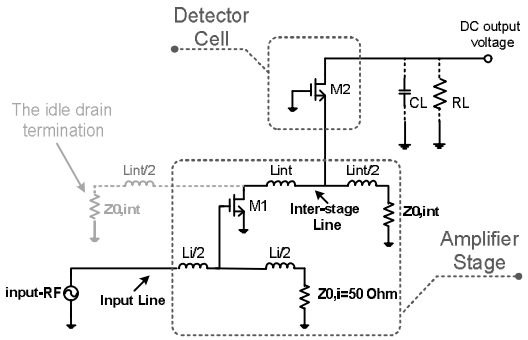

Fig. 2. Simplified schematic of proposed PD core

The power detection investigation by using the above PD core will be described in the next section. Moreover, we will exploit the proposed PD core in a SDLA structure to extend the total dynamic range. Extraction of the logarithmic function for the SDLA will be presented subsequently.

3. Circuit analysis and design

3.1. RF to DC conversion for the proposed PD core

The power detection process is often performed in three steps: V/I (voltage to current) conversion, RF to DC conversion and finally I/V conversion [4], [23-24]. A voltage may be converted to current easily by using a MOS

transistor through its transconductance. Moreover, the RF to DC conversion can be realized by using a single MOS transistor in one of the common-source, common-drain or common-gate forms, like those we have proposed as a detector cell in Fig. 2. We will prove this claim in the continuation.

As seen from Fig. 2, the amplifier stage in the proposed PD core is a single stage DA, comprises an active device (M1) and the two LC ladders at its input and output as a transmission line. The detector cell is a simple common gate transistor M2, which produces a DC voltage proportional to the power of amplified RF signal at the drain of M1. The parasitic capacitances of M1 and M2 in conjunction with the lumped inductors of the input and inter-stage lines make the two artificial transmission lines. Contrary to conventional DA structure, the idle drain line termination (marked with dotted line in this figure) has been eliminated in this configuration. Therefore, the voltage swing across the output drain of M1 is increased, which consequently enhances the amplifier's gain.

In general, the transfer characteristic curve of a linear amplifier may be shown as Fig. 3. As seen, a linear amplifier has the two operation modes. If the input signal amplitude is less than a threshold value of $V_{i,sat}$, then it works in amplifying (or linear) mode and if the amplitude is larger than this value, the amplifier is forced to operate in limiting mode.

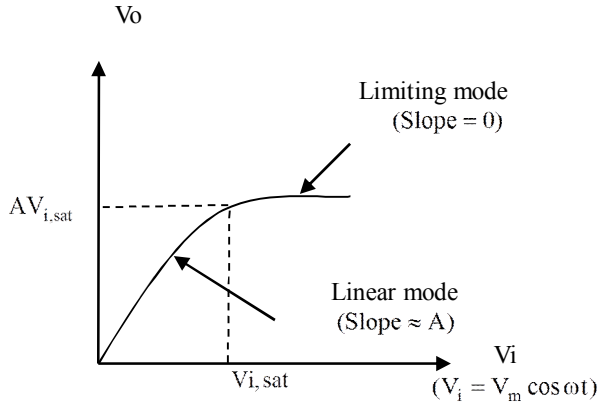

Fig. 3. General characteristic curve of a linear amplifier

By assumption that the single stage DA in Fig. 2 operates in linear mode, its output is a sine wave proportional to the RF input signal. In this condition, the detector transistor M2 meets a sine wave at its input.

The instantaneous current at the output of detector cell, now is given by:

$$i_{OUT} = K(V_{GS_2} + v_{gs_2} - V_t)^2 = K(V_{GS_2} - V_t)^2 + K[v_{gs_2}{}^2 + 2(V_{GS_2} - V_t)v_{gs_2}] \quad (2)$$

where the V_{GS_2} and v_{gs_2} indicate the DC and AC portion of the gate to source voltage of M2, respectively and V_t is the threshold voltage. From above, the instantaneous current of detector cell can be divided into the two individual parts, we name them i_{out1} and i_{out2}. The first part, $i_{out1} = K(V_{GS_2} - V_t)^2$, is a DC portion due to the biasing voltage and just affects the DC offset of the output current. The second part, $i_{out2} = K[v_{gs_2}{}^2 + 2(V_{GS_2} - V_t)v_{gs_2}]$, originates from the RF signal at the input of M2.

By considering the RF input signal of the detector cell transistor M2 as $v_{i,rf}$ and from the simplified schematic of Fig. 2, we have:

$$v_{gs_2} = -v_{i,rf} \quad (3)$$

Substituting (3) into the second part of equation (2), gives:

$$i_{out2} = K[v_{i,rf}{}^2 - 2(V_{GS_2} - V_t)v_{i,rf}] \quad (4)$$

By considering the RF received signal at the gate of M1 equal to $v_{g1} = V_m \cos \omega t$, magnitude of amplified signal at its output is given by:

$$|v_{i,rf}| = |v_{d1}| = |I_{d1}|Z_0 = g_{m1}Z_{0,int}|v_{g1}| = g_{m1}Z_{0,int}V_m \cos \omega t \quad (5)$$

The artificial transmission lines have been supposed lossless in above equation. From (4) and (5), we have:

$$|i_{out2}| = \frac{K}{2}(g_{m1}Z_{0,int}V_m)^2 + \frac{K}{2}(g_{m1}Z_{0,int}V_m)^2 \cos 2\omega t - 2K(V_{GS_2} - V_t)g_{m1}Z_{0,int}V_m \cos \omega t \quad (6)$$

A low-pass RC filter at the output eliminates the AC terms and so a constant DC current remains as:

$$i_{out,dc} = \frac{K}{2}\left(g_{m1}Z_{0,int}\right)^2 V_m{}^2 \qquad (7)$$

This proves a MOS transistor is capable to convert a part of its RF input signal to a DC value, proportional to the RF input power. If the amplifier stage operates in limiting mode, its output is a constant saturated voltage of $AV_{i,sat}$ and therefore there is no RF signal at the input of detector cell (i.e., $v_{i,rf} = 0$). Accordingly, the detector cell adds just a constant DC current to output, independent of an RF input signal amplitude.

3.2.Multipath cascaded single stage distributed power detector

The PD core proposed in previous section was designed based on the distributed circuit theory, especially to operate at microwave frequencies using minimum active devices. Nevertheless, it has a limited dynamic range and has not sufficient sensitivity to detect very week RF signals. Accordingly, a proper enhancement must be done for this structure to increase the dynamic range using the logarithmic topologies.

At first glance, it maybe seems that achieving a logarithmic transfer function is possible by developing the proposed PD core in a parallel summation schematic of Fig. 4(a). Indeed, this structure is the well-known topology of DA that each section drives a detector cell at its output. The main drawback concerned with this structure is the additive gain nature of the DA. Assuming that the transmission lines are lossless, the voltage gain at the last section of the DA drain line can be estimated by [25]:

$$A_V \approx \frac{1}{2} N.g_m.Z_{0,int} \qquad (8)$$

As seen, no logarithmic function can be derived from this equation.

As an alternative, we can use the proposed PD core in a multipath cascaded single stage distributed power detector (CSSDPD) configuration of Fig. 4(b), which is inspired from the SDLA configuration. The complete circuit schematic along with the biasing network has been indicated in this figure.

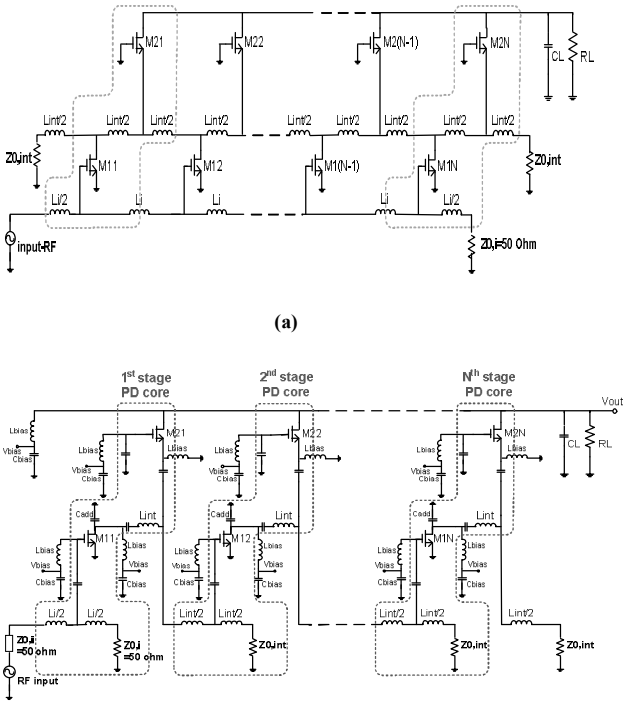

Fig. 4. a) Extension of the proposed PD core with additive gain nature; b) A complete schematic of the multipath CSSDPD with multiplicative gain nature.

Cascade of single stage distributed amplifier stages takes advantage of multiplicative gain feature [26]. This arises from the fact that the RF input signal is multiplied by the gain of each amplifier stage and so emerges multiplicatively at the input of subsequent stages. Summing the detected signal of each core through the multiple parallel paths successively approximates the desired logarithmic transfer function at the output node [14].

There are two artificial transmission lines in this configuration. One of them is the input line of the first stage PD core, we called it 'input line'. Another is called 'inter-stage line', which includes all of the other transmission lines. Only the input line must be terminated to 50Ω. There is no necessity for the inter-stage transmission lines to be matched to 50Ω. This gives the more degree of freedom to design this circuit and allows the inter-stage lines to have a larger characteristic impedance, which means attaining a given gain requirement by using the less number of sections compared with the conventional DA structure. Additionally, this consumes lower power and occupies lower chip area. Unlike the usual structure of DA, the phase velocity equalization is not mandatory in this

circuit, also.

Another problem related with the DA is the lossy nature of transmission lines, which results from the low quality of on-chip inductors. Accordingly, the losses in the long artificial transmission lines may be greater than the amount of signal amplification. This provides extra restrictions on this circuit, from the viewpoint of maximum number of sections. It is in contrary to achieve a large dynamic range. Cascade of single stage DA (in Fig. 4(b)) can solve this problem, also. Because the transmission lines are not continuous in this topology and the line of each section is separated from the others. However, an additional capacitor (C_{add}) is probably required in each inter-stage line of CSSDPD, to equalize the LC sections capacitance.

The bandwidth of proposed CSSDPD is restricted here by minimum cut-off frequency of the two transmission lines. Supposing all sections are similar, the cut-off frequency of two transmission lines and their characteristic impedance can be expressed as:

$$f_{c,i} = \frac{1}{\pi\sqrt{L_i C_{gs_{1j}}}}$$

$$Z_{0,i} = \sqrt{\frac{L_i}{C_{gs_{1j}}}} = 50^{\Omega}$$

$$f_{c,\text{int}} = \frac{1}{\pi\sqrt{L_{\text{int}} C gs_{1j}}} = \frac{1}{\pi\sqrt{L_{\text{int}}\left(C gs_{2k} + C ds_{2k}\right)}} = \frac{1}{\pi\sqrt{2L_{\text{int}} \times \left(C ds_{1_j} + C_{add}\right)}}$$

$$Z_{0,\text{int}} = \sqrt{\frac{L_{\text{int}}}{C_{gs_{1j}}}} = \sqrt{\frac{L_{\text{int}}}{C_{gs_{2k}} + C_{ds_{2k}}}} = \sqrt{\frac{L_{\text{int}}/2}{C_{ds_{1j}} + C_{add}}} \tag{9}$$

A mathematical analysis to derive a logarithmic transfer function for this circuit is provided in next section.

3.3. Transfer function extraction

From the Fig. 4(b), by considering the RF input signal as $v_i = V_m \cos \omega t$ and the voltage gain of amplifier stages in linear mode as $A = g_{m_{11}} Z_{0,\text{int}}$, the voltage at drain tips of amplification transistors are given as:

$$\begin{aligned}
\left|v_{d_{11}}\right| &= \left|I_{d_{11}} Z_{0,\text{int}}\right| = \left|g_{m_{11}} v_{g_{11}} Z_{0,\text{int}}\right| = \frac{1}{2} A.\left|v_i\right| \\
\left|v_{d_{12}}\right| &= \left|I_{d_{12}} Z_{0,\text{int}}\right| = \left|g_{m_{11}} v_{g_{12}} Z_{0,\text{int}}\right| = \frac{1}{2} A^2.\left|v_i\right| \\
&\vdots \qquad\qquad\qquad\qquad \vdots \\
\left|v_{d_{1N}}\right| &= \left|I_{d_{1N}} Z_{0,\text{int}}\right| = \left|g_{m_{11}} v_{g_{1N}} Z_{0,\text{int}}\right| = \frac{1}{2} A^N.\left|v_i\right|
\end{aligned} \tag{10}$$

Where $g_{m_{11}}$ the transconductance of the amplifier is stages and $v_{g_{1N}}$ is the voltage at the gate of Nth amplification transistor. Multiplicative gain can be obviously observed from these equations.

The gate voltage of each amplifier may be expressed as:

$$\begin{aligned}
\left|v_{g_{11}}\right| &= \frac{1}{2}\left|v_i\right| \\
\left|v_{g_{12}}\right| &= \left|v_{d_{11}}\right| = \frac{1}{2} A.\left|v_i\right| \\
&\vdots \qquad\qquad \vdots \\
\left|v_{g_{1N}}\right| &= \left|v_{d_{1(N-1)}}\right| = \frac{1}{2} A^{N-1}.\left|v_i\right|
\end{aligned} \tag{11}$$

On the other hand, the DC converted current at the output of jth path may be rewritten by generalizing the equation (7) as following:

$$\begin{aligned}
&i_{out,dc_j} = \frac{K}{2}\left(g_{m1} Z_{0,\text{int}}\right)^2 \left|v_{g_{1j}}\right|_{\max}^{\ 2} = \\
&\frac{K}{2} A^2 \left|v_{g_{1j}}\right|_{\max}^{\ 2} = \frac{K}{2} A^{2j}\left(\frac{V_m}{2}\right)^2, \qquad j = 1,2,...,N
\end{aligned} \tag{12}$$

In above, $\left|v_{g_{1j}}\right|_{\max}$ is the peak of voltage magnitude at the gate of amplifying transistor in jth section.

For a multipath CSSDPD with N stages, when all amplifier stages are in linear mode, the converted DC current of each path can be written as below:

$$\begin{aligned} i_{out,dc_1} &= \frac{K}{2}A^2\left(\frac{V_m}{2}\right)^2 \\ i_{out,dc_2} &= \frac{K}{2}A^4\left(\frac{V_m}{2}\right)^2 \\ &\vdots \qquad\qquad \vdots \\ i_{out,dc_N} &= \frac{K}{2}A^{2N}\left(\frac{V_m}{2}\right)^2 \end{aligned} \tag{13}$$

In limiting mode also, the amplifier stages output has a saturated value of $AV_{i,sat}$ and the output of paths in this case considered as a constant value of C.

By boosting the RF input signal in the cascaded structure, some of the amplifier stages may be in linear mode and some others in limiting mode. As a result, the converted DC currents summation of N parallel paths at output node may have $(N+1)$ situations:

$$\begin{aligned} &I_{O-S1} = NC && V_{i,sat} \le V_m \\ &I_{O-S2} = i_{out,dc_1} + (N-1)C && \frac{V_{i,sat}}{A} \le V_m < V_{i,sat} \\ &\vdots \qquad\qquad \vdots \\ &I_{O-SJ} = i_{out,dc_1} + \cdots + i_{out,dc_{(J-1)}} + (N-J+1)C && \frac{V_{i,sat}}{A^{J-1}} \le V_m < \frac{V_{i,sat}}{A^{J-2}} \\ &\vdots \qquad\qquad \vdots \\ &I_{O-S(N+1)} = i_{out,dc_1} + \cdots + i_{out,dc_{(N-1)}} + i_{out,dc_N} && \frac{V_{i,sat}}{A^{N}} \le V_m < \frac{V_{i,sat}}{A^{N-1}} \end{aligned} \tag{14}$$

In above, I_{O-SJ} indicates the converted DC output current at Jth situation, when $(J-1)$ stages operate in linear mode and $(N-J+1)$ ones in limiting mode.

From (14), given the RF input voltage is at its lower boundary at Jth situation, i.e. $V_m = \frac{V_{i,sat}}{A^{J-1}} = \frac{AV_{i,sat}}{A^J}$, we have:

$$J = \log_A\left(\frac{A.V_{i,sat}}{V_m}\right) \tag{15}$$

Replacing (13) in (14) for the Jth situation gives us:

$$\begin{aligned} I_{O-SJ} &= \frac{K}{2}A^2\left(\frac{V_m}{2}\right)^2 + \cdots + \frac{K}{2}A^{2(J-1)}\left(\frac{V_m}{2}\right)^2 + (N-J+1)C \\ &= \frac{K}{2}\left(\frac{V_m}{2}\right)^2 \times A^2 \times \frac{A^{2(J-1)}-1}{A^2-1} + (N-J+1)C \end{aligned} \tag{16}$$

The above equation by assumption that the gain of linear mode (A) is sufficiently greater than 1, can be approximated as:

$$I_{O-SJ} \approx \frac{K}{2}\left(\frac{V_m}{2}\right)^2 \times A^{2(J-1)} + (N-J+1)C \tag{17}$$

Substituting (15) in above and using straightforward calculations, the DC output current at Jth situation is given by:

$$\begin{aligned} I_{O-SJ} &\approx C\left[\frac{K.V_{i,sat}^{\,2}}{8C} + N + 1 + \log_A\left(\frac{V_m}{A.V_{i,sat}}\right)\right] \\ &\approx \frac{C}{\log_{10} A} \times \log_{10}\left(\frac{V_m}{\dfrac{V_{i,sat}}{A^{\left(\frac{K.V_{i,sat}^{\,2}}{8C}+N\right)}}}\right) \end{aligned} \tag{18}$$

The derived equation shows a logarithmic relationship between the output current of CSSDPD and the amplitude of RF input signal explicitly. The term $\frac{C}{\log_{10} A}$ is a constant value which indicates the slope of logarithmic function. The term $\frac{V_{i,sat}}{A^{\left(\frac{K.V_{i,sat}^{\,2}}{8C}+N\right)}}$ is reversely proportional to the number of sections (N) and will decrease by increasing N. This determines the beginning point of the logarithmic function, so that when the RF input signal amplitude (V_m) reaches this value, I_{O-SJ} will be zero. Accordingly, the more number of sections cause to decrease the minimum detectable input signal and increases the sensitivity.

4. Simulation results, layout and comparison

Over the microwave frequencies, the atmospheric loss meets a peak near the centre of 24GHz band $(24.05-24.25\text{GHz})$, which mainly occurs due to the absorption by water vapor molecules. Consequently, detecting the RF signals at this band encounters a challenge especially for those applications trying to cover distances of more than a few kilometers. This necessitates the design of power detectors with very high sensitivity for this band.

Here, the simulation results of a logarithmic power detector for 24GHz band based on the twelve stage CSSDPD circuit by using the $0.15\mu\text{m}$ PHEMT GaAs technology is presented.

4.1. Simulation results of PD core

Fig. 5(a) depicts the DC portion of output voltage for the proposed PD core versus the RF input amplitude sweep from -1.6V to $+1.6\text{V}$. The curve shown in this figure, belongs to an even function of equation (7) and confirms that the output characteristic of the proposed PD core is similar to those which can be achieved by a full-wave rectifier. Accordingly, the proposed PD core can do the desired task with just one active device, which is much lower than those are required by a full-wave rectifier in conventional SDLA configuration [8-10].

Fig. 5(b) indicates the transient response of output voltage versus the RF input amplitude variations from 0 to 1.6V. This shows the DC portion of output voltage increases by increasing the RF input amplitude and proves the RF input signal is converted to a DC voltage proportionally by the proposed PD core. The ripples are seen in this figure can be alleviated by applying a larger load capacitor (C_L) in the output RC filter (shown in Fig. 2).

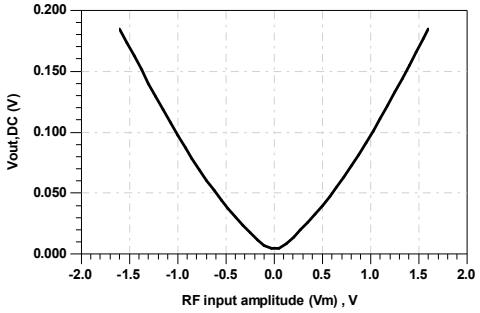

Fig.5(a). The DC component of output voltage as a function of input amplitude

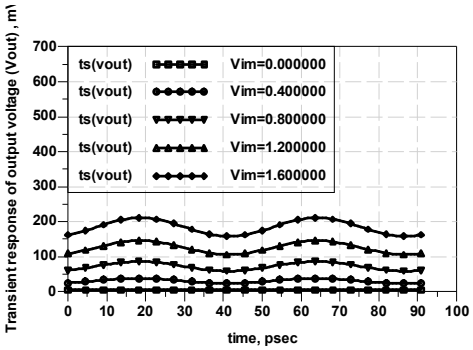

Fig. 5(b). Transient response of the proposed PD core for $\text{C}_\text{L}=105\text{fF}$

4.2. Simulation results for the twelve stage multipath CSSDPD

Fig. 6 depicts the DC output voltage of the twelve stage CSSDPD versus the amplitude of RF input. The logarithmic behavior is obvious in this figure.

Moreover, the transfer characteristic of proposed power detector and its detection error is shown in Fig.7. Indeed, this figure is the same as Fig. 6, except that the horizontal axis is in logarithmic form. As seen, the total dynamic range is 110dBm from -94 to $+16\text{dBm}$ and the maximum detection error over the dynamic range is $\pm 1.5\text{dBm}$. Minimum detectable power is -94dBm, which shows an ultra-high sensitivity.

Fig. 8 shows the total power gain (S_{21}) and the input return loss (S_{11}) in dB. As shown, the power gain is very flat $(108.1\pm 0.1\text{dB})$ over the frequency band. Moreover, S_{11} is less than -20dB over the operating frequency range, which boasts ease of input matching for the cascaded single stage DA topology.

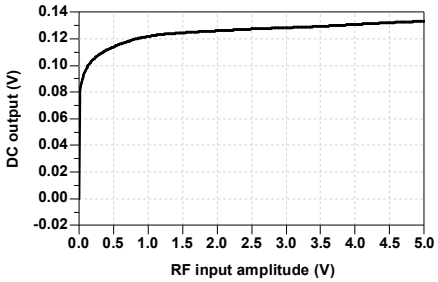

Fig. 6. DC output voltage of CSSDPD versus the RF input amplitude

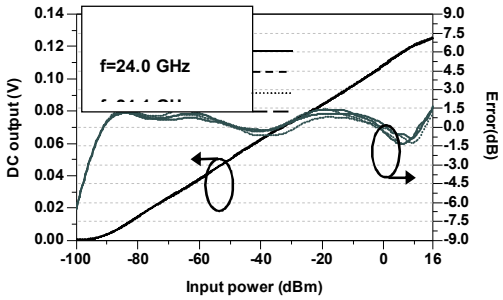

Fig.7. Transfer characteristic of the twelve stage CSSDPD and its error

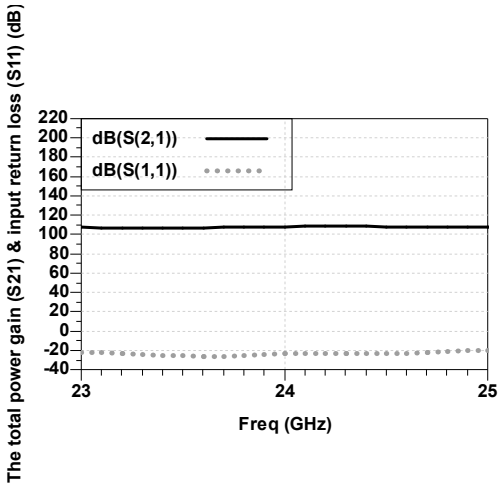

Fig.8. S-parameters of twelve stage CSSDPD

The layout of the designed power detector is shown in Fig.9. The total chip area including twelve stages, supplies nets and pads is $1.5\text{mm} \times 3.6\text{mm}$. This is $1\text{mm} \times 0.32\text{mm}$ for each PD core. The total power consumption is 194mW from $\pm 3\text{V}$ power supplies.

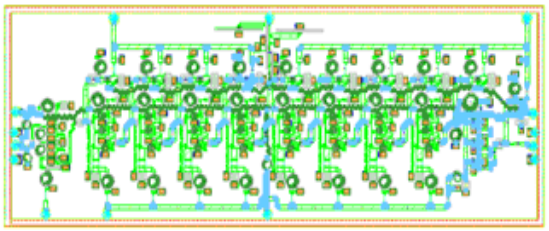

Fig. 9. Layout of the designed multipath CSSDPD

Table 1 summarizes the proposed power detector characteristics and compares this work with others.

Table1. Comparison of logarithmic power detectors

Ref. no.	Freq. (GHz)	Dynamic range (dB)	Logging error (dB)	Power cons. (mW)	Supply voltage (V)	Topology &Technology
[8]	DC to 8	40 60	±1	70 150	2.8	(SDLA) 180nm CMOS **(measured)**
[9]	1	65 74	±2 ±3	24	1.2	(SDLA) 65nm CMOS **(simulated)**
[10]	2 to 18	33	±1	690	-5	(SDLA) InP DHBT **(measured)**
[12]	0.5 to 1.2	60	±2.5	700	NA	(SDLA) GaAs **(measured)**
[13]	0.5 to 1.5	60	±1	400	±5	(SDLA) GaAs HBT **(measured)**
This work	24 to 24.3	95 110	±1 ±1.5	194	±3	(SDLA) 0.15 μm GaAs PHEMT **(simulated)**

5. Conclusion

In this study, the theory of a linear-in-dB microwave power detector with novel structure was analyzed and mathematically discussed. The PD core configuration exploited here is ultra wideband and requires the minimum number of transistors. A significant progress has been made in extending the dynamic range at frequencies of more than $20GHz$, while keeping the power consumption as low as possible. The total dynamic range of $110dBm$ with the minimum detectable power of $-94dBm$ has been achieved. The detection error over the total dynamic range is less than $\pm 1.5dB$. It is also less than $\pm 1dB$ from $-94dBm$ to $+1dBm$. The total power consumption of designed power detector is $194mW$.

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