Design and Analysis of a Two stage Class AB Operational Trans-conductance Amplifier in 180 –nm Technology

Shahrbanoo Ghorbanzadeh[1], Hadi Dehbovid[2*], Alireza Ghorbani[1], Seyed Mehdi AbediPahnekolaei[1]

Abstract–This paper presents design concept of Operational Transconductance Amplifier (OTA). Using active loads in the first stage and improved recycling structure, the effective trans-conductance of the first stage is increased. Nonlinear current mirror boosts the current of the second stage; Therefore, Slew Rate (SR) is increased. The class-AB technique is achieved without enhancing power dissipation and without unity-gain bandwidth (UGBW) or noise deterioration. The efficiency of the proposed OTA is evaluated by several simulations in a 0.18μm CMOS process with the 1.8 V supply voltage. This technique is very helpful for high amplification, stability, and low power applications. From the simulation results, the two stage amplifier gives better performance compared to other topologies, especially in terms of gain, output swing, slew rate and unity-gain bandwidth. The circuit is able to achieve 95 dB gain, a 3V output swing, a 172 $(V/\mu s)$ slew rate and a unity-gain bandwidth of 344 MHZ with a power supply voltage of 1.8 V.

Keywords: Operational Trans-Conductance Amplifier; OTA specifications; post layout simulation; Figures of Merits.

1. Introduction

Operational trans-conductance amplifier (OTA) is an important building block for analog circuits and systems. The OTAs are utilized in various applications such as switched-capacitor circuits, data converters and continuous time filters and low dropout voltage regulators [1-3]. Designing the OTAs may be critical for emerging portable electronic devices. In applications such as very high-resolution delta-sigma modulators and low dropout voltage regulators, the OTA should drive large capacitive loads and meanwhile keep high enough the DC gain, unity- gain bandwidth, and slew rates, while operating under low voltage supply and low static power [4-6]. Achieving these specifications are not viable using class-A OTAs. This is mainly due to the fact that the increasing of slew rate and unity- gain bandwidth would lead to increase power dissipation, considerably. Bulk-driven methods based low power OTAs have been proposed in [7-9]. The main disadvantage existent in this technique is that bulk-source trans-conductance is smaller than the gate-source trans-conductance and may not be enough in some applications.

Class- AB OTAs can be considered as a better solution for the realization of the above specifications.In multi-stage amplifiers, cascading of every gain stage can be useful to enhancement the total DC-gain. But, a medium frequency pole is generated by each stage which can deteriorate the phase margin [10]. A Positive feedback technique can be employed to boost the tail current of the input stage. The circuit can become unstable due to variations of process and environmental parameters [11]. Combined method using the bulk-driven and positive-feedback techniques is proposed in [3]. An OTA with bulk-driven input stage is proposed in which bulk trans-conductance is improved using the positive-feedback. But, some specifications such as input referred noise may not be desirable.

To dominate the deficiency of the class-A OTAs, the class-AB OTA can be helpful [12]. Several techniques for class-AB OTAs have been reported in the literature [12-21]. Class-AB OTAs suggested in [12] have high values for current efficiency (CE) factors. This improvement in CE is obtained by increasing the maximum value of the signal current both in the input and output branches. However,

1 Department of Electrical Engineering, Sari Branch, Islamic Azad university, Sari, Iran. Email:.Sh_ghorbanzadeh@yahoo.com.....

2* CorrespondingAuthor :Department of ElectricaliEngineering, NourBranch, Islamic Azad University, Nour, Iran. Email: hadi.dehbovid@yahoo.com..

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these methods suffer from low open- loop gain. A technique to achieve class AB operation is suggested with the cost of enhancement the power consumption and silicon area of the circuit [13]. Some class-AB techniques have been applied to the recycling folded cascode (RFC) OTA [14-15]. But, the OTAs need additional local common-mode feedback loops at the active load of the differential pair which should be implemented by passive or active matched resistors. In addition, improvements in some specifications, such as DC-gain, are not significant. In another method [16], an adaptive biasing circuit (ABC) for classic fully differential circuits has been introduced using dynamically control the bias current of the amplifier. However, circuit area and power dissipation have been increased due to auxiliary blocks. In [17], a class-AB OTA based on single-stage topology with non-linear current amplifiers has been introduced. But, some target specifications such as DC-gain and SR have not been improved significantly. In [18], a class AB RFC OTA has been suggested using current starving and transition between ohmic and saturation region for dynamic current boosting. Although power consumption is low, DC-gain and SR are not adequate. Some low-current OTAs have been suggested in [19-21]. But, technology or temperature sensitivity in the proposed class-AB OTAs is the main drawback of these techniques.

In this paper, a new two-stage class-AB OTA is proposed. The trans-conductance enhancement of the first stage is achieved via the simultaneous use of the active loads and the RFC technique. Therefore, the DC-gain of the OTA is increased. Enhancement of the SR is obtained using the nonlinear current mirror (NLCM). The rest of the paper is organized as follows. In Section 2, the proposed OTA is introduced. The performance evaluations of the OTA and comparison results are given in Section 3. Finally, Section 4 concludes the paper.

2. Proposed OTA

The conventional two- stage OTA using hybrid-cascade compensation technique is shown in Figure 1 [22]. The Figure 2 demonstrates the circuit configuration of the proposed class-AB OTA. In this Figure, Vo and $Vout$ indicate the output voltages of the first and second stages, respectively.

In Figure 2, a flipped voltage follower (FVF) including the transistors $(M_{1a}, M_{1b}, M_{2a}, M_{2b}, M_{3a}, M_{3b})$ are utilized as an ABC. When a large differential input signal is applied to the OTA, the FVF can deliver more current than the quiescent current. Therefore, it operates in class-AB and this characteristic can be useful for low-power applications [23-24]. The RFC block is also shown in Figure 2. Input signals are applied to the split transistor sets (M_{4a}, M_{4b}) and (M_{4c}, M_{4d}) which have the same aspect ratio. $M_{24a} : M_{24b}$ and $M_{25a} : M_{25b}$ with a ratio of $k:1$ are used as current mirrors. To improve matching, $M_{23a} : M_{23b}$ are employed to maintain the drain potentials of $M_{24a} : M_{24b}$ and $M_{25a} : M_{25b}$ equal [20]. The Source of (M_{4a}, M_{4b}) is connected to the drain of M_{3b} and to the gate of M_{10}. similarly, Source of (M_{4c}, M_{4d}) is connected to the drain of M_{3a} and to the gate of $M9$. Therefore, the class-AB operation can be obtained for the active load transistors M_9 and M_{10} related to the common-gate transistors M_5 and M_6 .

In this circuit, the gate of $M9$ and M_{10} are connected to the input stage using the FVF. Therefore, the trans-conductance of the input is increased from $g_{m1,2}$ to $g_{meff1} = g_{m4a}(1+\mathrm{k}) + g_{m9,10}$ which enhance the DC- gain. Increasing the input stage trans-conductance can also reduce the total input-referred noise voltage as follows:

$$\overline{V_{ni,\mathrm{pro}}^2} = \frac{8kT\gamma}{g^2_{meff1}} \begin{bmatrix} g_{m4b}(1+k^2) \\ +(g_{m25a} + g_{m25b}\,\mathrm{k}^2) + g_{m9} \end{bmatrix} \quad (1)$$

The nonlinear current mirrors (NLCMs) have been used for the output active loads including transistor sets $(M_{11}, M_{13}, M_{15}, M_{17})$ and $(M_{12}, M_{14}, M_{16}, M_{18})$. To active the nonlinear current mirrors (NLCMs), the gates of M_{11} and M_{12} are connected to the first stage outputs V_{o+} and, V_{o-} respectively. The transistors M_{15} and M_{16} are biased near the triode region so that their drain-source voltages are a bit higher than $\mathrm{V_{DS,sat}}$ [12].It should be noted that the transistors M_{16} and M_{18} should be biased in the vicinity of the triode region and saturation region, respectively. As a result, the current through M_{18} is given by

$$I_{18} = \frac{\beta_{18}}{2}\left(\frac{\sqrt{2I_{12}}}{\beta_{14}} + \frac{2I_{12}}{\lambda_{16}\beta_{16}\left(V_{b4} - V_{th}\right)^2} - \frac{1}{\lambda_{16}} \right)^2 \quad (2)$$

Where $\beta_{18} = \mu_n C_{ox}(\mathrm{W/L})_{18}$, λ is the modulation parameter and V_{th} represents the threshold voltage. The current through is given by

$$I_{12} = \frac{\beta_{12}}{2}(V_{GS12} - V_{th})^2 = \frac{\beta_{12}}{2}(V_{DD} - V_{o-} - V_{th})^2 \quad (3)$$

The voltage V_{o-} of this node can be obtained as below:

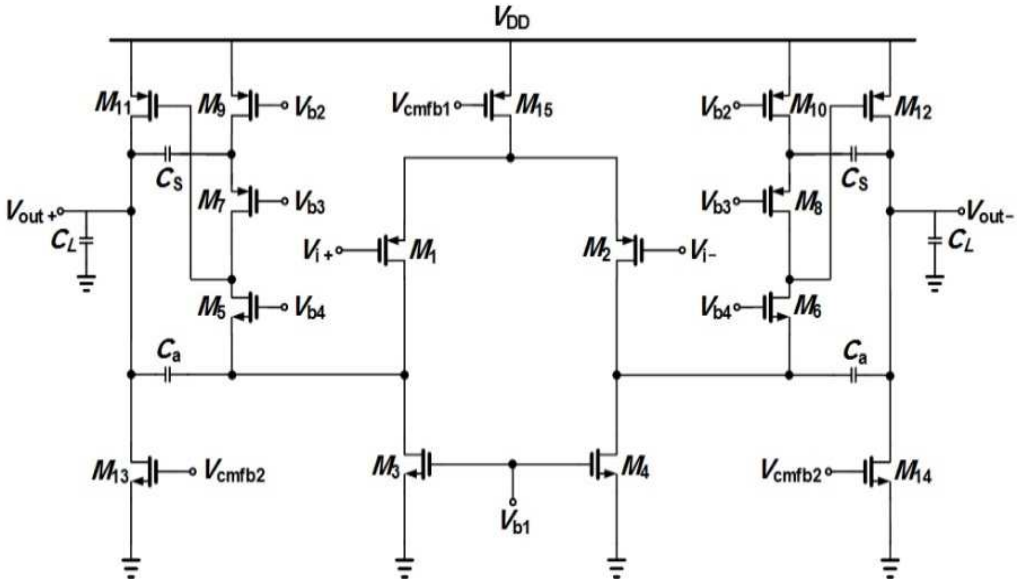


Fig 1. The conventional OTA [22].

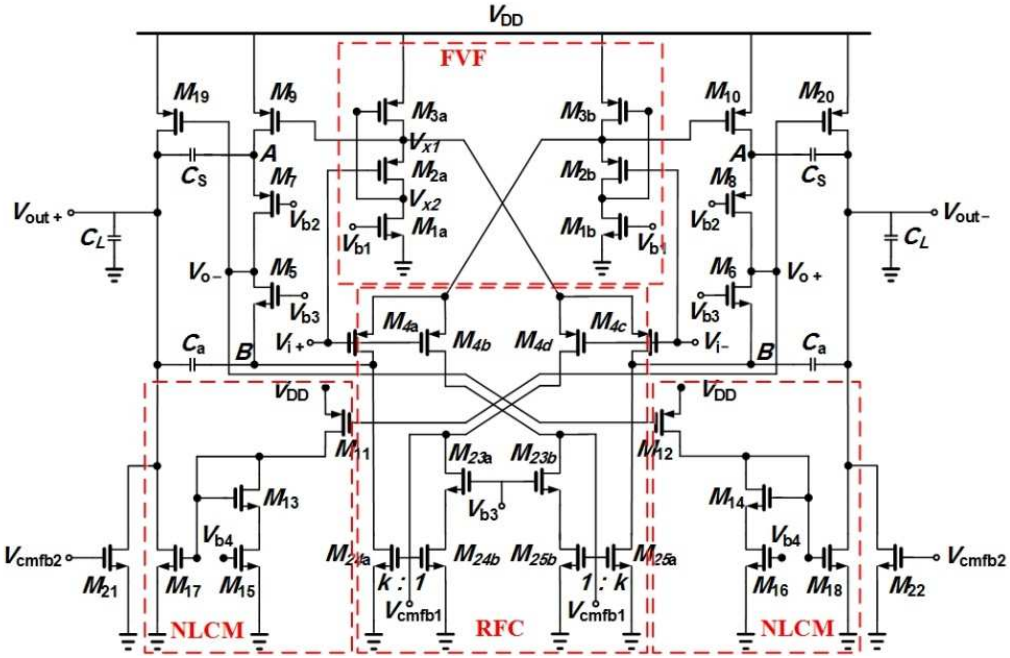


Fig 2. The Proposed OTA.

$$V_{o-} = g_{meff1}\frac{V_{id}}{2}R_{out1} + V_{CMO1} \quad (4)$$

where V_{CMO1} is the first stage common-mode output voltage.Substituting (4) in (3), the drain current of M_{12} is obtained:

$$I_{12} = \frac{\beta_{12}}{2}(V_{DD} - g_{meff}\frac{V_{id}}{2}R_{out1} - V_{CMO1} - V_{th})^2 \quad (5)$$

Finally, using (2), (5) the current through M_{20} is calculated:

$$I_{18} = \frac{\beta_{18}}{2}\left(\frac{\sqrt{2(\frac{\beta_{12}}{2}(V_{DD} - g_{meff}\frac{V_{id}}{2}R_{out1} - V_{CMO1} - V_{th})^2)}}{\beta_{14}} + \frac{2(\frac{\beta_{12}}{2}(V_{DD} - g_{meff}\frac{V_{id}}{2}R_{out1} - V_{CMO1} - V_{th})^2)}{\lambda_{16}\beta_{16}(V_{b4} - V_{th})^2} - \frac{1}{\lambda_{16}}\right)^2 \quad (6)$$

From (6), it is obvious that for a large V_{id} the output current increases proportional to V_{id}^4.That would enhance the SR of the OTA.

3. Simulation Results

To verify the performance of the proposed two-stage class-AB OTA several simulations are performed in a 0.18 µm CMOS process with 1.8V supply voltage using Cadence software. The specifications of the elements and bias voltages of the proposed OTA are reported in Table 1. The frequency responses of the proposed OTA are shown in Fig 3. According to the simulation results, The DC-gain of the OTA is 95 dB. UGBW and phase margin of the proposed OTA is 340 MHz and 64^o , respectively. For the slew ratemeasurement, a square wave whit amplitude 1Vpp at 1 kHz wasapplied to the OTA and the result is given in Fig 4. The average SR of the OTA is 172 (V/µs) .

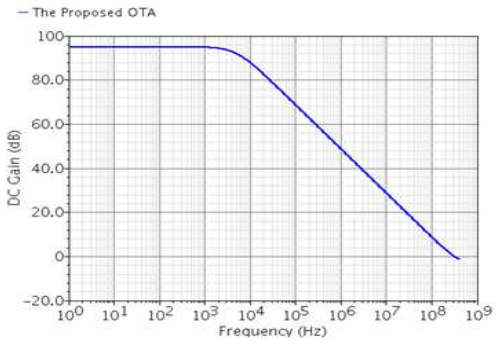
Complete OTA specifications along with a comparison to the conventional OTA are summarized in Table 2. The physical layout of the proposed OTA is shown in Fig 6. The layout area of the proposed OTAis 131µm×142µm.

Monte Carlo (MC) simulations are done by considering both process and mismatch variations. Fig 5 demonstrates the MC histograms of the proposed OTA using 1000-run simulations. The vertical axis represents the histogram count. The horizontal axis in Figa to d represents the DC-gain, input offset, phase margin and UGBW, respectively. The results are also summarized in Table 3. As can be seen from the results, under the process and mismatch variations the OTA specifications are not degraded significantly.post-layout simulation results are compared with some other methods in Table 4. Theproposed OTA shows the small value for layout area compared to the most existingmethods. Moreover, the results indicate that the proposed OTA has the highest DC-gain compared to the other techniques. It has the lowest input-referred noise due to the improved input stage trans-conductance.To compare the other performance parameters, the traditional couple of figures of merits in (7), (8) which for a given load indicate a trade-off between speed performance and total bias current $V_{DS,sat}$ are utilized [6-7].

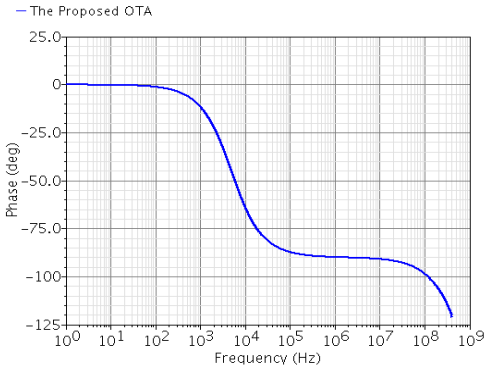
$$FOM_S = \frac{UGBW.C_L}{I_T} \quad (7)$$

$$FOM_L = \frac{SR.C_L}{I_T} \quad (8)$$

As can be seen from Table 4, the proposed OTA has proper values for both of FOMs and FOM_L.



(a)



(b)

Fig 3. Frequency responses for both OTAs: (a) magnitude and (b) phase

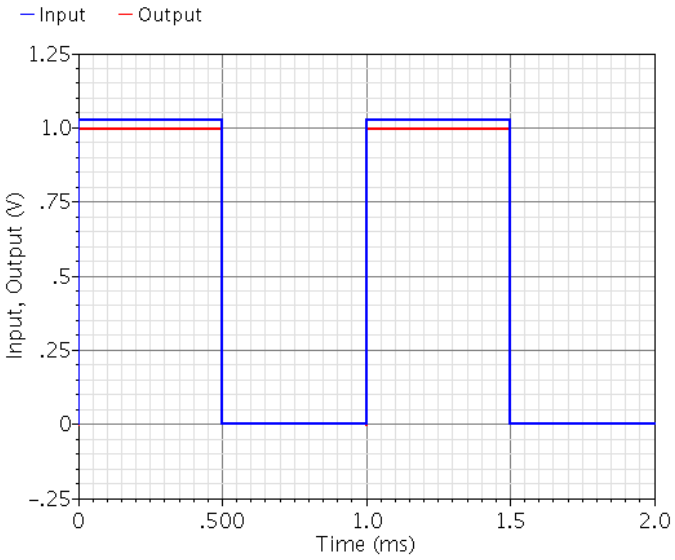


Fig 4. Large signal step responses of the OTA

Table 1. The specifications of the elements and bias voltages of the proposed OTA

Parameter	Value	Parameter	Value
$(W/L)_{1a,1b}$	1×10μm/0.18μm	$(W/L)_{23a,23b}$	×15μm/0.18μm
$(W/L)_{2a,2b}$	1×25μm/0.18μm	$(W/L)_{24a,25a}$	1×45μm/0.18μm
$(W/L)_{3a,3b}$	2×25μm/0.18μm	$(W/L)_{24b,25b}$	×15μm/0.18μm
$(W/L)_{4a,4b,4c,4d}$	1×12.5μm/0.18μm	C_a, C_s	2.1 pF
$(W/L)_{5,6}$	1×15μm/0.18μm	C_L	10 pF
$(W/L)_{7,8}$	1×30μm/0.18μm	V_{b1}	$0.63V$
$(W/L)_{9,10}$	1×30μm/0.18μm	V_{b2}	$0.77V$
$(W/L)_{11,12}$	2×15μm/0.36μm	V_{b3}	$1.15V$
$(W/L)_{13,14,15,16,17,18}$	2×10μm/0.36μm	V_{b4}	$0.77V$
$(W/L)_{19,20}$	2×40μm/0.36μm	V_{CMO1}	$1.15V$
$(W/L)_{21,22}$	2×10μm/0.36μm	V_{CMO2}	$0.9V$

Table 2. Specifications of the proposed OTA and conventional OTAs.

Specification	Conventional OTA			Proposed OTA		
	TT(27° C)	FF(–40° C)	SS(90° C)	TT(27° C)	FF(–40° C)	SS(90° C)
Technology	0.18µm	0.18µm	0.18µm	0.18µm	0.18µm	0.18µm
DC-Gain (dB)	74	69	71	95	88	96
Input-Referred Noise@100kHz ($\mu V/\sqrt{Hz}$)	0.55	0.44	0.95	0.21	0.19	0.30
Differential output Swing (peak to peak) (V)	2.8	2.8	2.8	2.8	2.8	2.8
Phase Margin (°)	62	64	78	64	63	67
Power Dissipation (mW)	2.9	4.3	1.8	3	4.1	2.3
Slew Rate ($V/\mu s$)	42	80	26	172	221	132
UGBW (MHz)	220	368	91	340	450	230
C_L (pF)	10	10	10	10	10	10

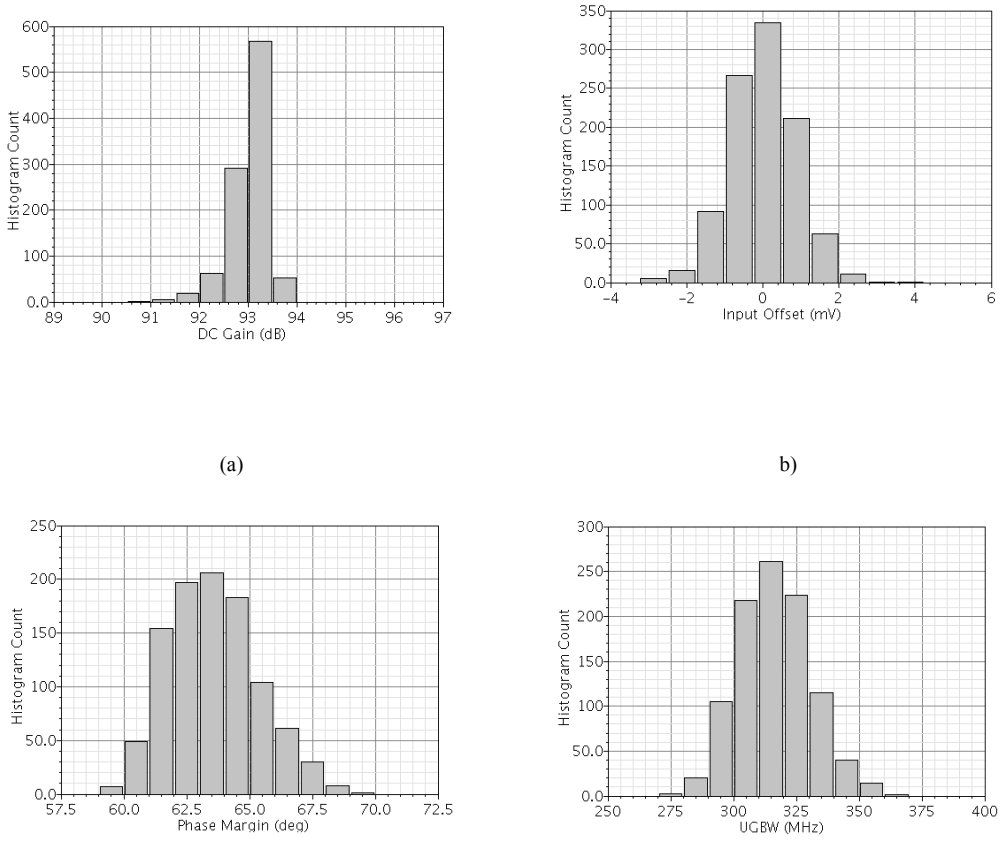


Fig 5. Histogram of MC Simulation. (a) Dc Gain, (b) Input Offset, (c) Phase Margin, (d) UGBW.

Table 3. The MC Analysis of the Proposed OTA.

Specification	Mean Value	Standard Deviation
DC Gain (dB)	93.5	3.9
Input Offset (mV)	0.02	0.8
Phase Margin ($^{\circ}$)	63.6	1.8
UGBW (MHz)	326.5	10.2

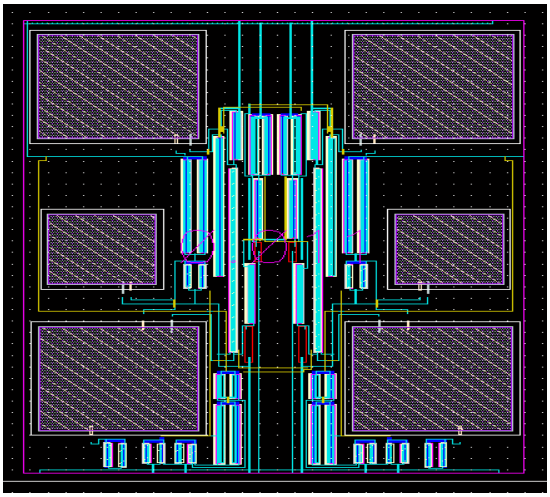


Fig 6. Physical layout of the proposed OTA

Table ٤.Performance Comparison of the Proposed OTA and the Existing Methods

	This[a] work	[12]	[14]	[17]	[23] [a]
Technology	0.18µm	0.5µm	0.5µm	0.18µm	0.18µm
Supply Voltage (V)	1.8	1	1	1.8	1.8
DC-Gain (dB)	93.5	30	76.8	72	93
Input-Referred Noise@100kHz ($\mu v/\sqrt{Hz}$)	0.23	144	0.023	144	0.31
Differential Output Swing (peak to peak) (V)	2.8	--	--	--	2.8
Phase Margin ($^{\circ}$)	64	90	75.1	50	65
Power Dissipation (mW)	3	0.08	0.1	11.9	3
Slew Rate ($V/\mu s$)	172	0.35	25.3	74.1	494
UGBW (MHz)	334	0.2	3.4	86.5	216
Loading Capacitance (pF)	10	80	70	200	1
Operating Mode[a]	SI	SI	SI	SI	SI
$FOM_S=\frac{MHz.pF}{mA}$	2000	200	1190	2613	135
$FOM_L=\frac{V.pF}{\mu s.mA}$	1012	350	8855	2239	309

3. Conclusion

In this paper, a new two-stage class-AB OTA in a 0.18 μm CMOS process with a 1.8 V supply voltage has been presented. The proposed OTA was based on the simultaneous application of class-AB operation in both of the stages. Using active loads and also RFC structure, the first stage trans-conductance has been increased. The NLCM in the output stage has been employed to enhance the SR of the OTA. To evaluate the effectiveness of the proposed method, several simulations have been performed. The results indicated the better performance of the proposed OTA in terms of DC-gain, UGBW, and SR compared to the existing methods.

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