A Topology of Class-AB OTA with Increased DC-Gain and Slew-Rate

Shahrbano Ghorbanzadeh[1], Hadi Dehbovid[*2], Alireza Ghorbani[1], Mehdi Abedi Pahnekola[1]

Abstract – The Operational Trans- conductance Amplifier (OTA)is a main building block in several analog signal and mixed- signal integrated circuits. This paper, a novel low power Class- AB CMOS Operational trans- conductance amplifier (OTA) with High gain and high slew rate is presented. The proposed two-stage OTA, the characteristics of class-AB are applied in both of the stages. The Use of active loads for the first stage provides the effective trans-conductance boosting and increased,DC-gain product. The nonlinear current mirrors boost the current of the second stage leading to the increase of the slew rate. The OTA canbe employed in low- voltage low- power circuits requiring a good performance/power tradeoff.Theoretical analysis and Cadence simulations prove the performance of the new OTA. The simulation results indicate that the DC gain is improved by abot 13db.The UGBW and phase margin of the proposed OTA are 305 MHZ and 65º ,respectively.

Keywords: Operational Trans- conductance Amplifier (OTA), Class- AB circuits, CMOS integrated circuits,Adaptive biasing

1. Introduction

OTA is a very important building block and is often used in many systems, such as sample-and-hold circuits and data converters in electronic circuits. In such applications, OTAs should have high values for DC-gain, slew rate (SR), and unity-gain bandwidth (UGBW) [1-3]. The continuously growing market of mobile and portable electronic devices and the evolution of CMOS technologies have made the OTA a critical design analog block in many systems, in terms of overall power consumption and performance [4–6]. Obtaining these aims may be difficult by the class-A OTAs. In the class-A OTAs, increasing of SR and UGBW are achieved with the cost of increasing the circuit power. In order to overcome the shortcomings of the class-A OTAs, the class-AB OTA can be useful. Several techniques for class-AB OTAs have been reported in the literatures [7-21].

Class-AB OTAs suggested in [7] have high values for current efficiency (CE) factors. This improvement in CE is obtained by increasing the maximum value of the signal current both in the input and output branches. However, these methods suffer from low open loop gain. A technique to achieve class AB operation is suggested with the cost of increasing the power consumption and silicon area of the circuit [8]. Some class-AB techniques have been applied to the recycling folded cascode (RFC) OTA [9-10]. But, the OTAs need additional local common-mode feedback loops at the active load of the differential pair which should be implement by passive or active matched resistors. In another method [11], adaptive biasing circuit (ABC) for classic fully differential circuits have been introduced using dynamically control the bias current of the amplifier. However, circuit area and power dissipation have been increased due to auxiliary blocks. In [12], a class-AB OTA based on single-stage topology with non-linear current amplifiers has been introduced. But, some target specifications such as DC-gain and SR have not been improved significantly. Some low-current OTAs have been suggested in [13-19]. But, technology or temperature sensitivity in the proposed class-AB OTAs are the main drawback of these techniques. The organization of this paper is as follows. In Section 2, the proposed circuit is briefly described. The performance evaluations of the OTA and simulation results are given in Section 3. Finally conclusions are drawn in section 4.

1 Department of Electrical Engineering, Sari Branch, Islamic Azad University, Sari, Iran

2*Corresponding Author : Department of Electrical Engineering , Nour Branch, Islamic Azad University, Nour, Iran. Email: hadi.dehbovid@gmail.com

Received: 2021.05.24 ; Accepted: 2021.12.18

2 . Proposed OTA Structure

In this section, a new family of OTA topologies suitable for low-voltage and low-power operation is proposed. The conventional two-stage OTA using hybrid-cascode compensation technique is shown in Figure 1 [22]. The first and second stages are folded-cascode and common-source amplifiers, respectively. The Figure 2 shows the diagram of the proposed OTA. Two matched transistorsM_1 and M_2 form the differential pair in the first stage is connected with an adaptive biasing circuit. The first one provides a conventional class AB operation. It can set well controlled quiescent currents but when a large differential in put signal is sense it automatically boosts dynamic currents above these quiescent currents.

Often these bias current are chosen small in order to save power consumption however, they deteriorate the small signal performance. the flipped voltage follower (FVF) [23-24] including the transistors (M_{1a}, M_{1b},M_{2a}, M_{2b}, M_{3a}, M_{3b}) is utilized as an adaptive biasing circuit which help increase the SR .In figure 2 , $V_O$and$V_{OUT}$are the output voltages of the first and second stages, respectively.Source of M_1 is connected to the drain of M_{3b} and to the gate ofM_{10}. similarly, Source of M_2 is connected to the drain of M_{3a} and to the gate ofM_9 .Therefore, the input signal appears at the gates of active loads transistors M_9 and M_{10}enhancing the trans-conductance of the OTA.

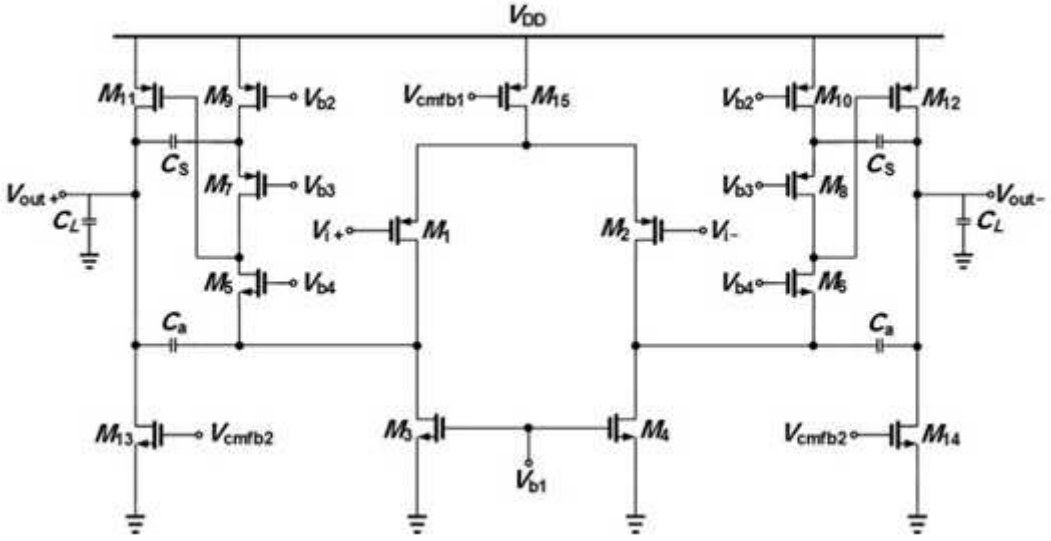

Fig. 1 The conventional OTA [22].

The nonlinear current mirrors have been used for the output active loads including transistor sets $(M_{11}M_{13}M_{15}M_{17})$ and $(M_{12}M_{14}M_{16}M_{18})$. The gates of M_{11} and M_{12} are connected to the first stage outputs V_0+ and V_0−, respectively. The transistors M_{15} and M_{16} are biased near the ohmic region so that their drain-source voltages are a bit higher than$V_{DS\,sat}$.

Consider a condition in which input voltages Vi+ and Vi− increase and decrease, respectively. The voltages of the nodes Vo− and Vo+ are then decreased and increased, respectively. Decreasing the voltage of the node Vo− increases the current of M_{12}.In order to change the drain voltage of M_{12}that is actually the gate voltage of M_{18}. Therefore, the current flowing through M_{18} increases significantly.

2.1 DC Gain

In this architecture, the input signal also appear at the gaete-source of M_9 andM_{10} using the Flipped Voltage Followers (FVF).This increases the effective trans-conductance of the proposed OTA. Figure 3 shows a small-signal model for calculating the voltages of the V_x and V_Y nodes.

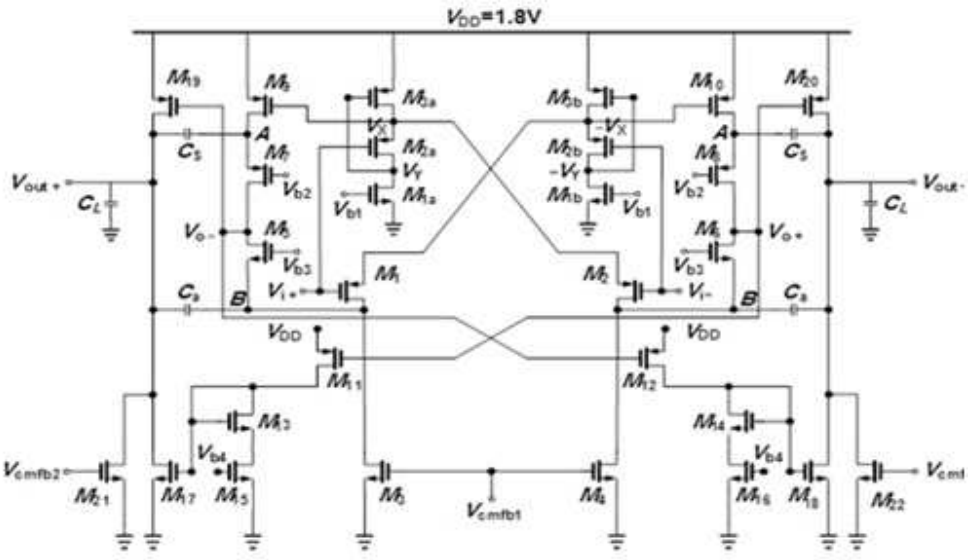

Fig.2 Proposed OTA structure.

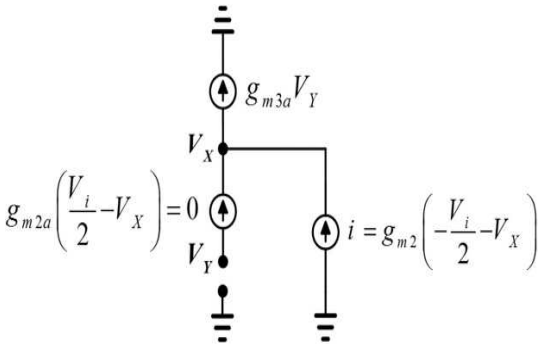

Fig. 3 Small- signal model for calculating the voltages of the V_x and V_Y nodes.

$$V_X = \frac{V_i}{2} \quad (1)$$

$$V_Y = -\frac{g_{m2}}{g_{m3a}} V_i \quad (2)$$

However, in the proposed OTA, trans-conductance of the first stage is

$$g_{meff\,1} = g_{m1,2} + g_{m9,10} \quad (3)$$

The DC-gain of the proposed OTA can be improved compared to the conventional OTA. Neglecting the body effect, DC-gain is found as follows:

$$A_{DC} = A_1 \times A_2 (4)$$

in which A_1 represents the DC-gain of the first stage as shown below:

$$A_1 = g_{meff1} \times R_{out1} \quad (4)$$

Where R_{out1} denotes the output resistance of the first stage.

$$R_{out1} = g_{m7} r_{ds7} r_{ds9} \parallel \left(g_{m5} r_{ds5} (r_{ds1} \parallel r_{ds3})\right) \quad (5)$$

Where

$$A_1 = (g_{m1} + g_{m9}) \times \left[g_{m7} r_{ds7} r_{ds9} \parallel \left(g_{m5} r_{ds5} (r_{ds1} \parallel r_{ds3})\right)\right] \quad (6)$$

where, r_{ds} is the drain–source resistance of the transistors and g_{mi} denotes the small-signal trans-conductance of the corresponding transistors.

In equation (7), A_2 is the DC-gain of the second stage can be calculated as follows:

$$A_2 = g_{meff2} \times R_{out2} \quad (7)$$

where g_{meff2} represents the effective trans-conductance of the second stage and R_{out2} is the output resistance of the second stage as given below

$$R_{out2} = r_{ds15} \parallel r_{ds17} \parallel r_{ds21} \quad (8)$$

Finally, $G_{meff2}$is obtained as follows

$$g_{meff2} = \left(g_{m17} + g_{m11} g_{m15} \left(r_{ds11} \parallel \frac{1}{g_{m15}} \right) \right) \quad (9)$$

Hence, the amplifier's DC gain is given by:

$$A_{DC} = (g_{m1} + g_{m9}) \times \left[g_{m7} r_{ds7} r_{ds9} \parallel \left(g_{m5} r_{ds5} (r_{ds1} \parallel r_{ds3}) \right) \right] \times \left(g_{m19} + g_{m11} g_{m17} \left(r_{ds11} \parallel \frac{1}{g_{m13}} \right) \right) \times (r_{ds17} \parallel r_{ds19} \parallel r_{ds21}) \quad (10)$$

Thus, the unity-gain bandwidth of the proposed amplifier is obtained as:

$$UGBW = \frac{G_{meff1}}{C_c} = \frac{g_{m1} + g_{m9}}{C_c} \quad (11)$$

where Cc represent the Miller compensation capacitor. Note that due to increased trans-conductance, the enhancement of UGBW is also obtained.

2.2 Input-referred noise

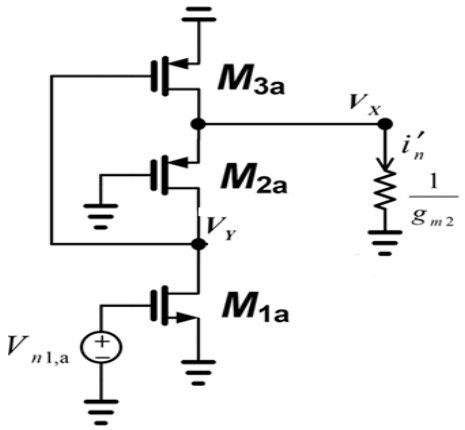

Fig.4 Noise of the proposed 0TA

According to Figure 4, the noise referenced to the input can be calculated in this figure, The noise current $i_n^{'}$is given by

$$v_x = \frac{g_{m1a} \times V_{n1a}}{g_{m2a}} \quad (12)$$

$$i_n^{'} = \frac{v_x}{1/g_{m2}} \quad (13)$$

where

$$i_n^{'} = \frac{\frac{g_{m1a} \times V_{n1a}}{g_{m2a}}}{1/g_{m2}} \quad (14)$$

The output noise voltage per unit bandwidth can be found as follows:

$$\overline{V_{no1a}^2} = i_n'^{\,2} \times R_{out1}^2 \quad (15)$$

$$\overline{V_{no1a}^2} = \left(\frac{g_{m1a} \times g_{m2}}{g_{m2a}} \right)^2 \times \overline{V_{n1a}^2} \times R_{out1}^2 \quad (16)$$

$$\overline{V_{no1a}^2} = A_V^2 \times \overline{V_{ni1a}^2} \quad (17)$$

$$\overline{V_{ni1a}^2} = \frac{\overline{V_{no1a}^2}}{A_V^2} \quad (18)$$

where

$$A_V = g_{meff} \times R_{out1} \quad (19)$$

The input-referred thermal noise of transistorM_{1a}, is explained as f0llows:

$$\overline{V_{niM1a}^2} = \frac{\left(\frac{g_{m1a} \times g_{m2}}{g_{m2a}} \right)^2 \times \overline{V_{n1a}^2} \times R_{out1}^2}{g_{meff}^2 \times R_{out1}^2} \quad (20)$$

The input-referred thermal noise of transistors M_1, $M_3$and, M_9 are given by:

$$\overline{V_{niM1}^2} = \left(\frac{g_{m1}}{g_{meff}} \right)^2 \times \overline{V_{n1}^2} \quad (21)$$

$$\overline{V_{niM3}^2} = \left(\frac{g_{m3}}{g_{meff}} \right)^2 \times \overline{V_{n3}^2} \quad (22)$$

$$\overline{V_{niM9}^2} = \left(\frac{g_{m9}}{g_{meff}} \right)^2 \times \overline{V_{n9}^2} \quad (23)$$

Finally by considering

$$\overline{V_{n1a}^2} = \left(\frac{4KT\gamma}{g_{m1a}}\right), \overline{V_{n1}^2} = \left(\frac{4KT\gamma}{g_{m1}}\right), \overline{V_{n3}^2} = \left(\frac{4KT\gamma}{g_{m3}}\right)$$

$$\overline{V_{n9}^2} = \left(\frac{4KT\gamma}{g_{m9}}\right) \quad (24)$$

in the above equations, the total input-referred thermal noise voltage per unit bandwidth of the OTA can be found as follows:

$$\overline{V_{nIOTA}^2} = \frac{8KT\gamma}{g_{meff}}(g_{m1a} + g_{m1} + g_{m3} + g_{m9}) \quad (25)$$

Therefore, increasing g_{meff}can significantly reduce the total input-referred thermal noise voltage of the proposed OTA.

2.3Output current of FVFCS

The architecture is a source degeneration current mirror topology formerly used for applications like input offset cancellation in amplifiers .

In these applications a degeneration transistor operating only in the ohmic region was used, thus implementing an approximately linear voltage-controlled resistance. However, in this paper we make the degeneration transistor enter saturation region for large input currents. Hence, a strongly nonlinear equivalent resistance is achieved which yields a large output current boosting.

that transistorM_{16} is biased using a constant gate voltage in ohmic region but near the boundary of saturation region, and M_{14} is in saturation region. Given that M_{16} is constant, when the drain current I_{in} of M_{16} increasesM_{16} enters saturation and develops a very large drain-source saturation voltage. This causes a large increase in the gate-source voltage of M_{18} given by $V_{GS18} = V_{DS16} + V_{GS14}$ which leads to a large increase in the output current. The current through M_{18} is

$$I_{18} = \frac{\beta_{18}}{2}\left(\sqrt{\frac{2I_{in}}{\beta_{14}}} + \frac{2I_{in}}{\lambda_{14}\beta_{14}(V_b - V_{th})^2} - \frac{1}{\lambda_{16}}\right)^2 \quad (26)$$

where $\lambda_{16\neq 0}$ and $V_b > V_{th}$

The OTA in Figure. 2 is built using this adaptive load. When V_{in+} decreases $V_{id} < 0$, the Class-AB input stage generates a current through transistor M_2 much larger.

$$I_{20} = \frac{\beta_{18}}{2}\left(\sqrt{\frac{\beta_{12}}{\beta_{14}}}\left[\sqrt{\frac{2I_B}{\beta_{12}} - V_{id}}\right] + \frac{\beta_{12}}{\lambda_{16}\beta_{16}(V_b - V_{th})^2}\left[\sqrt{\frac{2I_B}{\beta_{12}} - V_{id}}\right] - \frac{1}{\lambda_{16}}\right)^2 \quad (27)$$

For a large V_{id} (27) can be simplified to

$$I_{out} \approx \frac{\beta_{18}}{2}\left(\frac{\beta_{12}}{\lambda_{16}\beta_{16}(V_b - V_{th})^2} - V_{id}^2\right)^2 \quad (28)$$

From (28) it is clear that for a large $V_{id}$the output current increases with V_{id}^4, that would enhance the current boosting provided by the Class-AB, quadratically.

2.4 Input Offset

Manufacturing process variations across the chip lead to mismatch in devices, which are otherwise identical by design. A mismatch model [11] based on the study of equal area rectangular devices, states that the variance of a parameter ΔPcan beexpressed as:

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D_X \quad (29)$$

Where A_P is the area proportionality constant for parameter, S_P is the variation of P with spacing, and $D_X$is the distance between two devices along$x$. Since critical devices, such as the input pair or current mirrors, are interdigitated or cross-coupled, $D_X$approaches zero, and the second term of (29) can be neglected. Using (30), the drain-current variance due to process variation can be expressed as:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_T)^2 \quad (30)$$

$$\sigma^2(\mathrm{I_D}) = 4\mathrm{I_D^2}\frac{\sigma^2(\mathrm{V_T})}{(\mathrm{V_{GS}}-\mathrm{V_T})} + \mathrm{I_D^2}\frac{\sigma^2(\beta)}{\beta^2} \quad (31)$$

Assuming $\sigma^2(\mathrm{V_T})$ and $\sigma^2(\beta)$ are uncorrelated. Here represents $\mu_n \mathrm{C_{ox}}\frac{\mathrm{W}}{\mathrm{L}}$.

Equation (31) is very useful, because from a circuit analysis stand point, the drain-current variance can be treated as a small signal that can be referred to the gate of the MOS device through its transconductance, g_m.The result is

$$\sigma^2(V_{GS}) = \sigma^2(V_T) + \frac{I_D^2}{g_m^2}\frac{\sigma^2(\beta)}{\beta^2} \quad (32)$$

and since in analog design $\frac{g_m}{I_D}$ is generally maximized, the effect of the second term of (31) is diminished. Therefore

$$\sigma^2(\mathrm{V_{GS}}) \cong \sigma^2(\mathrm{V_T}) = \frac{\mathrm{A_{VT}^2}}{\mathrm{WL}} \quad (33)$$

Here A_{VT} is the area proportionality constant for the threshold voltage, V_T , which is provided by process characterization.

Using (33), the input offset variance can be expressed as the sum of all device drain-current variances seen at the output, and then referred to the input using the G_m amplifier's . The drain currents of transistors, M_{3b}, M_1 , and M_9, are chosen as $I_1 I$, $\propto_1 \times I$, and $\propto_2 \times I$. It should be noted that α1and α2are positive constants. The input offset variance of the proposed OTA is calculated using the method proposed in [20].

$$\sigma^2(I_{D\,M3}) = \frac{g_{m3}^2 A_{VTN}^2}{W_3 L_3} \quad (34)$$

$$\sigma^2(I_{D\,M1}) = \frac{g_{m1}^2 A_{VTP}^2}{W_1 L_1} \quad (35)$$

$$\sigma^2(I_{D\,M9}) = \frac{g_{m9}^2 A_{VTN}^2}{W_9 L_9} \quad (36)$$

$$\sigma^2(V_{OS}) = \frac{2A_{VTP}^2}{W_1 L_1}\left[1 + \frac{(\alpha_1+\alpha_2)\mu_N}{\alpha_1\mu_p}\left(\frac{L_1}{L_3}\right)^2\frac{A_{VTN}^2}{A_{VTP}^2} + \frac{\alpha_1}{\alpha_2}\left(\frac{L_1}{L_9}\right)^2\right] \quad (37)$$

In the above equations, A_{VTP} and A_{VTN} are the area proportionality constant for threshold voltage of PMOS and NMOS, respectively.

3 Simulation Results

In order to verify the performance of the proposed two-stage class-AB OTA several simulations are performed in a 0.18 μm CMOS process with 1.8V supply voltage using cadence software.

The frequency responses of the proposed OTA are shown in the Figure 5. As can be seen form the results, DC-gain of the OTA is 96 dB.UGBW and phase margin of the proposed OTA are 305 MHz and 65°, Respectively. . For the slew rate calculation, a square wave, 1 Vpp at 5 MHz was applied to the OTA and the result is given in Figure. The OTA specifications in the three processes and temperature corners are summarized in Table 1. As seen from the results, the OTA presents high DC-gain. In addition, the proposed OTA is stable in the three.

The proposed OTA simulation results are compared with the existing methods in Table 2. The results indicat e that the proposed OTA has the highest DC-gain compared to the other techniques. also, it has the lo west input-referred noise due to the improved input stage trans-conductance. To compare the other performance parame ters, the traditional couple of figures of merits in (38), (39) which for a given load indicate a trade-off between speed performance and total bias current (I_T)are utilized [25].

$$FOM_S = \frac{UGBW\,C_L}{I_T} \quad (38)$$

$$FOM_L = \frac{\mathrm{SR}\,C_L}{I_T} \quad (39)$$

As can be seen from Table 2, the proposed OTA has proper values for both of FOMs and FOML.

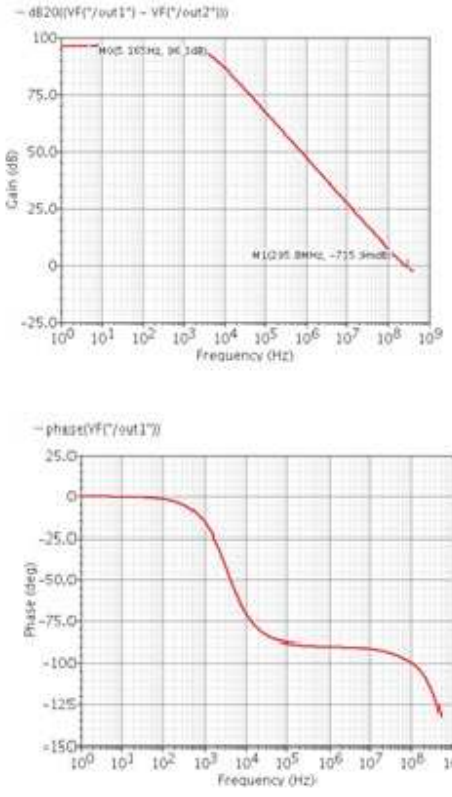

Figure 5. Frequency responses for both OTAs: (a) magnitude and (b) phase**.**

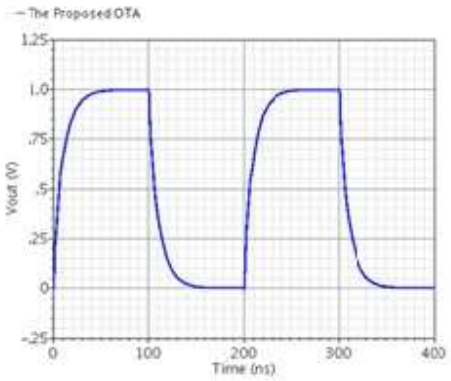

Fig.6 Large signal step response of OTA

4. Conclusion

In this paper a new two-stage class-AB OTA in a 0.18 μm CMOS process with a 1.8 V supply voltage has been presented. The proposed OTA was based on the simultaneous application of class-AB operation in both of the stages. Using active loads, the first stage trans-conductance has been increased. The nonlinear current mirror in the output stage has been employed to enhance the slew rate of the OTA. In order to evaluate the effectiveness of the proposed method, some simulations have been performed. The results indicated the better performance of the proposed OTA in terms of DC-gain, UGBW and SR compared to the existing methods.

Table 1 Specifications of the proposed OTA.

Specification	Proposed OTA		
Technology	TT(27° C) 0.18μm	FF(−40° C) 0.18μm	SS(90° C) 0.18μm
DC-Gain (dB)	96	88	96.5
Input-Referredise@100kHz ($\mu V/\sqrt{Hz}$)	0.21	0.19	0.30
Output Voltage Swing (peak to peak) (V)	3.2	3.2	3.2
Phase Margin (°)	65	62	67
Power Dissipation (mW)	2.9	4	2.1
Slew Rate (V/μs)	172	252	102
UGBW (MHz)	305	440	201
C_L (pF)	10	10	10

Table 2 Performance Comparison of the Proposed OTA and the Existing Methods.

	This work	[7]	[8]	[9]	[12]	[17]
Technology	0.18µ	0.35µ	0.18µ	0.13µm	0.5µ	0.18µ
Supply Voltage (V)	1.8	0.6	1	0.25	1	1.8
DC-Gain (dB)	96	69	64	60	30	72
Input-RefferedNoise@100kHz ($\mu v/\sqrt{Hz}$)	0.21	--	--	--	144	144
Differential Output Swing (peak to peak) (V)	3.2	--	--	--	--	--
Phase Margin (°)	65	65	45	53	90	50
Power Dissipation (mW)	2.9	0.00054	0.13	0.000018	0.08	11.9
Slew Rate (V/µs)	169	0.015	0.7	0.0007	0.35	74.1
UGBW (MHz)	305	0.011	2	0.002	0.2	86.5
Loading Capacitance (pF)	10	15	1	15	80	200
Operating Mode[a]	SI	SUB, BD	SI, BD	SUB, BD	SI	SI
$FOM_S=\frac{MHz.pF}{mA}$	2000	183	15	417	200	2613
$FOM_L=\frac{V.pF}{\mu s.mA}$	1012	250	5	146	350	2239

[a]SUB: subthresold; BD: bulk driven; SI: strong inversion.
[b]Only Schematic level simulation

References

[1] Francesco, C.,Pietro, M.,Gaetano, P.,Pasquale, T.,Alessandro, T.(2018). A Topology of Fully Differential Class-AB Symmetrical OTA With Improved CMRR. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *65*(11), 1504 – 1508.

[2] F, Centurelli., P, Monsurro., G, Parisi., P,Tommasino., A, Trifiletti. (2018). A 0.6 V class-AB rail-to-rail CMOS OTA exploiting threshold lowering. *Electronics Letters*, 54(15), 930-932.

[3] Torralba, A., Carvajal, R.G., Jimenez, M., et al.(2006). Compact low-voltage class-AB analogue buffer. *Electron. Lett*, 42 (3), 152–154.

[4] Peluso, V., Vancorenland, P., Steyaert, M., et al. (1997). 900 mV differential class AB OTA for switched opamp applications, *Electron. Lett*, 33 (17), 1455–1456.

[5] Tomasz, K. ,Fabian, K.(2020). A Compact 0.3-V Class AB Bulk-Driven OTA.. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*. 28 (1) ,224 – 232.

[6] Shirin, P. , Jaime, R. , Alejandro, R. , Manaswini, G. (2019) . Gain and Bandwidth Enhanced Class-AB OTAs.*IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)* , 778- 781.

[7] Luis HC, F., Tales Cleber, P., Robson L, M. (2007). An ultra-low-voltage ultra-low-power CMOS Miller OTA with rail-to-rail input/output swing.*IEEE Transactions on Circuits and Systems II: Express Briefs,*54(10), 843–847.

[8] George, R.,Spyridon, V. (2011). Low-voltage bulk-driven input stage with improved transconductance.*International Journal of Circuit Theory and Applications,* 39 (3) ,327-339.

[9] Luis HC, F., Sameer R, S. (2014). 60-dB gain OTA operating at 0.25-V power supply in 130-nm digital CMOS process.*IEEE Transactions on Circuits and Systems I: Regular Papers,* 61 (6) 1609-1617.

[10] Thandri, B. K.;Silva-Martinez, J.(2003). A robust feedforward compensation scheme for multistage operational trans-conductance amplifiers with no Miller Capacitors, *IEEE Journal of Solid-State Circuits*. 38 (2) 237-243.

[11] L. Callewaert, W. Sansen. (1990). Class AB CMOS

amplifiers with high efficiency. *IEEE Journal of Solid-State Circuits*, 25 (3) 684–691.

[12] JA. Galan, AJ. López-Martín, RG. Carvajal, J. Ramírez-Angulo, C. Rubia-Marcos.(2007). Super class-AB OTAs with adaptive biasing and dynamic output current scaling. *Circuits and Systems I: Regular Papers*, 54(3)449-457.

[13] Lopez-Martin, A., Baswa, S., Ramirez-Angulo, J., Carvajal, R.G. (2005). Low-voltage super class AB CMOS OTA cells with very high slew rate and power efficiency. *IEEE J. Solid-State Circuits*. 40 (5) 1068–1077.

[14] Garde, M.P., Lopez-Martin, A., Carvajal, R.G., Ramirez-Angulo, J. (2018). Super class AB recycling folded cascode OTA. *IEEE Journal of Solid-State Circuits*, 53 (9) 2614 - 2623.

[15] Garde, M.P., Lopez-Martin, A., Ramirez-Angulo, J.(2018). Power-efficient class AB telescopic cascode opamp. *Electron. Lett*, 54, (10) 620-622.

[16] Zuo, L., Islam, S.K. (2013). Low-voltage bulk-driven operational amplifier with improved transconductance, *IEEE Trans. Cir. Syst. I*, 60 (8) 2084-2091.

[17] Stepan Sutula, Michele Dei , LluísTerés, Francisco Serra-Graells, Variable-Mirror Amplifier: A New Family of Process-Independent Class-AB Single-Stage OTAs for Low-Power SC Circuits, IEEE Transactions on Circuits and Systems I: Regular Papers. 63 (2016) 1101-1110.

[18] Saso, J.M. Lopez-Martin, A., Garde, M.P., Ramirez-Angulo, J.(2017). Power-efficient class AB fully differential amplifier. *Electron. Lett*., 53 (19) 1298-1300.

[19] JEONGJIN, R. (2006). High-gain class-AB OTA with low quiescent current, *Journal Analog Integr. Circuits Signal Process*. 47,225–228.

[20] Sutula, S., Dei, M., Teres, L., and Serra-Graells, F.(2016). Variable-mirror amplifier: A new family of process-independent class-AB single-stage OTAs for low-power SC circuits. *IEEE Trans. Cir. Syst. I* , 63 (8) 1101-1110.

[21] Mohamad, Y.Tohid, M. (2014). A single-stage operational amplifier with enhanced transconductance and slew rate for switched-capacitor circuits.*Journal. Analog Integr. Circuits Signal Process*, 79(3) 589–598.

[22] Mohamad, Y.(2005). Hybrid cascode compensation for two-stage CMOS op-amps, *IEICE transactions Electronics*, 88 (22) 1161-1165.

[23] R.G. Carvajal, J. Ramirez-Angulo, A. Torralba, J.A.G. Galan, A. Carlosena, F.M. Chavero.The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design. *IEEE Transactions on Circuits and Systems I: Regular Papers*. 52 (7), 1276 – 1291.

[24] J. Guo, M. Ho, KY. Kwong, KN. Leung. (2015). Power-area-efficient transient-improved capacitor-free FVF-LDO with digital detecting technique. *Electronics Letters*, 51 (1), 94–96.

[25] M. J. M. Pelgrom, A. C. J. Duinmaijer, A. P. G. We lbers. (1989). Matching Properties of MOS Transistors. *IEEE Journal Solid-State Circuits*. 24 (5) ,