

RESEARCH ARTICLE

Performance Investigation of Pentacene Based Organic Double Gate Field Effect Transistor and its Application as an Ultrasensitive Biosensor

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ABSTRACT

In this paper, the electrical performance of double gate organic field effect transistor (DG-OFET) are thoroughly investigated and feasibility of the device as an efficient biosensor is comprehensively assessed. The introduced device provides better gate control over the channel, yielding better charge injection properties from source to channel and providing higher on-state current in comparison with single gate devices. The susceptibility of fundamental electrical parameters with respect to the variation of design parameters is thoroughly calculated. In particular, standard deviation and average value of main electrical parameters signify that metal gate work function, channel thickness and gate oxide thickness are fundamental design measures that may modify the device efficiency. The insensitivity of off-state current to the change of channel length and drain bias confirms feasibility of the device in the nanoscale regime. Next, a nano cavity is embedded in the gate insulator region for accumulation of biomolecules. The immobilization of molecules with different dielectric constants in the gate insulator hollow alters the gate capacitance and results in the drain current deviation with respect to the air- filled cavity condition. It is shown that by the occupancy of the whole volume of the nanogap, a maximum range of on-state current variation can be achieved.

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INTRODUCTION

Recently, a comprehensive study has been conducted regarding the application of organic materials. In particular, organic semiconductors provides the merit and benefits of printing on plastic substrates mainly at low temperature via solution-based processes [1-2], facilitating the fabrication of cost-effective extended- area, flexible devices. It is well established that flexible displays [3], field-effect transistors (FETs) [4-6] solar cells [7-8] and light-emitting diodes [9] are among the popular applications of organic materials. However, these materials suffer from low carrier mobility in comparison with silicon

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based devices [10-13]. By contrast, non-organic materials, mainly silicon, have poor flexibility as well as high temperature fabrication process. Organic Field Effect transistor (OFET) can be considered as one of the critical components of organic integrated circuits with the applications on smart cards, medical implants and sensors. Much the same as traditional metal-oxide semiconductor field effect transistor (MOSFET), OFET contains a conducting channel across the source and drain electrodes, in which the current is modulated by the gate bias. Basically, the arrangement of the gate, source and drain electrodes with respect to the organic material and the gate insulator provides different single gate architectures with different

electrical performance [14]. In bottom-gate top source/drain contact configuration (BG-TC), the gate insulator is formed above the gate contact and the active organic semiconductor can be deposited by vacuum vapor deposition or solution processing techniques. Next, source/drain contacts are formed above the semiconductor. However, in the bottom-gate bottom source/drain contact (BG-BC) architecture, the source and drain electrodes are created below the semiconductor. The BG-BC structure results in higher contact resistance and creates an elevated potential barrier at the source-channel junction. Consequently, low on-state and off-state current are achieved. By contrast, in (BG-TC) design, the bottom gate electrode reduces the contact resistivity and improves the on-state current. High frequency performance of OFET is considered in [15], and an analytical approach is conducted for assessing the threshold voltage of the organic transistor [16].

One of the main challenges of OFET is the low on-state current results from low mobility of carriers. The main target of this paper is designing a novel Double Gate OFET (DG-OFET) structure, aiming towards improving the switching performance of the device and reducing the static power dissipation. The proposed pentacene-based structure takes the advantage of BG-TC and BG-BC structures, providing high on/off current ratio. In this paper, impact of critical design parameters on the electrical performance of the device is comprehensively investigated for optimizing the device performance.

Moreover, statistical analysis is accomplished to calculate the sensitivity of device performance, based on the variation of critical design parameters. In the first step, all the nominal design parameters are set to consider constant and following that, one specific parameter is varied. Next, statistical measures, including standard deviation and mean value of each electrical parameter are calculated to elucidate the susceptibility of device performance. By definition, standard deviation is a measurable factor that measures the dispersion of a specific dataset relative to its mean value. If the calculated dataset is scattered further from the average value, a higher standard deviation can be achieved. In addition, the feasibility of DG-OFET is assessed as an Ultrasensitive is elucidated. Recently, the operation of field effect transistors as label-free biosensors have gained attention, which can electrically detect different biomolecules with

high sensitivity. In this paper, a cavity is created in the gate insulator region, which accumulates the biomolecules. Generally, each biomolecule has different permittivity that modifies the gate capacitance (C_g) and drain current. The paper is arranged as follows: the simulation setup and device structure are introduced in section two. Next, the electrical performance of the double gate organic MOSFET is thoroughly surveyed and impact of design parameter variation on device efficiency is elucidated. Following that, feasibility of the proposed device as an efficient biosensor for detecting biomolecules is clarified. Finally, the paper is outlined in section five.

Device structure and Computational models

The schematic and simplified geometry of double gate pentacene based field effect transistor is illustrated in Fig.1 (a). The proposed DG-OFET is a combination of BG-TC, Fig.1(b), and BG-BC, Fig.1(c), OFET structures with two gate electrodes on the top and bottom of the structure. The main benefit of DG-OFET is the coverage of top gate electrode across the device from source to drain, that facilitates reduction of source/drain contact resistance. The initial design parameters are summed up in Table. 1. The width of the device is 1000 μm , while in the simulation, the results are scaled to 1 μm . The numerical simulations are performed by device simulator, ATLAS [17], and subsequent models are activated for assessing the device performance:

- Carrier mobility models considering the effect of dopant density and impurities on carrier mobility are activated.
- The effect of horizontal and vertical electric field on the mobility of holes is taken into consideration.
- The main current mechanism of organic transistor is based on the drift and diffusion of carriers from source to drain in which the gate bias modifies the charge density in the channel. Accordingly, the related models regarding the transport of holes along the device are activated.
- The effect of traps at the gate insulator/ channel interface on the electrical characteristics of the proposed device is activated.

RESULTS AND DISCUSSION

The proposed DG-OFET structure has two gates with a similar work function value that are designed to be electrically connected. Basically,

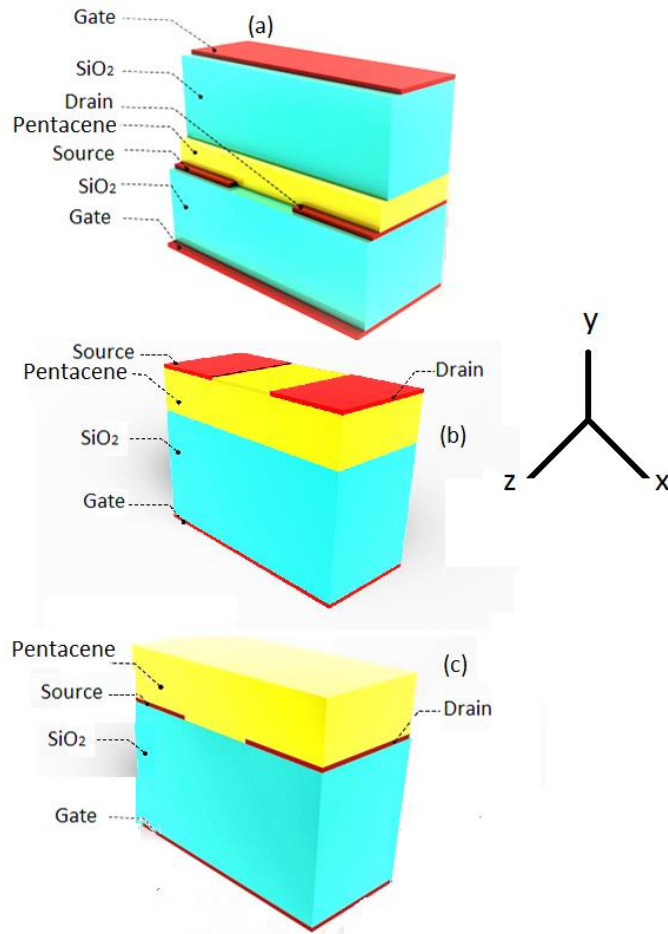


Fig. 1: Schematic of (a) DG-OFET (b) BG-TC and (c) BG-BC pentacene based field effect transistor.

Table 1. Initial design parameters of DG-OFET

Parameter	Value
Channel Length (L_{ch})	30 μ m
Source and Drain Length	30 μ m
Gate Length (L_G)	90 μ m
Thickness of Source/Drain Electrodes	5nm
Pentacene Thickness (T_{ch})	100nm
Gate Insulator Thickness (T_{ox})	300nm
Workfunction of Source/ Drain electrodes	4.9eV
Gate Workfunction (WF_G)	4.2eV
Drain-Source Voltage (V_{DS})	-2V
Gate Voltage (V_{GS})	0:-20V

pentacene based p-channel organic MOSFET operates in the accumulation mode and gate voltage modulates the hole density in the channel. In addition, the related source and drain metal

contact work function are different from the gate work function. Due to the Fermi level energy difference between the source/drain contact and the underlying organic semiconductor, high

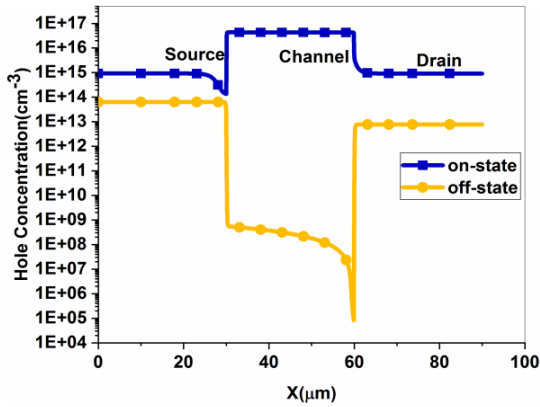


Fig. 2: Hole density along the device from source to drain in the off-state and on-state, for $V_{DS} = -2V$.

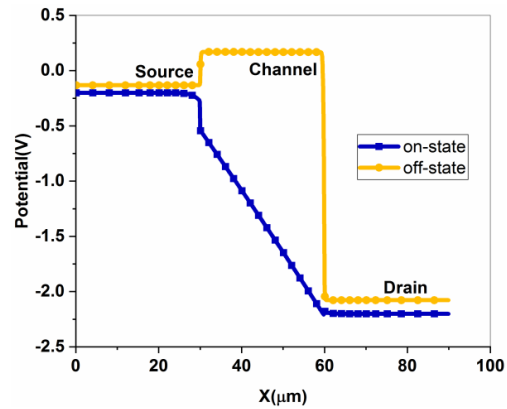


Fig. 3: Potential along the device from source to drain in the off-state and on-state, for $V_{DS} = -2V$.

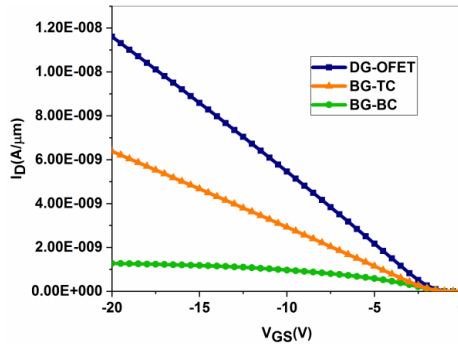


Fig. 4: The transfer characteristics of double gate and single gate organic MOSFET with top and bottom source/ drain configuration, for $V_{DS} = -2V$.

concentration of holes is induced in the source and drain. The main specification of the suggested structure is the deposition of metal gate contact across the whole length of the device, which can control the hole density in the source, drain and channel regions. In other words, the gate contact assists the hole accumulation in these regions, which as a result, reduces the hole density gradient between the source/drain and channel in the on-state.

The hole density distribution in the off-state and on-state are presented along the device from source to drain, depicted in Fig.2. In the absence of gate voltage, the source/drain metal work function plays a fundamental role and effectively modulates the source/drain hole concentration. Due to the hole density gradient between channel and source region, a potential barrier is created at the interface, which effectively reduces the off-state leakage current. On the other side, by the increment of

gate voltage towards a sufficient negative value, considerable amount of holes is accumulated in the channel. Fig.3 depicts the potential distribution along the device in the off-state and on-state operation. In the off-state, there exists a potential barrier at the source-channel junction, reducing the hole diffusion rate from source into the channel. However, the increment of negative gate bias accumulates holes in the channel, facilitating the transport of carriers towards the drain.

The transfer characteristics ($I_D - V_{GS}$) of DG-OFET are depicted in Fig.4 and the results are compared to BG-TC and BG-BC structures. It is generally accepted that DG-OFET has the capability to attain better gate control over the channel with the added advantage to increase the drain current. In BG-BC single gate structure, the source/drain charge density is modulated by the related contact work function and gate voltage merely controls the channel charge concentration. Accordingly,

Table 2. Electrical parameters of three different organic transistors

Structure	I_{on} (A/ μm)	I_{off} (A/ μm)	V_{th} (V)	I_{on}/I_{off}
BG-TC	6.38E-9	1.11E-18	1.86	5.75E+9
BG-BC	1.28E-9	3.09E-19	1.91	4.14E+9
DG-OFET	1.16E-8	4.9E-19	1.57	2.37E+10

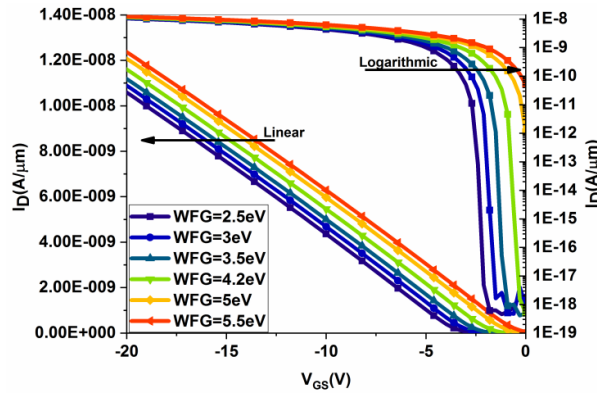


Fig. 5: The transfer characteristics of DG-OFET as a function of gate workfunction, for $V_{DS}=-2V$.

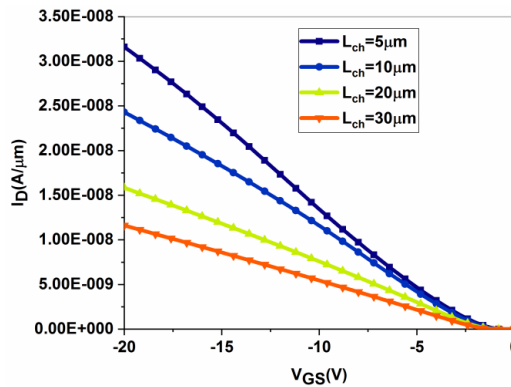


Fig. 6: The transfer characteristics of DG-OFET as a function of gate length, for $V_{DS}=-2V$.

high potential barrier at the source-channel junction results in considerable reduction of off-state current. By contrast, in BG-TC structure, the potential barrier at the source-channel interface is reduced, which can enable better performance as compared to BG-BC structure. The double gate structure takes the advantage of low off-state current of BG-BC structure and improved on-state current of BG-TC device, providing superior performance in terms of on/off current ratio and higher immunity towards short channel effects. The electrical characteristics of the proposed structures are summed up in Table.2.

The work function value of metal gate is an essential design measure that can effectively

modify the off-state current and threshold voltage of DG-OFET. The transfer characteristics of the device are illustrated in Fig.5, while the gate work function is parameterized. Clearly, the off-state current considerably increases as the gate work function enhances towards 5.3eV. The metal gate work function value determines the channel flat band potential, which, in turn, affects the charge accumulation in the channel. It is worth mentioning that tuning on metal gate work function value is viable for efficient performance of the device.

The effect of gate length scaling on the electrical performance of DG-OFET is depicted in Fig.6, while the gate length is parametrized from $L_G=30\mu\text{m}$ to $L_G=5\mu\text{m}$. The gate length scaling

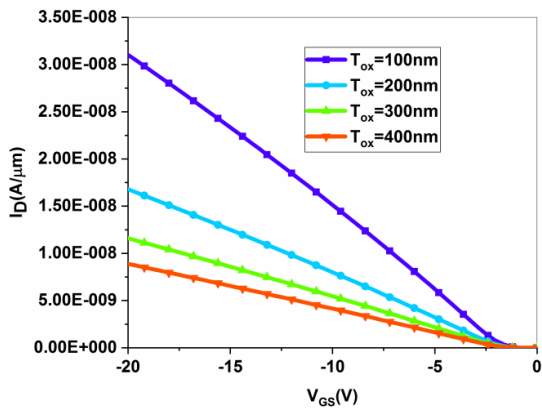


Fig. 7: The transfer characteristics of DG-OFET as a function of gate oxide thickness, for $V_{DS} = -2V$.

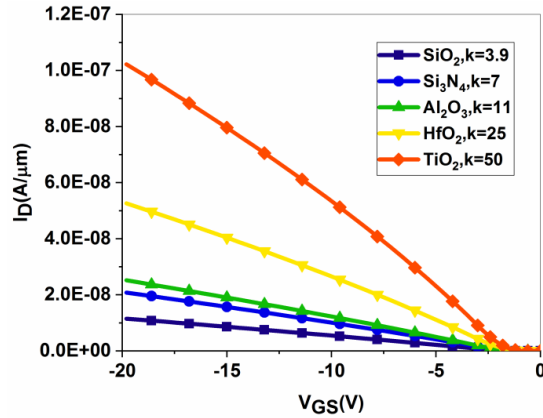


Fig. 8: The transfer characteristics of DG-OFET as a function of gate insulator permittivity.

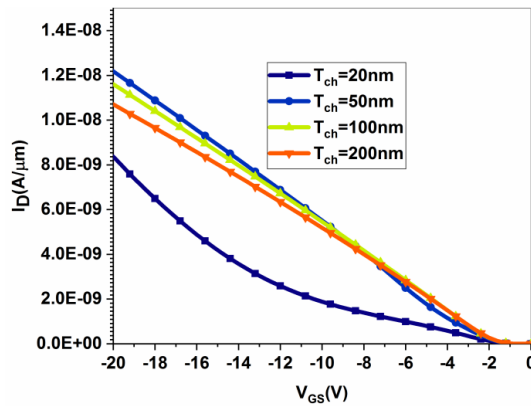


Fig. 9: The transfer characteristics of DG-OFET as a function of pentacene thickness, for $V_{DS} = -2V$.

of DG-OFET improves the charge transit time along the channel, yielding higher drive current to insignificant change in the off-state current. It is well established that in DG-OFET architecture, optimization of performance in terms of high on/off current ratio and high frequency operation is highly dependent upon the gate capacitance.

The effect of gate insulator capacitance on the electrical characteristics of the DG-OFET are demonstrated in Fig.7, while the SiO_2 thickness is varied from 400nm to 100nm. In particular, the gate capacitance effectively adjusts the potential barrier at the source-channel interface, modifying charge injection properties. Clearly, the drive current is considerably improved as the gate insulator thickness is scaled down to 100nm, yielding an increased gate capacitance due to the accumulated charge in the channel region. By definition,

employment of high-k dielectric improves the gate coupling over the channel that eventually allows charge density in the channel to be highly associated with the gate oxide capacitance. The transfer characteristics of the device are illustrated in Fig.8, for different gate oxide materials with dielectric constant ranging from 3.9 (SiO_2) to 50 (TiO_2). The results demonstrate that the usage of high-k dielectrics as the gate insulator significantly improves the on-state current as well as providing low gate leakage current.

Channel thickness is an important design factor that can affect the device efficiency, mainly in the nanoscale regime. The results depicted in Fig.9 demonstrate the considerable dependence of DG-OFET performance to the pentacene thickness. In fact, reduction of pentacene thickness up to 50nm results in better gate control over the channel. In

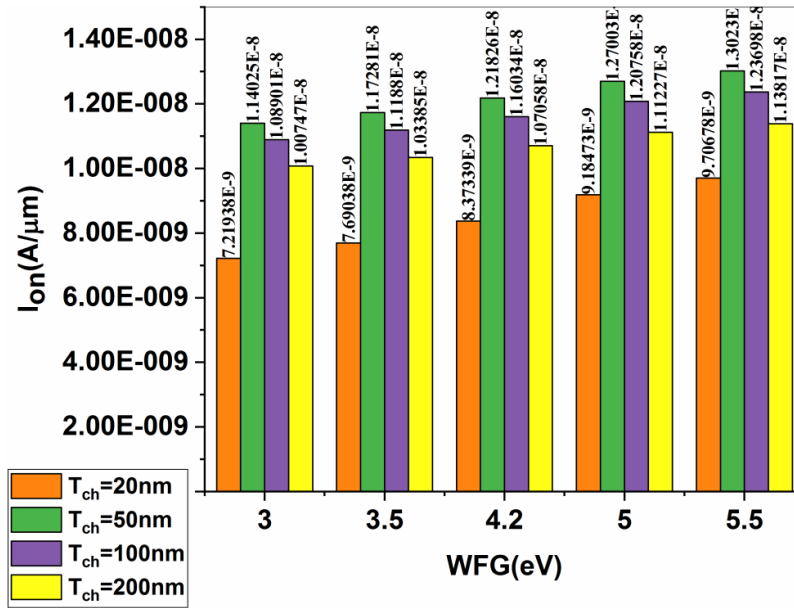


Fig. 10: Maximum on-state current of DG-OFET as a function of pentacene film thickness for different gate work function values.

this situation, the charge density in the channel is considerably increased, providing higher drive current. By contrast, further reduction of channel thickness below 50nm leads to the increment of threshold voltage and degradation of on-state current. In order to discuss this abnormal behavior in nanoscale regime, two parameters should be taken into consideration: the contact resistance and the carrier mobility. The contact resistivity is expected to scale directly with the pentacene thickness, which may reduce the on-state current. In addition, thin film pentacene is highly disordered and carriers have very low mobility, which signifies the low drain current.

It is well demonstrated that the metal gate work function can significantly modify the charge density in the channel. Evidently, to induce considerable amount of holes in the ultra-scaled channel with improved electrical performance, appropriate gate material should be chosen. Fig.10 presents the maximum on-state current as the gate work function and channel thickness are varied, providing a comprehensive roadmap for tuning the gate work function in different channel thicknesses. It is to be noted that as the channel thickness shrinks down, higher gate work function value should be assigned for improving the device performance.

Next, impact of temperature (T) on device

performance is assessed and the results are presented in Fig.11. The drain current increases as the temperature reaches to room temperature. However, further increasing the temperature degrades the carrier mobility and has an adverse effect on device performance. In addition, main analog parameters of the device including transconductance (gm) and current gain are calculated, presented in Fig.12. The cutoff frequency of 1MHz is achieved for DG-OFET which provides paves the way for high frequency application of the device. The transconductance can be further improved by employing high-k dielectric materials for the gate insulator.

The bar chart depicted in Fig.13, demonstrates the sensitivity of essential electrical measures as a function of device design values. Basically, all the design parameters are adjusted to their nominal values and then, one specific parameter is hanged and following that, mean value and standard deviation of selected electrical parameters are calculated. The sensitivity in percentile is calculated as the standard deviation over average value of each electrical parameter for a particular design parameter. Based on statistical analysis, a low sensitivity indicates that the data set is close to the related mean value and variation of a particular design parameter has negligible effect on the electrical efficiency of the device.

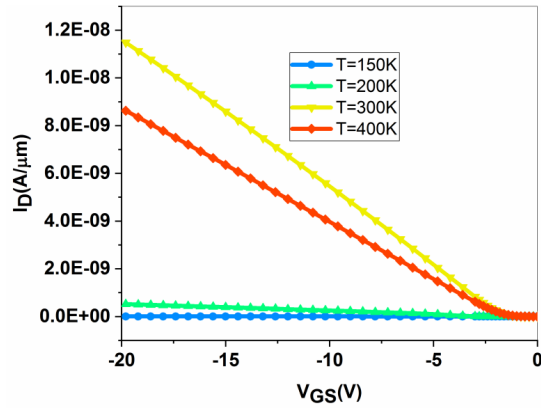


Fig. 11: The transfer characteristics of DG-OFET as a function of temperature, for $V_{DS} = -2V$.

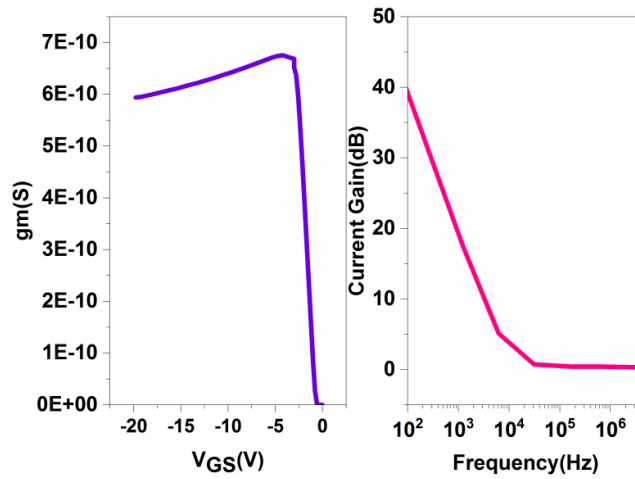


Fig. 12: Analog parameters of DG-OFET including gm and current gain for $V_{DS} = -2V$.

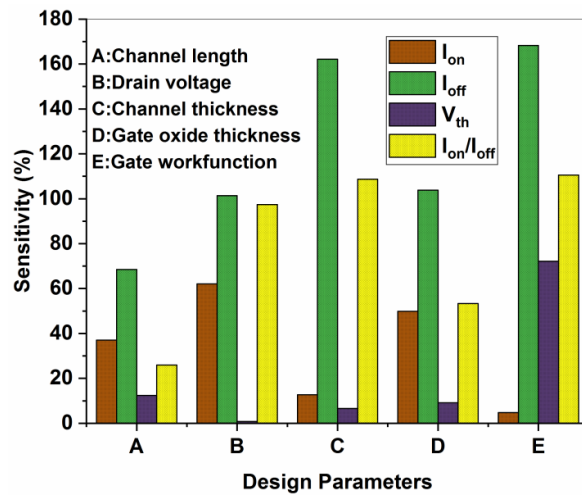


Fig. 13: Sensitivity bar chart of related DG-OFET main electrical parameters as a function of essential design measures.

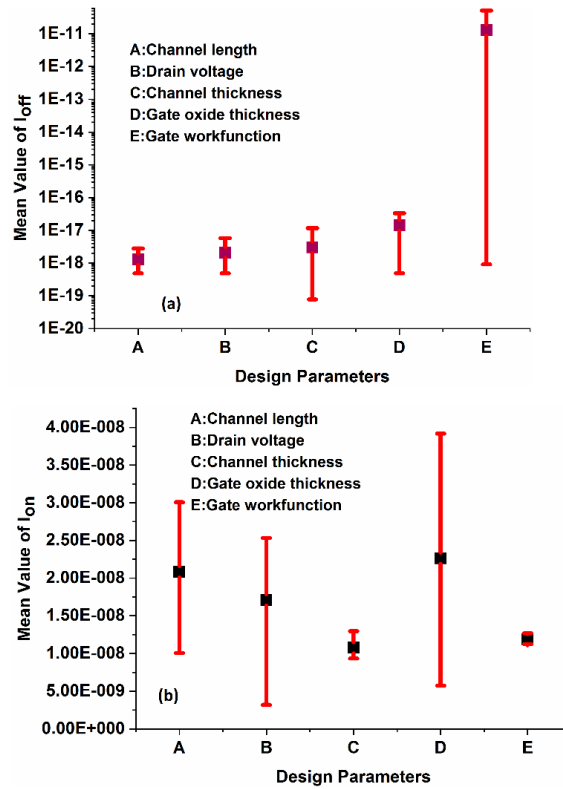


Fig. 14: Mean value and variation range of (a) off-state current and (b) on-state current of DG-OFET as a function of main design parameters.

The results demonstrate that threshold voltage is highly sensitive to the change of metal gate work function. Moreover, the main benefit of DG-OFET is the low susceptibility of threshold voltage to the variation of drain bias and gate length shrinkage, which provides an application of the device in the nanoscale regime. Moreover, regarding off-state current, gate work function and pentacene film thickness are substantial parameters that may modify device proficiency. Evidently, gate work function considerably affects induced hole density in the channel and modifies the off-state potential barrier at the source-channel interface. Channel thickness is another critical factor that can change the DG-OFET performance in the nanoscale regime. Clearly, reduction of channel thickness can effectively modify hole concentration in the channel, source and drain regions. The on-state current is greatly susceptible to drain voltage and effective gate oxide capacitance. Evidently, the drain voltage affects the carrier drift velocity. However, the gate oxide capacitance effectively mutates the charge concentration in the channel and the device

operation can be further improved by reduction of gate oxide thickness and employment of high-k dielectric materials (HfO_2 , $k=25$) as the gate insulator [18]. In addition, channel length scaling can reduce the transit time of carriers, improving the on-state current. Generally, one of the essential application of DG-OFET can be switches, that require high value of on/off current ratio as well as reduced static power dissipation in the off-state operation. The sensitivity analysis reveals that optimum value should be calculated for the gate work function and channel thickness in case of improving device switching performance.

Fig. 14(a) illustrates the related mean value and variation range of on-state current as a function of different design parameters. Clearly, on-state current faces an outstanding variety while the drain voltage is parametrized. The gate insulator thickness is another factor that affects the gate coupling over the channel, modifying the hole concentration in the channel. Moreover, average value as well as variation domain of off-state current with respect to the variation of critical

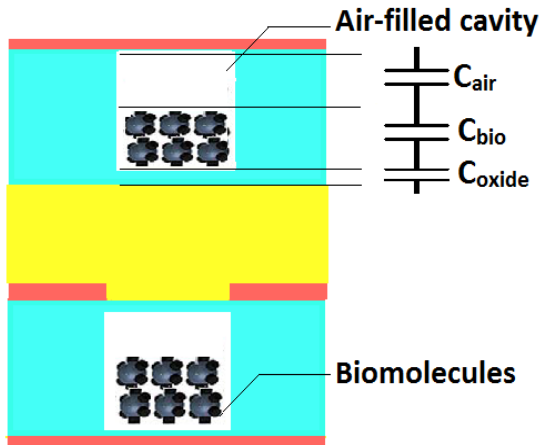


Fig. 15: Schematic of the dielectric modulated biosensor in which a hollow is created in the gate insulator.

design parameters are illustrated in Fig.14 (b). Clearly, a particular positive aspect of the proposed device is the limited alternation range of off-state current with respect to the channel length scaling and drain bias variation, facilitating application of the nanoscale DG-OFET. However, one of the challenges associated with the application of organic transistor is the high sensitivity of off-state current to the gate workfunction, making it essential to find appropriate material for the gate.

Nanogap Biosensor Based on Double Gate Organic Transistor

The schematic of double gate dielectric modulated nanogap DG-OFET is illustrated in Fig.15. The main feature of dielectric modulated DG-OFET involves the embedded hollow in the gate insulator at which certain molecules are collected [19-20]. The fabrication process of the device is fully compatible with the CMOS fabrication process. The gate insulator can be fabricated via atomic layer deposition (ALD) technique, which provides uniform highly resistive dielectric film. Following that, wet etching is used to form the few nanometer nanogap. It is worth to be noted that the upper gate electrode acts like a mask and cannot be etched by hydrofluoric acid (HF) solution (38-40% HF:H₂O=1:70). One distinguished feature of the introduced biosensor is the high susceptibility of on-state current to the variation of gate dielectric permittivity, which modifies the gate capacitance.

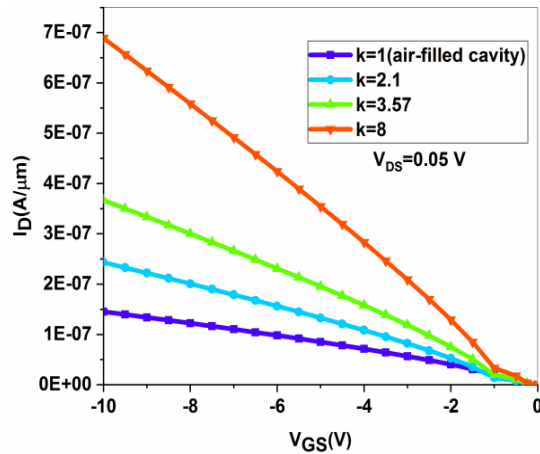


Fig. 16: Transfer characteristic of dielectric modulated biosensor as a function of permittivity of the absorbed biomolecule. The drain current in the case of air-filled nanogap is presented for comparison.

The dielectric layer between the top /bottom gate and the underlying organic material is composed of an air hole in which specified biomolecules are accumulated. In case of storage of biomolecules in the hollow, dielectric constant of the cavity differs from air ($k=1$) to the specified value of different biomolecules, resulting in the variation of gate capacitance and the drain current. In addition, for simulating absorption of different biomolecules in the nano cavity, the permittivity of the nanogap is changed with respect to the concentrated molecules. The biomolecules which are considered includes protein ($k=8$), 3-aminopropyltriethoxysilane (APTES)($k=3.57$) and streptavidin($k=2.1$) [21]. The size of biomolecules is accounted in the range of deca nanometer for protein and nearly 5nm for streptavidin [22]. In addition, based on experimental results, accumulation of streptavidin within hollow of 10nm length is reported [23]. Accordingly, hollow length of 100nm in vertical direction seems sufficient.

The transfer characteristics of nanogap DG-OFET is illustrated in Fig.16 as the drain current is calculated before and after the absorption of different biomolecules. It is evident that the drain current improves as the permittivity of the nanogap is enhanced. The drain voltage is considered as $V_{DS}=-0.05V$ for increasing the sensitivity of biosensor. It is well established that variation of nanogap permittivity leads to the modulation of gate capacitance and as a consequence, a

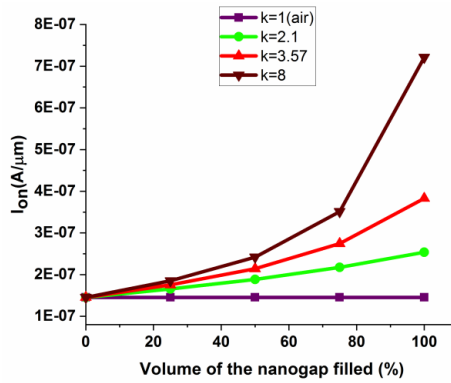


Fig. 17: On-state current of DG-OFET versus volume of the hollow that is filled by biomolecules with different dielectric permittivity.

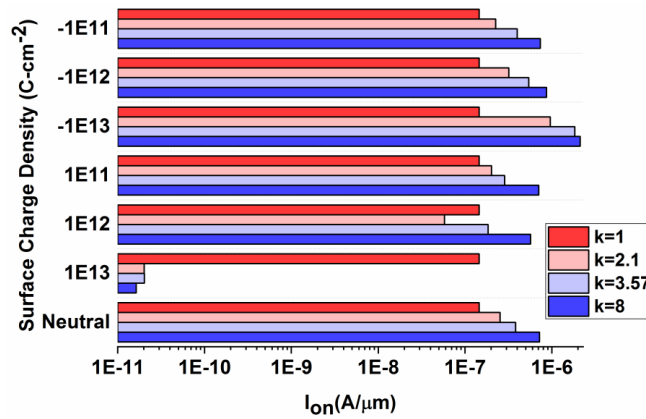


Fig. 18: On-state current bar chart of dielectric modulated biosensor for neutral, positively and negatively charged biomolecules. The drain current in the case of air-filled nanogap is presented for comparison.

considerable variation of drain current is achieved. It is essential to survey sensitivity of DG-OFET based biosensor upon the percentage of nano cavity capacity filled with molecules. The on-state current versus the occupancy of the hollow is illustrated in Fig.17 for different molecules. It is evident that on-state current increases as the higher percentage of the hole is filled with immobilized biomolecules. In particular, the gate capacitance can be calculated as follows:

$$\frac{1}{C_G} = \frac{1}{C_{bio}} + \frac{1}{C_{air}} + \frac{1}{C_{oxide}} \quad (1)$$

$$\frac{1}{C_{bio}} + \frac{1}{C_{air}} = \frac{T_{bio}}{k_{bio}\epsilon_0} + \frac{T_{air}}{k_{air}\epsilon_0} \quad (2)$$

In which, C_{bio} is the capacitance of cavity that is accumulated by molecules, C_{air} is the related

capacity of the air-filled cavity, C_{oxide} shows the gate oxide capacitance, ϵ_0 denotes the vacuum permittivity and $k_{bio(air)}$ represents relative permittivity of the biomolecule (air). Moreover, $T_{bio(air)}$ represents the thickness of nanogap that is filled by biomolecule (air). Evidently, the increment of filled cavity results in the dominant role of C_{bio} , improving the gate coupling over the channel.

Basically, the charge of the absorbed biomolecules can effectively modulate the charge density in the channel. The effect of neutral, positive and negative charge density are comprehensively assessed and the results are illustrated in the bar chart of Fig.18. Negatively charged biomolecules as well as dielectric constant of biomolecules can significantly modulate the channel hole density and as a consequence, can modify the maximum on-state current. Clearly, negatively charged absorbed

molecules attract holes to the surface of the channel and amplifies the gate electric field. Accordingly, the sensitivity of the biosensor can be comprehensively improved. However, on the other side, molecules with positive charge repel holes from the surface and reduces the current, degrading the performance of the biosensor.

CONCLUSION

In summary, the electrical performance of double gate organic field effect transistor is comprehensively investigated. The double gate structure provides superior efficiency in terms of on-state current and on/off current ratio. Sensitivity analysis reveals that gate work function and gate insulator thickness are substantial design measures that may modify the performance of DG-OFET. In addition, scaling of pentacene film thickness results in the enhancement of source/drain contact resistance and reduction of carrier mobility, degrading the device performance. It is well established that metal gate work function engineering is essential for optimizing the efficiency of the device. The low susceptibility of off-state current to the drain voltage variation and gate length scaling is a key advantage for the application of the proposed structure in the nanoscale regime. Next, the cavity embedded in the gate insulator of organic transistor provides the feasibility of this device as an efficient dielectric modulated biosensor. It is worth notifying that for achieving the highest sensitivity after the accumulation of molecules, maximum volume of the hollow should be filled by the biomolecules.

CONFLICT OF INTEREST

The authors declare that there is no conflict of interests regarding the publication of this manuscript.

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