RESEARCH ARTICLE

Influence analysis of dielectric pocket on ambipolar behavior and high-frequency performance of dual material gate oxide stack -double gate Nano-Scale TFET

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ARTICLE INFO

Article History:
Received 2021-10-29
Accepted 2022-03-30
Published 2022-06-30

Keywords:
Dual material,
Oxide stack,
Dielectric pocket,
Double gate TFET,
Ambipolar current.

ABSTRACT

In this paper, a new Nano-Scale structure of dual material gate oxide stack-double gate TFET (DMGOS-DG TFET) with the inclusion of the dielectric pocket (DP) is proposed in the drain region. Hence, the gate consists of three parts, named M1, M2, and M3 with work functions of ϕ_{M1}, $\phi_{M2,}$ and ϕ_{M3} respectively. The work function engineering with the gate oxide stack (SiO_2 as the bottom layer and HfO_2 as the top layer) improves on current, leakage current and ambipolar behavior. In addition, the dielectric pocket (DP) has been used in the drain region to achieve better ambipolar performance. Moreover, it is found that in comparison with the low-k DP (SiO_2), the presence of the high-k DP (HfO_2) provides a lower ambipolar current due to the greater depletion width in the drain region. Furthermore, the ambipolar behavior of the DP-DMGOS-DG TFET structure has been investigated by changing the length and thickness of the high-k DP. Finally, the comparative analysis of DMGOS-DGTFET and high-k DP-DMGOS-DG TFET on high-frequency performance reveals that DP inclusion reduces the gate-to-drain capacitance, which leads to the improved cut-off frequency.

How to cite this article
Ebrahimnia M., Sedigh Ziabari S. A., Kiani-sarkaleh A., Influence analysis of dielectric pocket on ambipolar behavior and high-frequency performance of dual material gate oxide stack -double gate Nano-Scale TFET. J. Nanoanalysis., 2022; 9(2): 90-98. DOI: 10.22034/jna.2022.1943631.1277.

INTRODUCTION

Low dissipation power and high speed are the main goals in the semiconductor industry that requires device scaling. Continuous downscaling of the feature size of the MOSFET has some problems such as short channel effects and high leakage current [1, 2]. Since the conduction of carriers in MOSFET relies on thermionic injection over the potential barrier, the value of sub-threshold slope (SS) is limited to 60 mv/decade. These problems indicate that MOSFET is not a suitable option for the future design of low-power applications. Hence, the tunnel-field-effect transistor (TFET) is introduced as the best alternative to MOSFET in the Nano-Scale regime. In Nano-Scale TFETs, the transfer of charge carriers from source to channel depends on band-to-band tunneling (BTBT). Because of this, Nano-Scale TFETs offer a steep sub-threshold slope of less than 60 mv/decade and a low Leakage current. Despite these benefits, Nano-Scale TFETs face limitations such as poor on current (I_{ON}) and ambipolar conduction [3-9]. So far, many techniques have been proposed to increase I_{ON}. These techniques include the double gate architecture [8-10], strain engineering

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[11], a p-n-p-n structure with source pocket [12, 13], L-shaped channel TFET [14, 15], band-gap engineering, and gate work function engineering [16]. Moreover, numerous techniques have been proposed to improve ambipolar behavior at negative gate voltage. The overlap and underlap of the gate-drain [17, 18], Gaussian doping in drain region [19, 20], hetero-structure [21, 22], hetero-gate-dielectric [23] are some of the approaches used to reduce ambipolarity. Recently, splitting the drain region to remove ambipolar current has been reported. This method relies on heavy doping in the upper part and light doping in the lower part of the drain region [24-26].

In this work, using dual work function, oxide stack (SiO_2/HfO_2) and dielectric pocket, a novel Nano-Scale structure of dual material gate oxide stack-double gate TFET (DMGOS-DG TFET) with the dielectric pocket (DP) based drain region is introduced. Therefore, the work function of the source/drain-side gate segments is less than the work function of the middle gate segment. The lower work function of the gate segment near the source enhances I_{ON} due to the increased tunneling rate at the channel-source boundary, whereas the lower work function for the gate segment near the drain limits off current (I_{OFF}) and ambipolar conduction due to the reduced tunneling probability at the channel-drain boundary [27, 28]. Then the dielectric pocket is incorporated in the drain region for further suppression of ambipolar conduction. The performance of DP-based TFET for analog/RF applications has been investigated [28-33]. The use of DP in the drain region increases the tunneling barrier width at the boundary between the channel and the drain. This increase in width mitigates ambipolar current. By choosing the proper length, thickness, and dielectric material for the pocket, ambipolar current can be greatly reduced without damaging on current, threshold voltage, and sub-threshold slope. Then the high-frequency performance of DMGOS-DG TFET with and without DP is investigated, which shows that the presence of DP can improve the gate-to-drain capacitance and cut-off frequency. The rest of the paper is organized as follows: Section 2 describes the fundamentals of Nano-Scale DG TFET. Section 3 elaborates the proposed device structure and the simulation method. Section 4 discusses the simulation results. Finally, in Section 5, the main findings of the results are summarized.

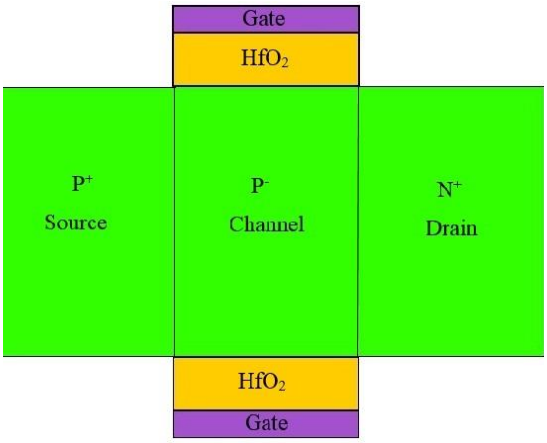


Fig. 1. Schematic view of Nano-Scale DG TFET.

FUNDAMENTALS OF NANO-SCALE TFET

Nano-Scale TFET is a P-I-N structure in Nano-dimensions. The doping types of the drain and source regions are opposite in a TFET. For the N-type TFET, the source is P^+-doped while the drain is N^+-doped. For the P-type TFET, The types of doping of the drain and source regions are reversed. The channel can be an intrinsic or lightly doped P-type or N-type semiconductor. In the N-and P-type TFET, the dominant carriers in the channel region are electrons and holes, respectively [8, 9]. In this section, we described the Nano-Scale double gate TFET (DG TFET) in detail.

Basic Structure

Fig. 1 shows the basic structure of the Nano-Scale DG TFET. The device behaves as the N-type TFET. For suppression of ambipolar behavior, the doping source is considered higher than the drain doping. High doping in the source region is essential to increase the on current. The silicon body thickness is assumed to be small to improve I_{ON}. The double-gate structure in the Nano-Scale DGTFET improves gate control on the channel [34, 35]. The device design parameters are given in Table 1.

Qualitative Behavior

The qualitative behavior of Nano-Scale DG TFET is described by energy band profile and transfer characteristics. Fig. 2(a) and (b) show the energy band profile of Nano-Scale DG TFET in the OFF and ON states. The TFET is in the OFF-state when the gate voltage is zero. It can be seen from Fig. 2(a) that the source valence band is not

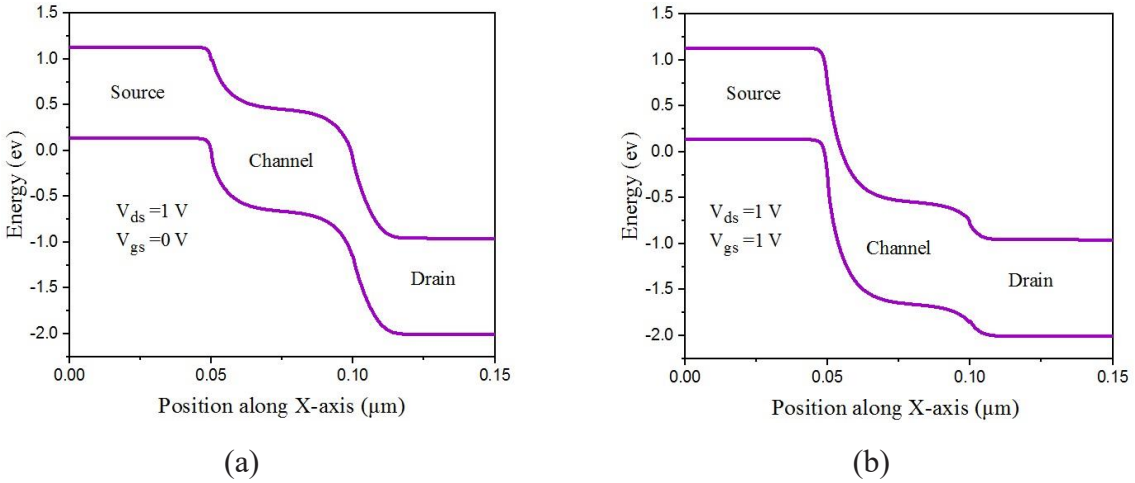


Fig. 2. Energy band profile (a) OFF state (b) ON state of Nano-Scale DG TFET.

Table 1. Design parameters of Nano-Scale DG TFET.

Parameter	value
Source doping	1×10^{20} cm^{-3}
Drain doping	5×10^{18} cm^{-3}
Channel doping	1×10^{17} cm^{-3}
Channel length	50 nm
HfO_2 gate oxide thickness	3nm
Gate work function	4.5 eV
silicone body thickness	10 nm

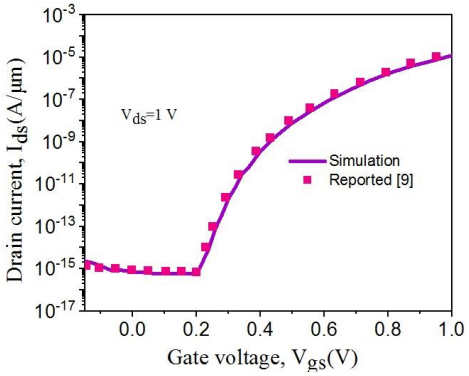


Fig. 3. Transfer characteristics of Nano-Scale DG TFET.

aligned with the channel conduction band. In the OFF state, electrons in the channel conduction band tend to transfer to the drain region. However, since the doping source is P-type, very few electrons can be transferred from the source to the channel. This leads to a very low OFF current. When the gate voltage sufficiently increases, the source valence band is aligned with the channel conduction band, as shown in Fig. 2(b). As a result, electrons can tunnel from the source to the channel. The gate voltage at which this alignment of the valence band and conduction band occurs is the beginning of the ON state of the device. Fig. 3 shows the transfer characteristics of Nano-Scale DG TFET. It is clear from the figure that the I_{OFF} is very low under V_{gs} =0 V. As V_{gs} increases, current boosts due to the narrowing of the tunneling barrier. The I_{ds}-V_{gs} curve obtained in Fig. 3 is in close agreement with the results reported in [9].

PROPOSED DEVICE STRUCTURE AND SIMULATION METHOD

Fig. 4 depicts the schematic view of DMGOS-DG TFET with the presence of the dielectric pocket (DP) in the drain region. The stacked oxide is composed of SiO_2 and HfO_2. Furthermore, the gate separated into three segments, called tunneling gate (M1), control gate (M2), and auxiliary gate (M3) with work functions ϕ_{M1}, ϕ_{M2}, and ϕ_{M3} under lengths L1 = 15 nm, L2 = 20 nm, and L3 = 15 nm, respectively. The work functions of the tunneling gate and the auxiliary gate are the same (ϕ_{M1} = ϕ_{M3} = 4 eV) which are less than the control gate work function (ϕ_{M2} = 4.4 eV). For single material gate oxide stack-double gate TFET (SMGOS-DG TFET), the work function of the entire gate is equal to 4.4 eV. The thickness of the silicon-based body is 10 nm. The length of the source, channel, and drain regions is assumed to be 50 nm. The doping concentrations of P^+ source and N^+ drain regions are considered to be 1×10^{20} cm^{-3}

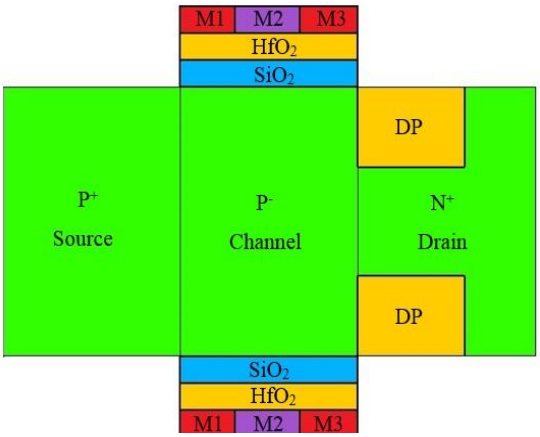


Fig. 4. Schematic view of DP-DMGOS-DG TFET.

Table 2. Design parameters of DP-DMGOS-DG TFET.

Parameter	value
DP length (L_{DP})	30 nm
DP thickness (T_{DP})	3 nm
Dielectric constant of HfO_2	25
Dielectric constant of SiO_2	3.9
SiO_2 gate oxide thickness	1nm
HfO_2 gate oxide thickness	1nm

and 5×10^{18} cm^{-3}, respectively. The channel region has a lowly doped P-type with a concentration of 1×10^{17} cm^{-3}. Details of other parameters are given in Table 2. All simulations are performed using the Silvaco-Atlas simulator. Due to the band-to-band tunneling process in TFET, it is necessary to select the non-local BTBT model to investigate changes in the electric field at any point in the tunneling area. The band-gap narrowing model has also been used to investigate the effect of high doping in the source and drain regions. In addition to the models mentioned, the Shockley-Read-Hall recombination model, auger recombination model, and electric field and concentration-dependent mobility have also been used to achieve exact simulation results.

RESULTS AND DISCUSSION

DC Characteristics

In this section, the effect of dual work function and dielectric pocket on the DC performance of the device is investigated. Fig. 5 shows that the DMGOS-DG TFET provides a higher on current, lower off current, and improved ambipolar conduction compared to SMGOS-DG TFET. Enhancing

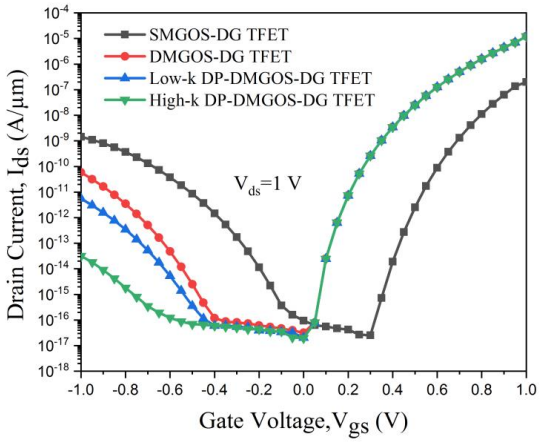


Fig. 5. Comparison of transfer characteristics between SMGOS-DG TFET, DMGOS- DG TFET, low-k DP-DMGOS-DG TFET, and high-k DP-DMGOS-DG TFET.

the on current is due to the lower tunneling gate work function (ϕ_{M1}), which narrows the tunneling barrier at the channel-source interface. While the lower auxiliary gate work function (ϕ_{M3}) expands the tunneling barrier at the channel-drain interface, which degrades off current and ambipolar conduction. Furthermore, the presence of the dielectric pocket (DP) in the drain region of DMGOS-DG TFET expands the tunneling barrier at the channel-drain interface, leading to a further reduction of ambipolarity without changing the on current. As can be observed from Fig. 5, the choice of a high-k material (HfO_2) for the pocket results in lower ambipolarity for V_{gs} < -0.4 V compared to the low-k material (SiO_2). Fig. 6(a) and (b) exhibit the energy band profile of SMGOS-DG TFET, DMGOS-DG TFET, and low/high-k DP-DMGOS-DG TFET in ON and ambipolar states. As shown in Fig. 6(a), the inclusion of DP in the drain region does not change the tunneling width at the channel-source interface. In consequence, the DMGOS-DG TFET has the same on current with and without DP. It is also evident from Fig. 6(b) that tunneling width at the channel-drain junction is maximum when the high-k material is embedded in the drain region of the DMGOS-DG TFET.

Fig. 7 shows the lateral electric field profile of all four structures in the ambipolar state. It can be noticed from the figure that due to the presence of the dielectric pocket, the fringing field in the vicinity of the channel-drain junction is wider. Furthermore, the inclusion of the high-k material causes a greater depletion width in the drain region compared to low-k material. Therefore, high-k DP-DMGOS-DG TFET reduces the tunneling of

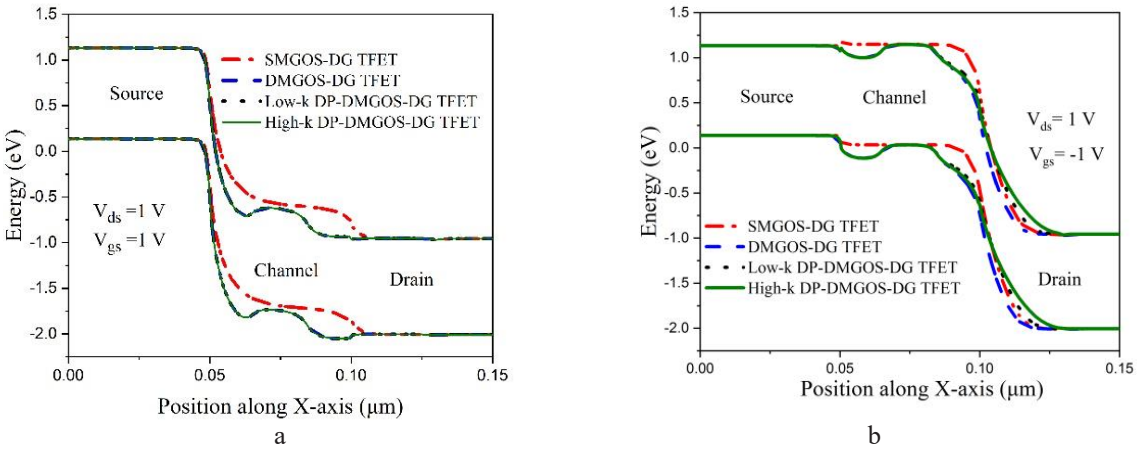


Fig. 6. Comparison of energy band profile (a) ON state (b) ambipolar state between SMGOS-DG TFET, DMGOS-DG TFET, low-k DP-DMGOS-DG TFET, and high-k DP-DMGOS-DG TFET.

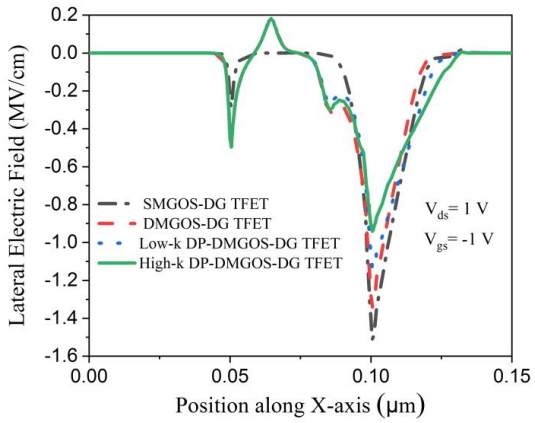


Fig. 7. Comparison of lateral electric field among SMGOS-DG TFET, DMGOS-DG TFET, low-k DP-DMGOS-DG TFET, and high-k DP-DMGOS-DG TFET.

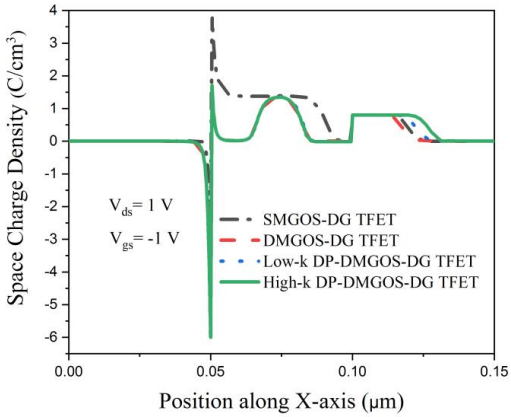


Fig. 8. Comparison of space charge density among SMGOS-DG TFET, DMGOS-DG TFET, low-k DP-DMGOS-DG TFET, and high-k DP-DMGOS-DG TFET.

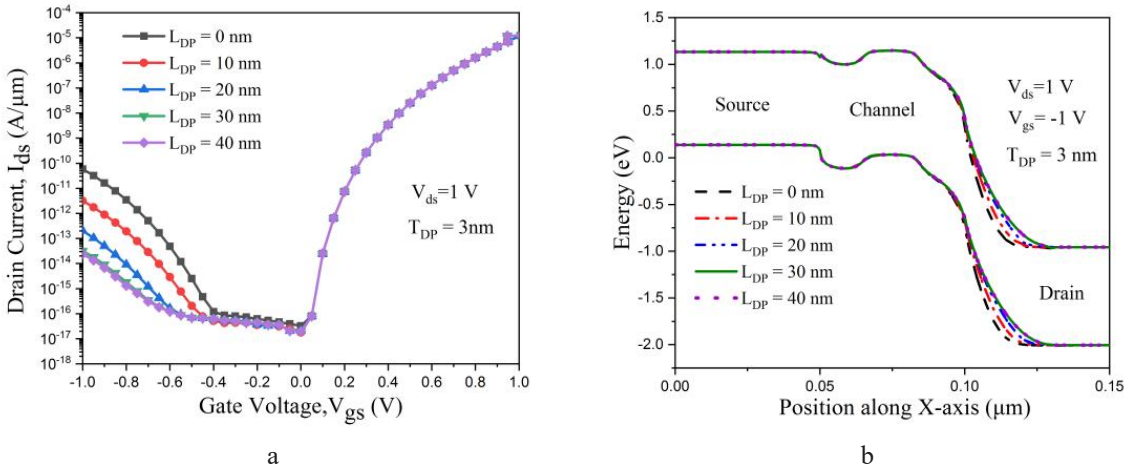
carriers due to the largest depletion width in the drain region and the lowest value of field peak at the channel-drain junction. As a result, the minimum ambipolarity is obtained by the presence of the high-k material in the drain region. For further analysis, the space charge density of different structures is plotted in Fig. 8. It can be observed that high-k DP-DMGOS-DG TFET has more space charge width in the drain region compared to other structures. Hence enlargement of barrier width occurs at the channel-drain tunneling junction, which eventually leads to a lower I_{amb}. Therefore, DMGOS-DG TFET with high-k DP (HfO_2) can be introduced as the proposed structure. The comparative performance of the proposed high-k DP-DMGOS-DG TFET with other structures is shown in Table 3.

Effect of Lenght and Thickness of High-k Dielectric Pocket

In this section, the effect of changing the length and thickness of the dielectric pocket on the transfer characteristics of high-k DP-DMGOS-DG TFET is analyzed. Fig. 9(a) shows that when the DP length (L_{DP}) changes from 0 to 30 nm, the ambipolar current decreases from 5.87×10^{-11} to 4.19×10^{-14} A/μm. The reduction in I_{amb} is consistent with increasing the pocket length up to 30 nm, and for $L_{DP} > 30$ nm, more reduction is not observed. The ambipolarity dependence on L_{DP} can be better investigated from Fig. 9(b) by comparing the energy band profiles for different pocket lengths. As the high-k DP length increases to 30 nm, the tunneling barrier width in the channel-drain interface is expanded. Consequently, the ambipolar current

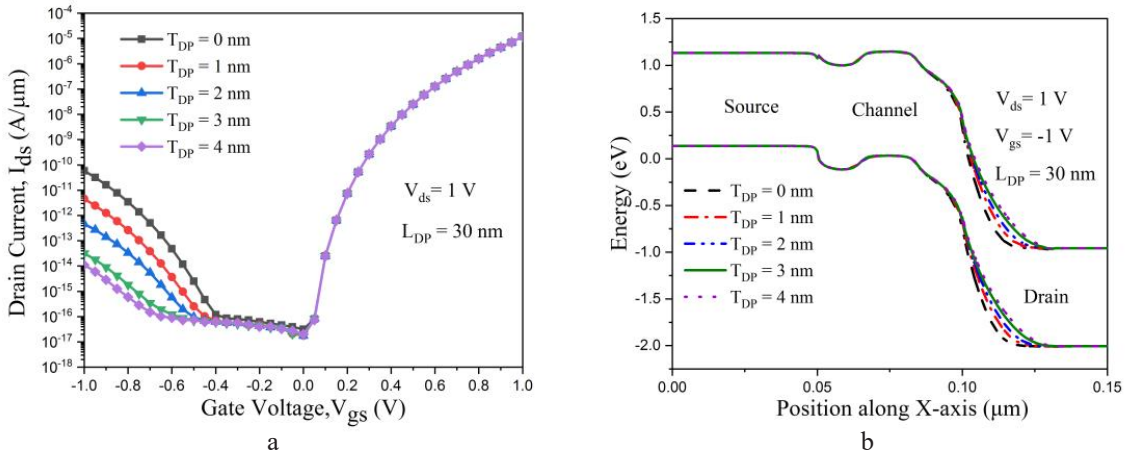
Table 3. Performance comparison of SMGOS-DG TFET, DMGOS-DG TFET, low-k DP-DMGOS-DG TFET, and high-k DP-DMGOS-DG TFET.

Parameter	SMGOS-DG TFET	DMGOS-DG TFET	low-k DP-DMGOS-DG TFET	high-k DP-DMGOS-DG TFET
I_{ON} (A/μm)	1.99×10^{-7}	1.22×10^{-5}	1.22×10^{-5}	1.22×10^{-5}
I_{OFF} (A/μm)	1.51×10^{-16}	1.65×10^{-17}	1.63×10^{-17}	1.63×10^{-17}
I_{amb} (A/μm)	1.44×10^{-9}	5.87×10^{-11}	5.51×10^{-12}	4.19×10^{-14}
V_{th} (V)	0.58	0.31	0.31	0.31
SS (mV/dec)	35.2	20.1	20.1	20.1



a b

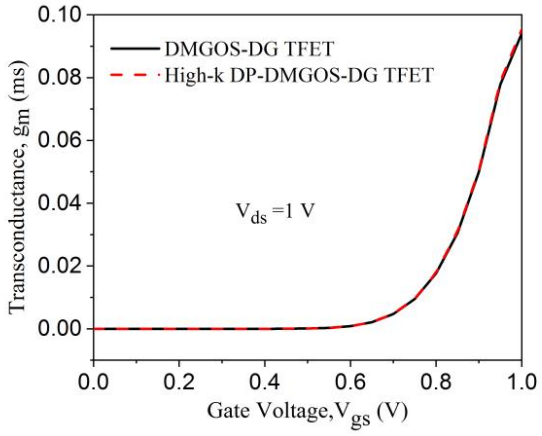
Fig. 9. (a) Transfer characteristics (b) energy band profile of high-k DP-DMGOS-DG TFET with different length of DP.



a b

Fig. 10. (a) Transfer characteristics (b) energy band profile of high-k DP-DMGOS-DG TFET with different thickness of DP.

is reduced. The widening of the barrier is mainly due to the increase in the depletion width on the drain side. As can be noticed from Fig. 10(a) that the ambipolar conduction is decreased gradually with increasing the DP thickness (T_{DP}) from 0 to 3 nm, and for T_{DP} > 3 nm, there is no remarkable change in ambipolar behavior. The energy band profile for different pocket thicknesses is plotted in Fig. 10(b). It is clear from the figure that the tunneling barrier at the channel-drain interface expands with increasing thickness, which reduces ambipolar conduction. Furthermore, inserting the dielectric pocket in the drain region is ineffective in the tunneling rate of carriers at the channel-source interface. Therefore, the on current is constant with changing the pocket dimensions.



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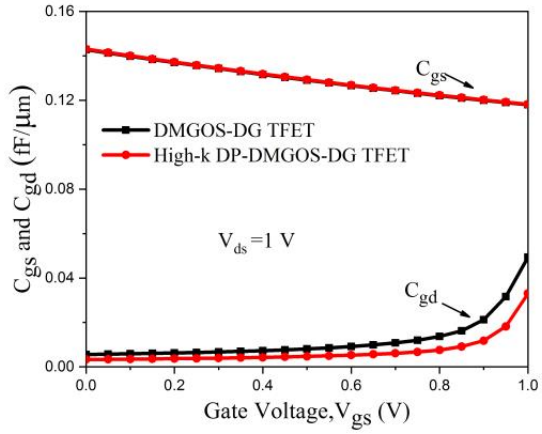

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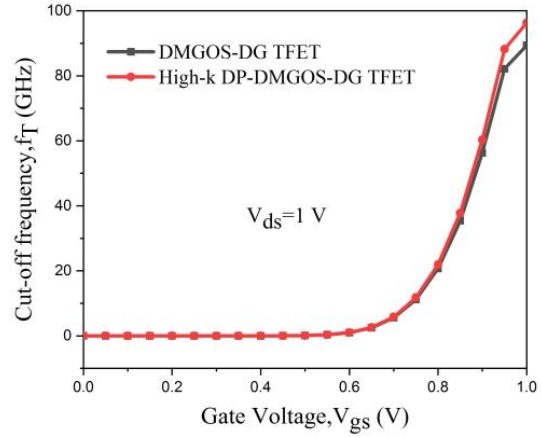

c

Fig. 11. Comparison of (a) trans conductance (b) gate-to-source/drain capacitance (c) cut-off frequency between DMGOS-DG TFET, and high-k DP-DMGOS-DG TFET.

High-Frequency Performance Analysis

In this section, the effect of the high-k dielectric pocket on the high-frequency parameters of DMGOS-DG TFET is investigated in detail.

Fig. 11(a) compares the transconductance (g_m) of DMGOS-DG TFET with and without high-k DP under different V_{gs}. As expected, there is no difference between the two structures in g_m because the DP inclusion near the channel-drain junction does not change the tunneling distance between the source valence band and the channel conduction band in the ON state.

Fig. 11(b) shows the variety of gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}) versus V_{gs} for DMGOS-DG-TFET with and without high-k DP. Since the inversion layer is not formed on the drain side at the lower V_{gs} values, both the capacitances C_{gs} and C_{gd} are only comprised of parasitic capacitances. But when the value of V_{gs} increases, first the inversion layer is created on the drain side, and then with further increase in V_{gs}, it is extended towards the source. As a result, C_{gd} begins to increase at higher V_{gs}. Meanwhile, C_{gs} is mainly composed of parasitic capacitance and with increasing gate voltage, no notable change in its value is observed [31, 32]. Furthermore, it is obvious from Fig. 11(b) that the value of C_{gs} in DMGOS-DG TFET is unchanged with the DP application, while the value of C_{gd} decreases with the presence of DP. The reason for this decrease is the depletion region is created by DP.

One of the most basic RF parameters is the cut-off frequency (f_T), computed as [36]

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (1)$$

The variation of f_T versus V_{gs} for DMGOS-DG TFET with and without high-k DP is shown in Fig. 11(c). Since both the g_m and C_{gs} parameters are independent of the DP effect on DMGOS-DG TFET, f_T is dependent only on C_{gd}. Thus, high-k DP-DMGOS-DG TFET offers a higher cut-off frequency under higher gate voltage due to C_{gd} reduction.

CONCLUSION

In this paper, a novel structure of dual material gate oxide stack-double gate TFET (DMGOS-DG TFET) is proposed with the presence of the dielectric pocket (DP). A stacked gate oxide with the work function engineering is applied to increase

the on current, reduce the off current, and improve the ambipolar behavior. Furthermore, the DP inclusion in the drain region of the DMGOS-DG TFET is suppressed ambipolar conduction without affecting I_{on}, SS, and V_{th}. It is demonstrated that the use of high-k DP (HfO_2) provides the ambipolar current of 4.19×10^{-14} A/μm at V_{gs} = -1V, which is less than that of low-k DP (SiO_2). The length and thickness of the high-k dielectric material are then optimized to achieve the minimum ambipolarity. Additionally, the study of the high-frequency performance of DMGOS-DG TFET with and without high-k DP illustrates that the DP effect improves the cut-off frequency by decreasing C_{gd}, while it is ineffective on g_m and C_{gs}.

CONFLICT OF INTEREST

The authors declare no conflicts of interest.

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