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Reduction of Components in Cascaded Multilevel Inverters by Using a New Basic Unit

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Abstract

Todays, the multilevel inverters are becoming popular for medium/high power applications. In the meantime, the cascaded multilevel inverters use less power electronic elements. In this paper, first, a new basic unit is proposed for cascaded multilevel inverters. The basic unit is capable of producing four positive output voltage levels. Then, to achieve a higher number of voltage levels at the output side, several basic units are used in series connection. Because the proposed basic unit cannot produce zero and negative levels, so to solve this problem, one H-bridge is used to obtain zero and negative output voltage levels. The proposed topology is analyzed and different factors such as rating voltage, number of levels, required DC voltages sources, power electronics components, and gate driver circuits are calculated. Moreover, the proposed inverter is compared with several other topologies. As a result, the proposed topology needs to less number of power electronic elements, DC voltage sources and gate driver circuits. To prove the correct operation of the proposed topology, the simulation results of a nine-level inverter in PSCAD/EMTDC software program are used.

Keywords

Asymmetric cascaded multilevel inverter, Cascaded multilevel inverter, H-bridge, Symmetric cascaded multilevel inverter.

1. Introduction

Over the last five decades, the use of multilevel inverters (MLIs) has been developed due to the demand for medium/high voltage and higher power converters that can produce high quality waveforms. Multilevel converters consist of the combination of several DC voltage sources and semiconductor switches that are capable of producing high voltage step waveforms at the output. The rating voltage of these switches is much lower than the output voltage due to the dependence on the amplitude voltage of the connected DC sources. Also, low switching losses, electromagnetic wave interference (EMI) and high efficiency have increased the attractiveness of multilevel inverters for researchers [1-9]. Among the three main types of multilevel inverters with the names neutral-point-clamped (NPC), flying capacitor (FC) and CHB multilevel inverters, due to their modularity and simplicity of control, have attracted the attention of many Researchers have proposed different structures based on this inverter [10-14]. Multilevel CHB inverters are divided into two main groups, symmetrical configuration consisting of DC voltage sources with the same amplitude and asymmetrical configuration consisting of DC voltage sources with different amplitude. In the meantime, asymmetric inverters produce more voltage levels in the output, despite having more power electronic elements and as a result, having a larger size and more cost compared to symmetric inverters [15, 16].

In the last few decades, the importance of reducing the number of elements and increasing the number of output voltage levels has led researchers to work on different and new structures. In structures of [2, 5, 9, 15, 16], both symmetric and asymmetric configurations are considered for voltage sources. The switches used in asymmetric structures presented in [8], [10], [17,18] bear high rating voltage and also the large number of DC voltage sources used in them increases the cost of these structures. In the structure of [19], the number of DC voltage sources is reduced, but the use of active elements such as capacitors increases the volume of the circuit and the voltage balance problem of the capacitors. In the first part of this paper, a new basic level inverter topology is proposed, which can produce all levels (odd and even) in the output using the H-bridge. In the next section, several basic units of the proposed topology are connected in cascade and a new multilevel inverter structure is presented. After calculating the amplitude of DC voltage sources and determining the equations of the number of used power electronic elements, it compares with some recent and popular topologies.

2. Proposed Basic Cascaded Multilevel Converter Structure

Fig.1, proposes a new basic structure unit for multilevel inverter to produce four levels of output voltage. This structure consists of four unidirectional switches (each switch comprises of an antiparallel diode and an IGBT) and three dc voltage sources. As shown in Fig. 1, turning on the S_1 and S_2 or (S_3 and S_4) switches at the same time causes the voltage sources to be short-circuited. Therefore, these switches should not be turned on at the same time. Table 1, shows the output voltage for different switching states of proposed basic unit in Fig. 1. In this table, 1 and 0 indicate the on and off states of the switches, respectively.

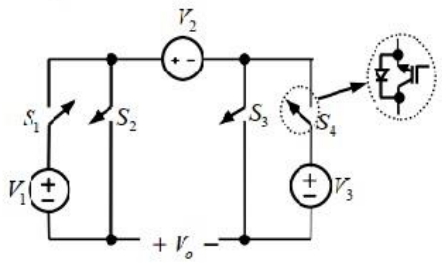


Fig. 1. Structure of the presented basic unit

Table 1. Switching states of proposed basic unit

S_1	S_2	S_3	S_4	v_o
1	0	1	0	$V_2 - V_1$
0	1	1	0	V_2
1	0	0	1	$V_2 - V_1 + V_3$
0	1	0	1	$V_2 + V_3$

By developing the inverter of Fig. 1, which utilizes the n series connection of the basic unit, the proposed inverter shown in Fig.2, is obtained. Since this structure is only able to produce positive voltage levels at the output, the H-bridge is used to produce zero and negative levels. Table 2, shows the output voltage for different switching states of proposed cascaded multilevel inverter in Fig.2. In this structure, the number of output voltage levels (N_{step}), the number of switches (N_{IGBT}), the number of DC voltage sources (N_{source}), the maximum output voltage produced ($V_{o,\max}$) and the variety of the magnitudes of voltage

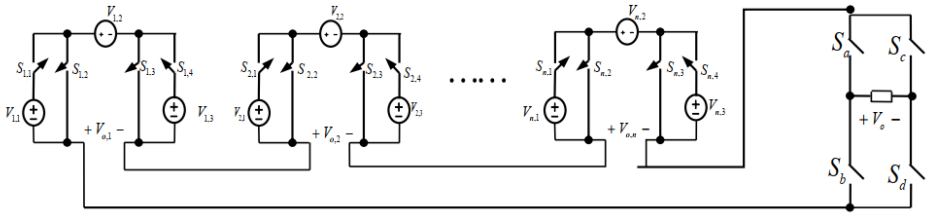


Fig. 2. Proposed cascaded multilevel inverter

sources ($N_{variety}$) are calculated as follows:

$$N_{Variety} = 2n \quad (1)$$

$$V_{S1} = V_1 \quad (2)$$

$$V_{S2} = V_1 \quad (3)$$

$$V_{S3} = V_3 \quad (4)$$

$$V_{S4} = V_3 \quad (5)$$

$$V_a = V_o = V_2 + V_3 \quad (6)$$

$$V_b = V_o = V_2 + V_3 \quad (7)$$

$$V_c = V_o = V_2 + V_3 \quad (8)$$

$$V_d = V_o = V_2 + V_3 \quad (9)$$

Another important parameter is the rating voltage of the switches ($V_{block,1}$), which is calculated by:

$$\begin{aligned} V_{block,1} &= V_{S1,1} + V_{S1,2} + V_{S1,3} + V_{S1,4} \\ &= V_1 + V_1 + V_3 + V_3 \\ &= 2(V_1 + V_3) \end{aligned} \quad (10)$$

Now, the rating voltage of all the switches in the proposed inverter ($V_{block,n}$) is obtained in:

$$\begin{aligned} V_{block,n} &= V_{block,1} + V_{block,2} + V_{block,3} + \ldots + V_{block,H} \\ &= V_{S1,1} + V_{S1,2} + V_{S1,3} \\ &\quad + V_{S1,4} + \ldots + V_{Sn,1} + V_{Sn,2} \\ &\quad + V_{Sn,3} + V_{Sn,4} + V_{Sa} + V_{Sb} \\ &\quad + V_{Sc} + V_{Sd} \\ &= 2V_{1,1} + 2V_{1,3} + \ldots + 2V_{n,1} \\ &\quad + 2V_{n,3} + 4(V_2 + V_3) \end{aligned} \quad (11)$$

3. Determination of the Magnitude of DC Voltage Sources

According to the following algorithm, to create non-repetitive and different output voltage values (v_o), the values of DC voltage sources for each unit are considered according to Table 2.

First unit:

$$V_{1,1} = V_{dc} \quad (12)$$

$$V_{1,3} = V_{1,2} = 2V_{1,1} = 2V_{dc} \quad (13)$$

Second unit:

$$\begin{aligned} V_{2,1} &= V_{o\max,1} + V_{dc} \\ &= 4V_{1,1} + V_{dc} = 5V_{dc} \end{aligned} \quad (14)$$

$$V_{2,3} = V_{2,2} = 2V_{2,1} = 10V_{dc} \quad (15)$$

Third unit:

$$\begin{aligned} V_{3,1} &= V_{o\max,1} + V_{o\max,2} + V_{dc} \\ &= 4V_{1,1} + 4(5V_{2,1}) + V_{dc} \\ &= 25V_{dc} \end{aligned} \quad (16)$$

$$V_{3,3} = V_{3,2} = 2V_{3,1} = 50V_{dc} \quad (17)$$

In general, the amount of DC voltage sources in n units is calculated as follows:

$$V_{n,1} = \sum_{i=1}^{n-1}(V_{o\max,i}) + V_{dc} = 5^{n-1}V_{dc} \quad (18)$$

$$V_{n,3} = V_{n,2} = 2V_{n,1} = 2 \times 5^{n-1}V_{dc} \quad (19)$$

Considering the obtained equations for n units, we have:

$$\begin{aligned} V_{block,n} &= 2n(V_{1,1} + V_{1,3}) \\ &\quad + 4(5^n - 1)V_{1,1} \end{aligned} \quad (20)$$

Table 2. Switching states of proposed basic unit

$S_{1,1}$	$S_{1,2}$	$S_{1,3}$	$S_{1.4}$	$S_{2,1}$	$S_{2,2}$	$S_{2,3}$	$S_{2,4}$	…	S_a	S_b	S_c	S_d	v_o
1	0	1	0	0	0	0	0		1	0	0	1	$V_{1,2}-V_{1,1}$
0	1	1	0	0	0	0	0		1	0	0	1	$V_{1,2}$
1	0	0	1	0	0	0	0		1	0	0	1	$V_{1,2}-V_{1,1}+V_{1,3}$
0	1	0	1	0	0	0	0		1	0	0	1	$V_{1,2}+V_{1,3}$
0	0	0	0	1	0	1	0		1	0	0	1	$V_{2,2}-V_{2,1}$
0	0	0	0	0	1	1	0		1	0	0	1	$V_{2,2}$
…													⋮
1	0	1	0	0	0	0	0		0	1	1	0	$-(V_{1,2}-V_{1,1})$
0	1	1	0	0	0	0	0		0	1	1	0	$-(V_{1,2})$
1	0	0	1	0	0	0	0		0	1	1	0	$-(V_{1,2}-V_{1,1}+V_{1,3})$
0	1	0	1	0	0	0	0		0	1	1	0	$-(V_{1,2}+V_{1,3})$
…													⋮

Considering the mentioned algorithm, the following relationships for n units are obtained:

$$N_{step} = 2 \times 5^n - 1 \quad (21)$$

$$N_{IGBT} = 4n + 4 \quad (22)$$

$$N_{source} = 3n \quad (23)$$

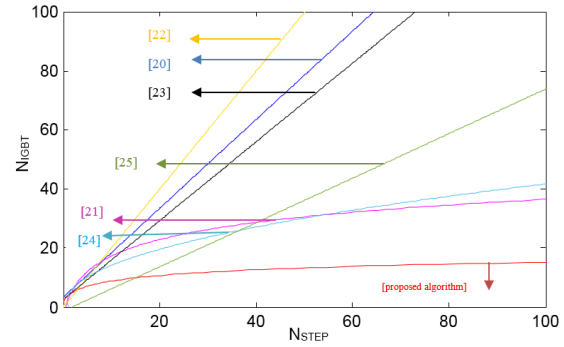
$$N_{driver} = 4n + 4 \quad (24)$$

$$V_{o,\max} = (5^n - 1)V_{dc} \quad (25)$$

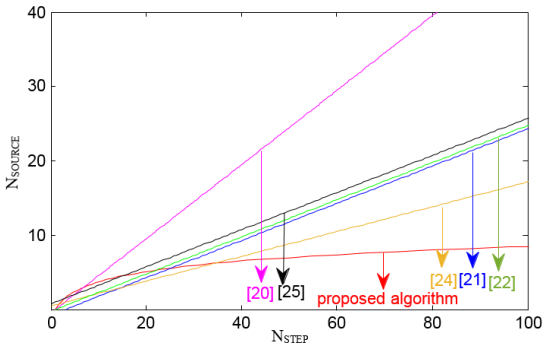
4. Comparison Results

To ensure the accuracy of the performance and confirm the results, the proposed multilevel inverter structure is compared with other conventional structures in different dimensions. First, in this direction, the number of used IGBTs in them is checked. The Fig. 3(a) indicates that the proposed structure uses fewer switches compared to other structures in [20-25]. Comparison of the number of used DC voltage sources is one of the criteria used in the cost and size. In order to compare inverters, in Fig. 3(b), a comparison is made between the number of DC voltage sources used in the proposed structure with structures [20-25], and with this comparison, the less number of DC voltage sources of the proposed structure is highlighted compared to other structures. Fig. 3(c) shows a comparison between the number of gate driver circuits in the proposed multilevel structure with other structures. The results of this comparison indicate that the number of gate driver circuits in the proposed structure is less than the structures of [20-25]. For example, to produce 69 voltage levels at the output, the number of used power electronic elements in different structures is compared numerically in Table 3. Using the findings of this Table, the structures in [20-25] and proposed multilevel inverter need 107, 34, 138, 95, 37, 51 and 8 IGBTs, respectively, to produce 69 voltage levels at the output and the number of used DC voltage sources in the proposed structure is equal to 8 and it is equal to 34, 17, 34, 10, 12, 18 in the

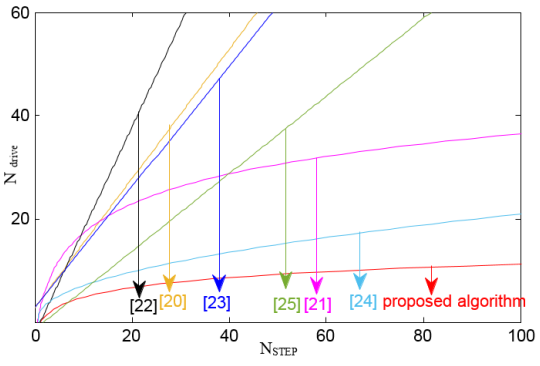
other structures, to produce the same number of output voltage levels. Despite the need for 15 gate driver circuits in the proposed structure, the structure in [20-25] use 89, 34, 136, 84, 18 and 51 gate driver circuit, respectively.



(a)



(b)



(c)

Fig. 3. Comparison results (a) N_{IGBT} (b) N_{source} (c) N_{driver} versus N_{step}

5. Simulation results of proposed 9-level converter

To confirm the results from the mathematical relations, the simulation of the proposed structure for a 9-level cascaded multilevel single-phase inverter is done in the PSCAD / EMTDC software. According to Fig. 1, this structure for $n=1$ consists of four unidirectional switches, one H bridge with four unidirectional switches, 12 IGBTs, 8 gate driver circuits and three DC voltage sources with values of 10V, 20V and 20V for V_1, V_2 and V_3, respectively. All the switches are considered ideal and the assumed load is R-L with values of 50Ω and 55mH for resistance and inductor, respectively. The method used for control is base fundamental frequency switching with 50Hz for output voltage. The output voltage and current waveform is shown in Fig. 4. The sinusoidal nature of the load current is due to the presence of the R-L load in the multilevel inverter, which acts as a low-pass filter for the current. Fig. 5 shows the voltage on the switches of $S_1, S_2, \ldots, S_4, S_a, \ldots, S_d$. The amplitude of positive and zero voltage in the waveform confirms that these switches are unidirectional.

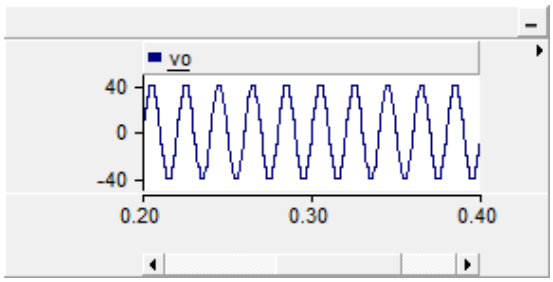
6. Conclusion

In this paper, a basic unit structure using four unidirectional switches and three separate DC voltage sources for multilevel inverter was proposed. Then, several basic units were cascaded together to produce higher voltage levels at the output. By determining the relationships for amplitude

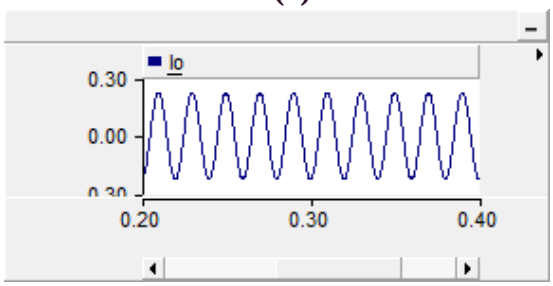
Table 3. Comparison of the proposed structure inverter with other reference structures for producing 69-level

parameters	[20]	[21]	[22]	[23]	[24]	[25]	**proposed structure**
N_{level}	69	69	69	69	69	69	**69**
N_{IGBT}	107	34	138	95	37	51	**13**
N_{source}	34	17	34	10	12	18	**7**
N_{driver}	89	34	136	84	18	51	**13**

of DC voltage sources of the units, the maximum number of levels in the output was obtained. The H-bridge was used to generate negative and zero voltage levels at the output. The proposed structure was compared with other structures from various dimensions, such as used the number of IGBTs and gate driver circuits and DC voltage sources. The result of this comparison showed a reduction in the used number of power electronic elements in the proposed structure and as a result, a reduction in the overall price and size of the new inverter. For example, to produce 69 output voltage levels, the proposed inverter needs 15 IGBTs, 15 gate driver circuits and 8 DC voltage sources, while the structure used in [22, 25], to generate the same number of voltage levels at the output, includes 138, 51 IGBTs and 136, 51 gate driver circuits and 34, 18 DC voltage sources, respectively. Experimentally and with the help of PSCAD/EMTDC software program, the correctness of the recommended structure controlled by the fundamental frequency method has been confirmed for a single-phase 9-level inverter prototype.

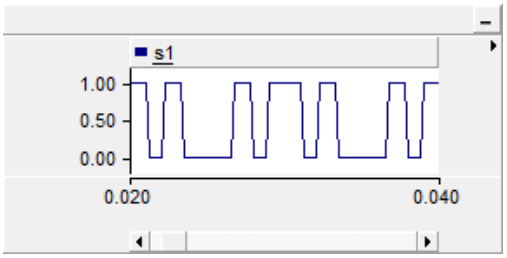


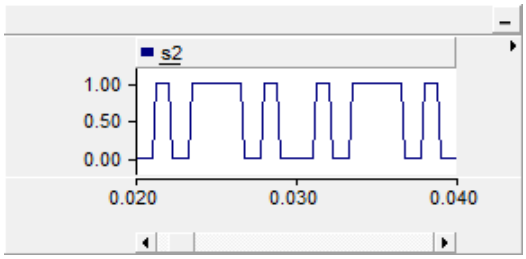
(a)



(b)

Fig. 4. (a) output voltage waveforms **(b)** output current waveforms for 9-level cascaded multilevel in the simulation





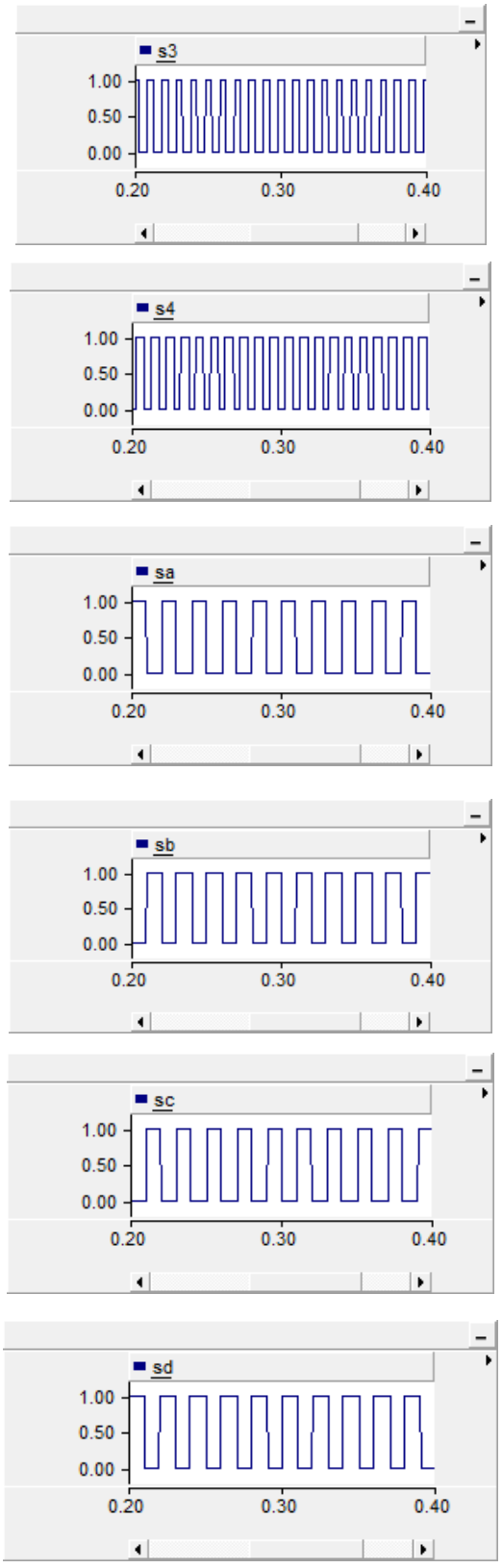


Fig. 5. Voltage waveforms for different switches in the simulation

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