# Design and Realization of a Junction-less TFET for Analog and Digital Applications Based on Strain Engineering

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**ABSTRACT:**
This paper investigates the effects of the uniaxial tensile strain on the performance of an all silicon junction-less tunneling field-effect transistor (JLTFET) for analog and digital applications. The behavior of the JLTFET under global and local uniaxial strain are studied based on the energy band diagram at ON, OFF, and ambipolar states. Under local uniaxial tensile strain, it has been observed that the tunneling length at the channel/source interface in the ON state has been decreased and at the channel/drain interface in the OFF state has been increased. Simulations illustrate improvements in ON current, $I_{ON}/I_{OFF}$ and steep sub threshold swing (SS) and superior transconductance ($g_m$). The strained JLTFET, also demonstrates capability for low-voltage application and high cut-off frequency ($f_T$) and suppressed ambipolar current ($I_{amb}$).

**KEYWORDS:** JLTFET; Band-to-band Tunneling; Local Strain; Global Strain; Ambipolar Current, Cut-off Frequency.

## 1. INTRODUCTION

Low power consumption and steep sub-threshold swing (SS) of tunneling field effect transistors (TFETs), has put it at the center of attention in recent years. The main challenges for TFETs is low drain current due to low band to band tunneling rate in high band gap material such as silicon[1]. The other drawback of TFETs is the ambipolar behavior that limits the design of VLSI/ULSI circuits. The origin of this phenomenon is tunneling path at negative(positive) gate biases between the channel valence band and the drain conduction band in n-TFETs(p-TFETs).To suppress this parasitic behavior, methods such as using Gaussian doping profiles, gate/drain overlap, hetero-structure insulators and gate work function engineering have been employed[2]–[4]. Using smaller band-gap materials such as SiGe, Ge, and III–V materials can improve the TFET performance compared to Si TFETs. Employing new materials with higher carrier mobility and geometrical engineering or other novel methods are considered in VLSI/ULSI circuit design[5]–[8]. The strain engineering can be an attractive alternative among the various methods in device manufacturing because of it no significant additional processing cost. As the strain narrows the energy band diagram of material, this idea can be considered as an alternative for employing lower band gap material such as germanium [9]–[14].

The rest of the paper is organized as follows. Section 2 is an overview of the research background. Section 3 represents the device structure and simulation methodology. Results of all simulation will be discussed in section 4. And finally the conclusion of current study will be presented in section 5.

## 2. LITERATURE REVIEW

Although silicon TFETs demonstrates simple process for CMOS technology, however, the large band gap of silicon degrade the tunneling rate and consequently the tunneling current of TFET. Thus engineering technics such as imposing strain can be considered as practical way to reduce the band gap while manufacturing process remains fully silicon compatible. It has been observed that using tensile strained silicon (s-Si) significantly promotes tunneling currents[15], [16]. As gate scaling, the efficiency of various techniques to induce strain on devices degrades. Also, it has been shown that beyond a certain



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critical strain, additional increase in strain does not result in electron mobility enhancement[17]–[21].

Many researches have been devoted to strain engineering in recent years. In [22] strain engineering on the Electrical Performance of Short Channel InAs has been reported. Impact of strain on drain current and threshold voltage of a double gate TFET reported in[23]. Many studies focused on the assessment of the performance of TFETs under strain engineering[24]–[27].

In this paper, we studied the effects of uniaxial tensile strain on the analog and digital performance of a junction less tunneling FET (JLTFET). A uniformly tensile profile is induced for all regions (Global strain) or only for the Source region (Local strain). Then, we present the simulation results exhibiting considerably enhanced band to band tunneling (BTBT) current due to using highly uniaxial tensile strained silicon in the JLTFET.

## 3. MATERIAL AND METHODS

Fig. (1) shows a 2-D structure of a JLTFET. Drain, source and the channel regions are uniformly doped with donor dopant. The SiO2 separates the control gate (C-gate) and polarity gate (P-gate) electrodes from the channel and the source. Material parameters are listed in Table 1.

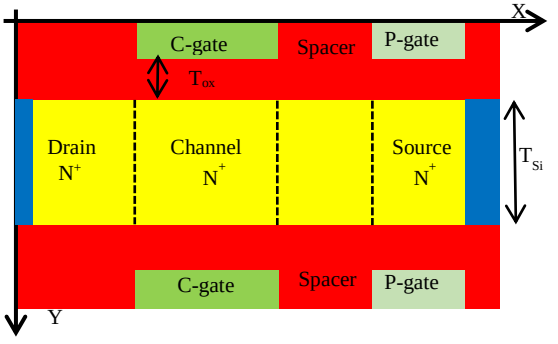


**Fig. 1.** Schematic view of JLTFET.

All simulations have been done in SILVACO ATLAS 2D 5.19.20 R. Because of high impurity atoms in the channel and due to interface trap effect, the Shockley Read Hall (SRH) and Auger (AUGER) recombination models were included in the simulation. We incorporated the effect of Fermi-Dirac statistics in the calculation of the intrinsic carrier concentration required in the expressions for SRH recombination. Assuming high doping concentration, a band-gap narrowing model (BGN) was also included. Quantum confinement effects on BTBT were induced through the use of the quantum confinement model given by Hansch (HANSCHQM). To include a mobility model into the simulation, the Lombardi mobility model (CVT) also employed. The non-local method considers tunneling at an energy level Ei, from the point Pi in the source valence band to the point Qi in the channel conductance band. Using Landauer's tunneling formula, we can write the drain current ID as[28]–[31]:

$$I_D = \frac{2q}{\hbar}\int_{E_{C,channel}}^{E_{V,source}} \left(f_{P_i}(E_i) - f_{Q_i}(E_i)\right) T_{BTBT}(E_i)dE_i \quad (1)$$

Where $f_{P_i}(E_i)$ and $f_{Q_i}(E_i)$ are the Fermi level at energy $E_i$ at points $P_i$ and $Q_i$ respectively, ħ is reduced plank constant and q is electro charge.

**Table 1.** Device design and material parameters.

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Gate oxide thickness | $t_{ox}$ | 2 | nm |
| Body thickness | $t_{si}$ | 5 | nm |
| Drain/Channel/Source doping concentration | $N_D$ | $1 \times 10^{19}$ | $cm^{-3}$ |
| C-gate work function | $W_c$ | 4.7 | eV |
| P-gate work function | $W_p$ | 5.93 | eV |
| Dielectric constant | K | 3.9 | - |

$T_{BTBT}$ is band to band tunneling probability which in general can be calculated by Wetzel-Kramer-Brillouin (WKB) approximation:

$$T_{BTBT} \approx \exp\left(-\frac{4}{3}\frac{\lambda\sqrt{2m^*}}{q\hbar(E_g+\Delta\emptyset)}(E_g)^{3/2}\right) \quad (2)$$

where m* is the electron effective mass, q is the electron charge, ħ is the Plank constant, $\lambda$ is the screening tunneling length of the barrier that depends on device geometry, $E_g$ denotes the energy bandgap and $\Delta\emptyset$ represents the energetic difference between the valence and conduction bands of tunneling regions [32]–[35]. Drain current depends on tunneling probability, which itself is dependent on band bending at the interfaces of the channel-source or channel-drain. The effect of strain on Si band structure can be modeled as [36], [37]:

$$(\Delta E_g)_{s-Si} = 0.4x \quad (3)$$

$$V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) = V_T \ln\left(\frac{m_{h,Si}^*}{m_{h,s-Si}^*}\right)^{3/2} \cong 0.075x \quad (4)$$

$$\emptyset_{F,s-Si} = \emptyset_{F,Si} + (\Delta\emptyset_F)_{s-Si} \quad (5)$$

$$(\Delta\emptyset_F)_{s-Si} = \frac{-(\Delta E_g)_{s-Si}}{2q} + V_T ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) \quad (6)$$

Where x is the germanium mole fraction in $Si_{1-x}Ge_x$ substrate $(\Delta E_g)_{s-Si}$ is the change in the energy band gap of strained silicon. $V_T$ is thermal voltage, $N_{V,Si}$ and $N_{V,s-Si}$ is the density of states in the valence band of non-strained and strained silicon. $(\Delta\emptyset_F)_{s-Si}$ Is the Fermi level modification for strained silicon(s-Si).

## 4. RESULTS AND DISCUSSION

The key issue about this study is to induce a uniform uniaxial tensile strain which has a constant level along the channel direction (x-axis). This uniform tensile strain, is induced once over the entire regions including drain, channel and the source (Global strain), and once only on the source region (Local strain). The high level of tensile strain (5 GPa) induces a band gap shrinkage of 0.2 eV[38]. In this way, we assumed the energy band diagram of JLTFET along the channel as reference ($E_g$=1.1 eV). Based on the aforementioned issues, our study is being developed based on three important assumptions: i) the induced strain is local and global. ii) The Profile of induced strain is uniform in induced region. iii) The induced strain is uniaxial tensile.

The energy band diagram of unstrained and strained JLTFET in OFF ($V_{ds}$=1 V; $V_{gs}$=0 V) and ON ($V_{ds}$=1 V; $V_{gs}$=1 V) states are shown in Fig. 2.

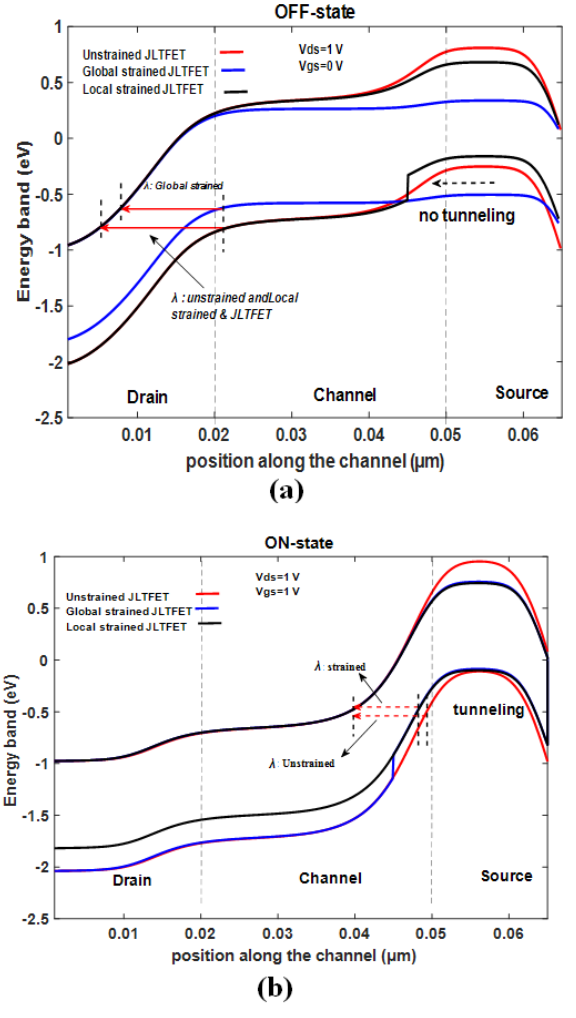


**Fig. 2.** The energy band diagram of unstrained JLTFET and strained JLTFET: a) OFF state b) ON state.

As we expect, the tunneling length in the ON state decreased at source side in both local strained JLTFET and Global strained JLTFET due to band gap shrinkage caused by induced strain. It is clear that in the ON state, tunneling length is narrower and electrons can tunnel from valence band of the source to conduction band of the channel.

The contour plot of electron concentration in the OFF state for unstrained and global/local strained JLTFET are shown in Fig. 3. It should be noted that in the case of global strain (Fig. 3-b), electron concentration in the channel is greater than unstrained JLTFET (Fig. 3-a) and local strained JLTFET (Fig. 3-c). Therefore the electron injection from the channel to the drain region is more.

This is why the OFF current in global strain is more for Global strained JLTFET(Fig.4). In the OFF-state, the electrons in the valence band of the source did not have any available energy state in the channel into which they could tunnel.

In according to Fig. 4, the magnitude of the $I_{OFF}$ in Global strained JLTFET is $1.36\times10^{-8}$ A/μm which is much more than unstrained JLTFET and Local strained JLTFET. As the electron concentration in the channel for Global strained JLTFET is more than the two others, the $I_{OFF}$ is more for this device.

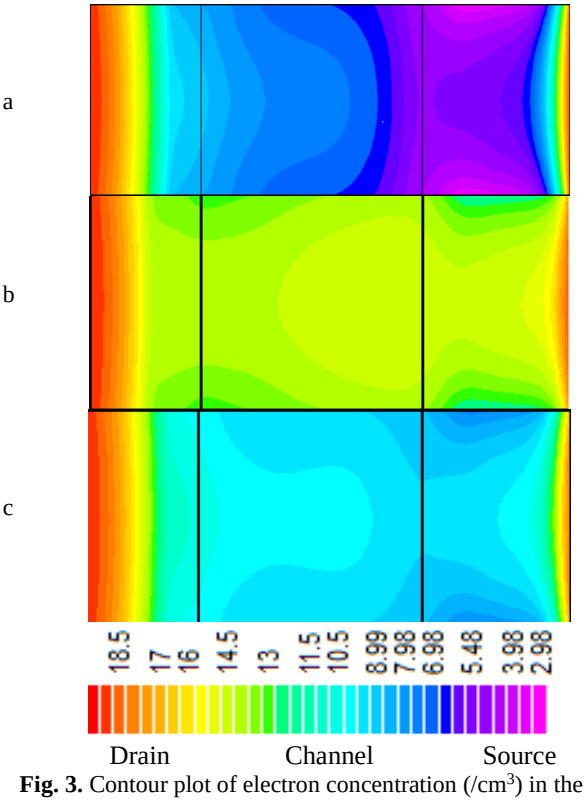


**Fig. 3.** Contour plot of electron concentration (/cm$^3$) in the OFF state: a) unstrained JLTFET b) Global strained JLTFET and c) Local strained.

Increasing gate voltage, the energy bands in the channel are further lowered, and electrons occupying energy levels from the valence band edge of the source to the conduction band edge of the channel can tunnel to the conduction band of the channel. This leads to a steep increase in the drain current.

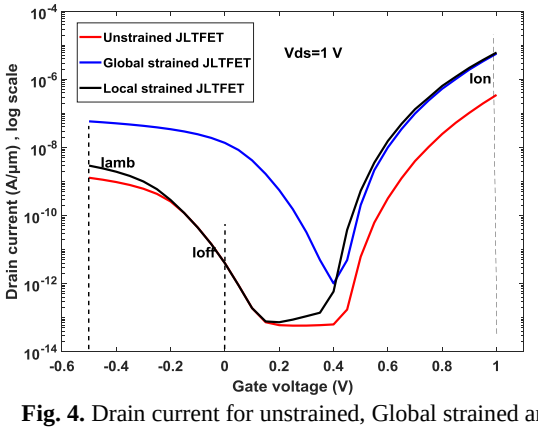


**Fig. 4.** Drain current for unstrained, Global strained and Local strained JLTFET.

It is clear from Fig. 4, although the global strain will improve ON current but OFF and ambipolar current ($I_{AMB}$) will also increase which is undesirable in analog and digital application. One of the main issues related to device performance is the ambipolar current. This current is due to migration of electrons from valence band of the channel to conduction band of the drain at negative gate voltages. The magnitude of the ambipolar current should be as low as possible in order to prevent power loss.

From Fig. 4, the magnitude of $I_{AMB}$ in Global strained JLTFET is greater than local strained JLTFET and unstrained JLTFET. The reason is band gap shrinkage at drain side due to induced global strained. This shrinkage narrows the tunneling length that leads to increase in BTBT rate at channel-drain junction. The electron concentration profile of unstrained and strained JLTFET in the ON state is shown in Fig. 5. For Local and Global strained JLTFET, the electron population at source region is higher than unstrained JLTFET. The reason is lower energy band gap due to strain effect. These electrons participate in BTBT mechanisms which lead to higher ON current. Therefore, for Global and Local strained JLTFET, the more electrons in the source valence band has a chance to travel to conduction band of the channel. This phenomenon results in higher ON current magnitude in Global and Local strained JLTFET in comparison with unstrained-JLTFET. It should be noted for unstrained JLTFET, because of longer tunneling length, the BTBT rate is less than global and Local strained JLTFET. This is why the electron population for unstrained JLTFET is lower than Global and Local strained JLTFET in the channel region.

Based on WKB approximation which considers the tunneling area as a triangle, the BTBT probability depends on the height and the width of the potential barrier. The height of the potential barrier is the Eg of the material. Hence for strained regions this height is the same because of uniform uniaxial strain (Eg=0.92 eV). The length of the potential barrier depends on the slope of the energy bands (i.e. the electric field). The electric field of unstrained JLTFET and strained JLTFET for Global and Local cases are shown in Fig. 6. a higher slope leading to a shorter tunneling length. This junction lies almost at the edge of the source, since the source is heavily doped as compared to the channel.

Hence, the electron at the source edge occupying the energy level, tunnels through a potential barrier. In the OFF-state, for all cases due to the formation of band diagram looks like $N^+$-I-$P^+$ doped device structure, it has been created two electric field peaks at the source-channel and drain-channel junction. Simultaneously, the strained JLTFET because of smaller tunneling barrier has lower values of lateral electric field which leads to the increase of carrier tunneling. However, in the ON-state, due to the presence of gate-source voltage, the energy band diagram behaves similar to $N^+$-N-$P^+$ doped device structure, so it has been created one strong electric filed peak at the source-channel junction which implicates the tunneling probability goes up in that region.

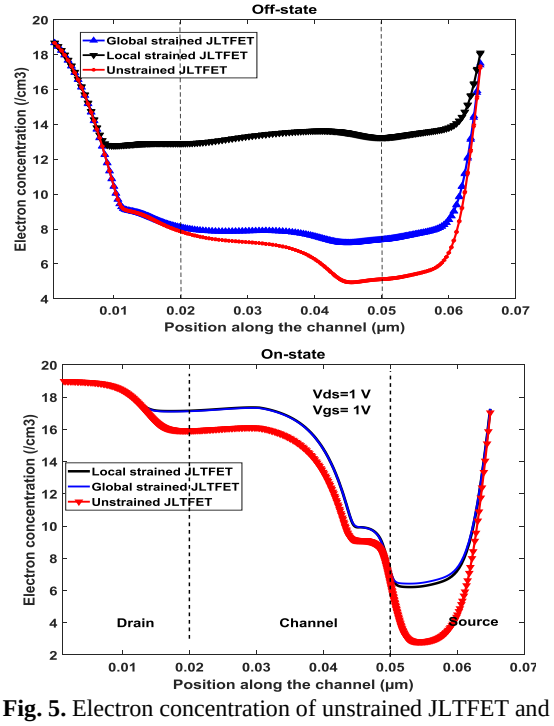


**Fig. 5.** Electron concentration of unstrained JLTFET and strained JLTFET in the OFF/ON state.

(a)

(b)

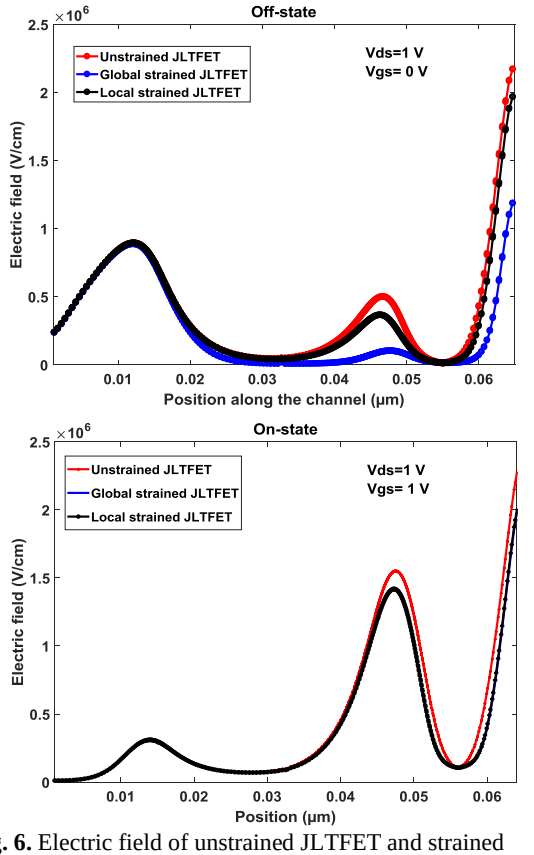


**Fig. 6.** Electric field of unstrained JLTFET and strained JLTFET: a) OFF state b) ON state.

One of the main features of MOS devices is the tranconductance ($g_m$). The $g_m$ determines how the device can transfer gate voltage to drain current.

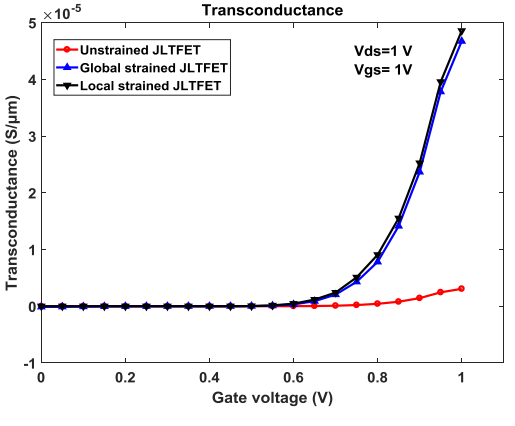


**Fig. 7.** Transconductance for unstrained JLTFET, global strained JLTFET and Local strained JLTFET.

The transconductance of unstrained and strained JLTFET strained are shown in Fig. 7. The $g_m$ for Global and Local strained JLTFET is more than unstrained JLTFET. This means strain can transfer more gate voltages to drain current. This property is one of the main advantages of a device in analog applications.

Cut-off frequency ($f_T$) plays an important role to evaluate the device performance in RF applications, where $f_T$ is the frequency at which short circuit current gain becomes unity, and is defined as follows:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (7)$$

Fig.8. shows the $f_T$ for strained and unstrained JLTFET. As the gate voltage increases, the number of electrons injected from source to channel due to BTBT mechanism is increased, hence, frequencies starts increasing [12]. Fig. 8 clearly shows that inducing uniaxial tensile strain in JLTFET leads to increase of $f_T$ over the entire range of $V_{gs}$ in comparison with unstrained JLTFET. It is seen that in the Global strained JLTFET and Local strained JLTFET, energy band shrinkage due to strain results to shortening of tunneling length which leads to increase in $g_m$ (Fig. 7).

**Table 2.** Device performance for unstrained and Global/Local strained JLTFET.

| Parameter | Unstrained JLTFET | Global strained-JLTFET | Local strained-JLTFET |
|---|---|---|---|
| $SS_{avg}$ [mV/dec] | 20.2 | 38.1 | 16.1 |
| SS [mV/dec] | 32.2 | 30.0 | 27.6 |
| $V_t$ [V] | 0.38 | 0.37 | 0.37 |
| $I_{ON}$ [A/μm] | $3.5 \times 10^{-7}$ | $5.72 \times 10^{-6}$ | $6.15 \times 10^{-6}$ |
| $I_{OFF}$ [A/μm] | $4.0 \times 10^{-12}$ | $1.36 \times 10^{-8}$ | $4.0 \times 10^{-12}$ |
| $I_{ON}$ / $I_{OFF}$ | $8.75 \times 10^{4}$ | $4.2 \times 10^{2}$ | $1.53 \times 10^{6}$ |
| $I_{AMB}$ [A/μm] | $1.28 \times 10^{-9}$ | $5.85 \times 10^{-8}$ | $2.92 \times 10^{-9}$ |

It is noteworthy; the magnitude of cut-off frequency for unstrained JLTFET is ~5 GHz which has a negligible value against strained JLTFET which is ~70 GHz s. As a result, strained JLTFET can be superior candidate for analog application due to utilizing thinner tunneling barrier at the source-channel interface, which leads to the increase the probability of carrier tunneling.

In order to evaluating a device performance in digital application some metrics are used which are listed in Table 2. Sub threshold swing (SS) decreasing is a way to increase the turn-on steepness of the device. This criterion is a way of reducing the voltage supply without performance loss. As SS in TFETs changes with gate voltage, average SS is defined as [34]:

$$SS_{avg} \cong \frac{V_{DD}}{\log(\frac{I_{ON}}{I_{OFF}})} \quad (8)$$

Applying the Global strain and Local strain, decreased point sub threshold slope (SS) by 6.8% and 14.28% respectively by in comparison with unstrained JLTFET. However the average sub threshold swing ($SS_{avg}$), in Global strained JLTFET increased by 88.6% which clearly shows the device performance degraded. In the Local strained HLTFET, ($SS_{avg}$) is 16.1 mV/dec which implicate the Local strained JLTFET is a steep device. This feature is very important especially in digital applications. The threshold voltage for unstrained JLTFET and strained JLTFE does not change dramatically, however the magnitude of threshold voltage is small. The OFF current which is considered as leaky current, leads to more power consumption especially in VLSI devices. The magnitude of OFF current in Global strained JLTFET is much more than unstrained and Local strained JLTFET that results in unacceptable $I_{ON}/I_{OFF}$ ratio. Ion and $I_{ON}/I_{OFF}$ in Local strained JLTFET has been improved by 1657% and 1682% respectively which show very good enhancement. The am bipolar current, in Global strained-JLTFET increased significantly. This increase results to more power consumption in analog or digital application. By inducing local strain, the ambipolar current decreased significantly in comparison with Global strained JLTFET.

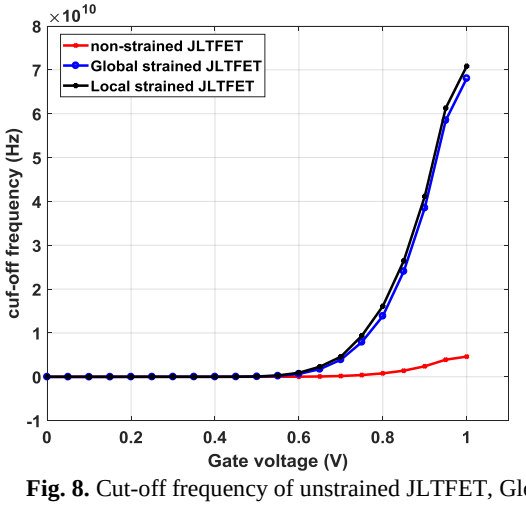


**Fig. 8.** Cut-off frequency of unstrained JLTFET, Global strained and Local strained JLTFET.

## 5. CONCLUSION

The study demonstrates that a local and global uniform uniaxial strain profile with the magnitude of 5GPa corresponding to 2.1 eV band gap shrinkage in a silicon JLTFET can enhance the performance of all-silicon JTFETs as low-standby-power and energy efficient devices. Local strain at source side can raise $I_{ON}$ by 17.57 times in comparison with unstrained JLTFET while keeping $I_{OFF}$. The largest value for $I_{ON}$ to $I_{OFF}$ ratio has been seen for local strain at source side. For the particular device structure and strain level studied in this paper, sub threshold swing (SS) is reduced to 27.6 mV/dec for a device whose band gap is 0.92 eV at the tunnel junction. Simulations illustrate improvements in ON current, $I_{ON}/I_{OFF}$, sub threshold swing (SS) and transconductance (gm). The strained JLTFET, also demonstrates capability for low-operating-voltage application due to low threshold voltage ($V_t$).A short review of your proposed method, its contribution, and results should be provided here.

## REFERENCES

[1] W. Y. Choi, B. G. Park, J. D. Lee, and T. J. K. Liu, **"Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec,"** *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, 2007.

[2] M. Rahimian and M. Fathipour, **"N-P-N Bipolar Action in Junctionless Nanowire TFET : Physical Operation of a Modified Current Mechanism for Low Power Applications,"** no. August, pp. 1–24, 2016.

[3] D. B. Abdi and M. J. Kumar, **"Controlling ambipolar current in tunneling FETs using overlapping gate-on-drain,"** *IEEE J. Electron Devices Soc.*, vol. 2, no. 6, pp. 187–190, 2014.

[4] K. K. K and B. R. N, "Sub-threshold Leakage Current Reduction Using Variable Gate Oxide Thickness ( VGOT ) MOSFET," vol. 2, no. 2, pp. 24–28, 2013.

[5] P. K. Asthana, B. Ghosh, Y. Goswami, B. Mukund, and M. Tripathi, **"High-Speed and Low-Power Ultradeep-Submicrometer III – V Heterojunctionless,"** *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 479–486, 2014.

[6] S. B. Rahi, P. Asthana, and S. Gupta, **"Heterogate junctionless tunnel field-effect transistor: future of low-power devices,"** *J. Comput. Electron.*, vol. 16, no. 1, pp. 30–38, 2017.

[7] S. B. Rahi, B. Ghosh, and P. Asthana, **"A simulation-based proposed high-k heterostructure AlGaAs/Si junctionless n-type tunnel FET,"** *J. Semicond.*, vol. 35, no. 11, 2014.

[8] X. Liu *et al.*, **"Study of novel junctionless Ge n-Tunneling Field-Effect Transistors with lightly doped drain (LDD) region,"** *Superlattices Microstruct.*, vol. 102, no. 2, pp. 7–16, 2017.

[9] A. C. Seabaugh and Q. Zhang, **"Low-voltage tunnel transistors for beyond CMOS logic,"** *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, 2010.

[10] K. Boucart and A. M. Ionescu, **"Double-gate tunnel FET with high-K gate dielectric,"** *IEEE Trans. Electron Devices*, vol. 54, no. 7, pp. 1725–1733, 2007.

[11] H. Aghandeh, S. Ali, and S. Ziabari, **"Gate engineered heterostructure junctionless TFET with Gaussian doping pro fi le for ambipolar suppression and electrical performance improvement,"** *Superlattices Microstruct.*, pp. 1–12, 2017.

[12] R. Molaei Imen Abadi and S. A. Sedigh Ziabari,

**"Improved performance of nanoscale junctionless tunnel field-effect transistor based on gate engineering approach,"** *Appl. Phys. A Mater. Sci. Process.*, vol. 122, no. 11, pp. 1–9, 2016.

[13] Y. Goswami, P. Asthana, and B. Ghosh, **"Nanoscale III–V on Si-based junctionless tunnel transistor for EHF band applications,"** *J. Semicond.*, vol. 38, no. 5, p. 054002, 2017.

[14] J. Schulze *et al.*, **"Vertical Ge and GeSn heterojunction gate-all-around tunneling field effect transistors,"** *Solid. State. Electron.*, vol. 110, pp. 59–64, 2015.

[15] H. D. Tsague and B. Twala, **"Simulation and parameter optimization of polysilicon gate biaxial strained silicon MOSFETs,"** *2015 5th Int. Conf. Digit. Inf. Process. Commun. ICDIPC 2015*, pp. 38–43, 2015.

[16] M. Najmzadeh, L. De Michielis, D. Bouvet, P. Dobrosz, S. Olsen, and A. M. Ionescu, **"Silicon nanowires with lateral uniaxial tensile stress profiles for high electron mobility gate-all-around MOSFETs,"** *Microelectron. Eng.*, vol. 87, no. 5–8, pp. 1561–1565, 2010.

[17] S. Takagi, M. Kim, M. Noguchi, S. M. Ji, K. Nishi, and M. Takenaka, **"III-V and Ge/strained SOI tunneling FET technologies for low power LSIs,"** *Dig. Tech. Pap. - Symp. VLSI Technol.*, vol. 2015–Augus, no. 2011, pp. T22–T23, 2015.

[18] S. Takagi and M. Takenaka, **"Ge/III-V MOS device technologies for low power integrated systems,"** *Eur. Solid-State Device Res. Conf.*, vol. 2015–Novem, pp. 20–25, 2015.

[19] M. K. Moghadam and S. E. Hosseini, **"Investigation of a SiGe Tunnel FET : Comparison to Si and Ge TFETs,"** *J. Electr. Syst. Signals*, vol. 2, no. 1, pp. 21–25, 2014.

[20] M. Visciarelli, E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, **"Impact of Strain on Tunneling Current and Threshold Voltage in III-V Nanowire TFETs,"** *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 560–563, 2016.

[21] T. A. Langdo *et al.*, **"SiGe-free strained Si on insulator by wafer bonding and layer transfer,"** *Appl. Phys. Lett.*, vol. 82, no. 24, pp. 4256–4258, 2003.

[22] C. Grillet, D. Logoteta, A. Cresti, and M. G. Pala, "**Assessment of the Electrical Performance of Short Channel InAs and Strained Si Nanowire FETs,"** *IEEE Trans. Electron Devices*, vol. 64, no. 5, pp. 2425–2431, 2017.

[23] S. Saurabh and M. J. K. Ã, **"Impact of Strain on Drain Current and Threshold Voltage of Nanoscale Double Gate Tunnel Field Effect Transistor : Theoretical Investigation and Analysis Impact of Strain on Drain Current and Threshold Voltage of Nanoscale Double Gate Tunnel Field Effect T,"** vol. 064503, no. 064503, pp. 1–35.

[24] Q. T. Zhao, J. M. Hartmann, and S. Mantl, **"An Improved Si Tunnel Field Effect Transistor With a Buried Strained Si(1-x)Ge(x),"** *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1480–1482, 2011.

[25] M. Kumar and S. Jit, **"Effects of Electrostatically Doped Source/Drain and Ferroelectric Gate Oxide on Subthreshold Swing and Impact Ionization Rate of Strained-Si-on-Insulator Tunnel Field-Effect Transistors,"** *IEEE Trans. Nanotechnol.*, vol. 14, no. 4, pp. 597–599, 2015.

[26] Q. T. Zhao *et al.*, **"Strained Si and SiGe nanowire tunnel FETs for logic and analog applications,"** *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 103–114, 2015.

[27] M. J. Kumar and S. Saurabh, **"Tunnel Field Effect Transistor (TFET) with strained silicon thinfilm body for enhanced drain current and pragmatic threshold voltage,"** *2008 NSTI Nanotechnol. Conf. Trade Show, NSTI Nanotech 2008 Jt. Meet. Nanotechnol. 2008, June 1, 2008 - June 5, 2008*, vol. 3, pp. 28–30, 2008.

[28] D. K. Dash, P. Saha, and S. K. Sarkar, **"Analytical modeling of asymmetric hetero-dielectric engineered dual-material DG-TFET,"** *J. Comput. Electron.*, vol. 17, no. 1, pp. 181–191, Mar. 2018.

[29] S. Kumar and B. Raj, **"Compact channel potential analytical modeling of DG-TFET based on Evanescent-mode approach,"** *J. Comput. Electron.*, vol. 14, no. 3, pp. 820–827, Sep. 2015.

[30] S. Kumar, E. Goel, K. Singh, B. Singh, M. Kumar, and S. Jit, **"A Compact 2-D Analytical Model for Electrical Characteristics of Double-Gate Tunnel Field-Effect Transistors with a SiO2/High-k Stacked Gate-Oxide Structure,"** *IEEE Trans. Electron Devices*, vol. 63, no. 8, pp. 3291–3299, Aug. 2016.

[31] R. Vishnoi and M. J. Kumar, **"2-D analytical model for the threshold voltage of a tunneling FET with localized charges,"** *IEEE Trans. Electron Devices*, vol. 61, no. 9, pp. 3054–3059, Sep. 2014.

[32] P. Palestri and C. Press, *Nanoscale MOS transistors: Semi-classical modeling and applications*. Cambridge University Press, 2014.

[33] M. J. Kumar, V. Venkataraman, and S. Nawal, **"Analytical drain current model of nanoscale strained-Si/SiGe MOSFETs for analog circuit simulation,"** in *Proceedings of the IEEE International Conference on VLSI Design*, 2007, pp. 189–194.

[34] S. Sharma, "**An Analysis of Device Characteristics of Strained N-Channel MOSFET,"** vol. 3, no. 8, pp. 87–90, 2016.

[35] P. Pandey, R. Vishnoi, and M. J. Kumar, "A full-range dual material gate tunnel field effect transistor drain current model considering both source and drain depletion region band-to-band tunneling," *J. Comput. Electron.*, vol. 14, no. 1, pp. 280–287, Mar. 2015.

[36] J. S. Lim, S. E. Thompson, and J. G. Fossum, **"Comparison of threshold-voltage shifts for uniaxial and biaxial tensile-stressed n-MOSFETs,"** *IEEE Electron Device Lett.*, vol. 25, no. 11, pp. 731–733, Nov. 2004.

[37] T. Numata, T. Mizuno, T. Tezuka, J. Koga, and S. I. Takagi, **"Control of threshold-voltage and short-channel effects in ultrathin strained-SOI CMOS**

**devices,"** *IEEE Trans. Electron Devices*, vol. 52, no. 8, pp. 1780–1786, Aug. 2005.

[38] R. Molaei Imen Abadi *et al.*, **"An Improved Si Tunnel Field Effect Transistor With a Buried Strained Si(1-x)Ge(x),"** *Microelectron. Eng.*, vol. 162, no. November, pp. 1480–1482, 2011.