An Ultra-broadband and Low Noise distributed Drain Mixer with Filtering Structure

Masoume Mahmoudi Meimand¹, Ahmad Hakimi²

1- Department of Electrical and Computer Engineering, Graduate University of Advance Technology, Kerman, Iran Email[: M.mahmoudi@student.kgut.ac.ir](mailto:M.mahmoudi@student.kgut.ac.ir)

2- Department of Electrical Engineering, Shahid Bahonar University of Kerman, Kerman, Iran Email: Hakimi@mail.uk.ac.ir

Received: March 2014 Revised: June 2014 Accepted: July 2014

ABSTRACT

This paper presents a 6 to 64 GHz passive distributed drain mixer implemented by using a standard 0.13 um CMOS process. To improve the bandwidth, low conversion loss and low noise figure, filtering structures is utilized for wideband matching. Both Chebyshev and Butterworth filters are used instead of the classical constant-k sections of the conventional DA in order to form respectively the gate and drain transmission lines. This mixer consumes zero dc power and exhibits a conversion loss of 4.9-7.9 dB and noise figure (DSB) of 6.8-8.1 dB from 6 to 64 GHz.

KEYWORDS: CMOS, Distributed Mixer, Drain Mixer, Chebyshev Filter, Butterworth Filter.

1. INTRODUCTION

Recently, the demand of high speed wireless communication is significantly increased due to the popularity of portable digital devices. For the modern multiband receiver front-end, a broadband downconverted mixer plays an important role and bandwidth and conversion gain are the important specifications of these mixers. To achieve better aliquot bandwidth, distributed topology is a good candidate with the characteristics of traveling-wave circuits [1].

Active distributed mixers have been reported using CMOS technology [2], [3]. For broad bandwidth, the active distributed mixers consume additional dc power as the number of stages increases, in [4] a complementary LO switching pair is proposed to replace the original upper LO stage. The distributed active mixer achieves relatively broad operation bandwidths, low CLs but the noise figure is high. In [5] to the distributed amplifier, a good second harmonic suppression and a broadband passive APDP were employed in this proposed sub-harmonic mixer to realize ultra-broadband, low conversion loss, good flatness but noise figure is relatively high. Alternatively, using a passive mixer as a unit cell of the distributed mixer is suitable for wideband and lowpower system applications [6]–[7]. Although a passive mixer has zero dc power consumption, the high local oscillator (LO) power is a drawback [8]. In [9] for the broad bandwidth and flat conversion loss, a broadband impedance-transforming Marchand balun network is analyzed to design the wideband LO matching, but

mixer exhibits a measured conversion loss of 7.5 ± 1.5 dB and noise figure(SSB) of 13.2 to 17.2 dB from 33 to 58 GHz.

To solve the high conversion loss of passive distributed drain-pumped mixer, filtering structure is proposed. The proposed distributed mixer achieves broad operation bandwidth, low conversion loss and low noise figure.

Section 2 discusses the filter design method. In Section 3, circuit design considerations are presented. Section 4 shows simulation results. Finally, a conclusion is presented in Section 5.

2. FILTER DESIGN METHOD

In this method we use the benefits of the Chebyshev and Butterworth filters, for instance the desirable characteristic of Butterworth and chebyshev filters are flatness and fast roll-off, respectively, that can be used in design of DA circuit. This method will absorb the input and output parasitic capacitance of the transistors as in the conventional constant-k networks.

The passive elements of Butterworth and chebyshev filters are scaled from the normalized parameters of the corresponding LPF as depicted in Fig. 1. The inductance and capacitance values can be unnormalized from the parameters by the following equations:

$$
g_k = \begin{cases} a_k : k = 1,3,5,7 \\ b_k : k = 2,4,6 \end{cases}
$$
 (1)

Majlesi Journal of Telecommunication Devices Vol. 3, No. 3, September 2014

$$
C_k = \frac{bk}{2 \pi \cdot Z_0 \cdot f_c} \tag{2}
$$

$$
L_k = \frac{Z0 \cdot ak}{2 \cdot \pi \cdot f_c} \tag{3}
$$

Where C_k and L_k are the real inductance and capacitance values, b_k and a_k are the normalized inductance and capacitance values $Z_0 = 50\Omega$ is the characteristic impedance, f_c is the filter cut-off frequency.

In Table 1, the values of normalized the Butterworth and Chebyshev filters are shown. The values of unnormalized the Butterworth and Chebyshev filters are shown in Table 2.

3. CIRCUIT DESIGN

In this section a passive distributed drain mixer with filtering structure is proposed. This broadband passive distributed drain mixer is simulated by Agilent ADS software using 0.13-μm CMOS process.

3.1. The Proposed Mixer Circuit

The schematic of proposed distributed drain mixer is shown in Fig. 2. To achieve wide operation band Width and low noise figure filtering structures is used.

To avoid dc power consumes at the termination resistor of gate line, a capacitor $(C_5=1pF)$ is added between the termination resistor and ground. Because of this capacitor is not a perfect short circuit for all frequency, so it will degrade RF return loss [1]. Given that we used distributed drain-pumped topology, a sufficient LO input power is required to drive these devices.

Filter Type	Butterworth	Chebyshev		
$g_0 = g_8$				
g ₁	0.4450	1.7372		
g_2	1.2470	1.2583		
g_3	1.8019	2.6381		
g_4	2.0000	1.3444		
g_5	1.8019	2.6381		
g_6	1.2470	1.2583		
g_7	0.4450	1.7372		

Table 1. Filter normalized parameters [10].

Table 2. Filter unnormalized parameters.	
--	--

л.			
Butterworth	Chebyshev		
0.044nH	0.1728nH		
0.0496pF	0.05 PF		
0.179nH	0.2624nH		
0.0796pF	0.0535pF		
0.179nH	0.2624nH		
0.0496pF	0.05 PF		
0.044nH	0.1728nH		

An LO power of 10 dBm is determined as an agreement of LO power and conversion loss.

To flatten the conversion loss at low frequency, the resistor R₁=50 Ω is selected. Two capacitors C₁=0.8pF and $C_3=1pF$ are the dc-blocking capacitors of the RF and LO ports, respectively [1].

With the quality factor $Q=10$ the series impedance of the inductors are calculated, and the transistors width are 30-um (W=30um).

4. EXPERIMENTAL RESULTS

The simulated conversion losses of this mixer are shown in Fig. 3. This exhibits a wide and flat conversion loss of -4.9-7.9 dB from 6 to 64GHz with an LO power of 10 dBm. The simulation results of RF return loss are shown in Fig. 4.

Fig. 2. Schematic of the proposed mixer circuit.

Fig.3. Simulated CL as a function of RF Frequency.

Majlesi Journal of Telecommunication Devices Vol. 3, No. 3, September 2014

Table 5: Comparison of the wideband maxers									
		Bandwidth	Conversion	Noise Figure	LO Power	DC			
	Topology	(GHz)	Gain (dB)	(dB)	(dBm)	$\mathsf{Consumption}(mW)$			
[4]	0.18 um CMOS	5-45	$-11 - -13.2$	$7.6 - 10.2$		1.4			
$[5]$	90 nm CMOS	33-103	$-0.52 - -3.35$	$7.9 - 10.3$	10	24.5			
[8]	0.18 um CMOS	$2 - 40$	$-5+1$	$10.7 - 12.6(SSB)$	12				
$[9]$	90 nm CMOS	$33 - 58$	$-6- -9$	$13.2 - 17.2(SSB)$	10				
This work	0.13 um CMOS	$6 - 64$	$-4.9 - -7.9$	$6.8 - 8.1$	10				

Table 3. Comparison of the wideband mixers

The LO-to-RF and LO-to-IF isolations are shown in Figs. 5. The LO-to-RF isolation is overcome by the parasitic capacitance of C_{GD} of the transistor. The simulated NF as a function of RF is shown in Fig. 6. Fig.7 shows the IF output power and conversion loss versus RF input power.

The simulation results of conversion loss versus LO input power is shown in Fig. 8. It is observed that the low conversion loss of this mixer depends on a sufficient LO power. The simulation results of conversion loss versus dc gate–source voltage V_{GS} is shown in Fig. 9.

The NF simulation is done by applying the worst case mismatches, to all resistors, capacitors and inductors. These mismatches are calculated based on

Fig. 4. Simulated results of the input return loss.

Fig. 5. Simulated LO-to-RF, and LO-to-IF isolation.

the process information and are verified by Monte Carlo simulations. The Monte Carlo simulation of NF of the mixer has been performed to examine the proposed technique against mismatches. Based on the simulation results shown in Fig. 10, the mean value of the NF of the mixer with NF decrease technique is 7.3 dB.

Table 3 summarizes the performances of recently published CMOS wideband mixers.

5. CONCLUSION

In this paper, a low-power, low-loss, low noise figure and wideband passive distributed drain-pumped mixer was proposed. High bandwidth, low conversion loss and low noise figure have been guaranteed by

Fig. 6. Simulated NF as a function of RF frequency.

Fig. 7. The IF output power and conversion loss versus RF input power.

Majlesi Journal of Telecommunication Devices Vol. 3, No. 3, September 2014

Number of Monte Carlo Run **Fig. 10.** NF Monte Carlo simulation of the proposed mixer.

using the filter structure in the gate and drain transmission lines. The mixer operates from 6 to 64 GHz with a conversion loss of 4.9-7.9 dB and a DSB NF of 6.8 to 8.1 dB.

REFERENCES

[1] H. Y. Yang, J. H. Tsai, C. H. Wang, C. S. Lin, W. L. Lin, K. Y. Lin, T. W. HuangH, and Wang, **"Design and analysis of a 0.8–77.5-GHz ultra-broadband distributed drain mixer using 0.13-um CMOS**

technology, " *IEEE Trans. Microw. Theory Tech,* Vol. 57, No. 3, pp. 562–572, Mar. 2009.

- [2] C.-R. Wu, H.-H. Hsieh, and L.-H. Lu, **"An ultrawideband distributed active mixer MMIC in 0.18-um CMOS technology, "** *IEEE Trans. Microw. Theory Tech.,* Vol. 55, No. 4, pp. 625–632, Apr. 2007.
- [3] N. Garg, L. B. Lok, I. D. Robertson, M. Chongcheawchamnan, and A. Worapishet, **"1 to 20 GHz CMOS distributed mixer using asymmetric coplanar strip transmission lines, "** *in Proc. Radio Freq. Integr. Circuits Symp.,* pp. 217–220, Jun. 2006.
- [4] Y-Sh. Lin, Ch-L. Lu, and Y-H. Wang, **"A 5 to 45 GHz Distributed Mixer With Cascoded Complementary Switching Pairs, "** *IEEE Microw. Wireless Compon. Lett,* Vol. 23, No. 9, pp. 495–497, Sep. 2013.
- [5] Sh-H. Hung, K-W. Cheng, and Y-H. Wang, **"An Ultra-Broadband Subharmonic Mixer With Distributed Amplifier Using 90-nm CMOS Technology, "** *IEEE Trans. Microw. Theory Tech.,* Vol. 61, No. 10, pp. 3650– 3657, Oct. 2013.
- [6] F. Ellinger, **"26.5–30-GHz resistive mixer in 90-nm VLSI SOI CMOS technology with high linearity for WLAN,** *" IEEE Trans. Microw. Theory Tech.,* Vol. 53, No. 8, pp. 2559–2565, Aug. 2005.
- [7] F. Ellinger, L. C. Rodoni, G. Sialm, C. Kromer, G. von Buren, M. L. Schmatz, C. Menolfi, T. Toifl, T. Morf, M. Kossel, and H. Jackel**, "30–40-GHz drain-pumped passive-mixer MMIC fabricated on VLSI SOI CMOS technology, "** *IEEE Trans. Microw. Theory Tech.*, Vol. 52, No. 5, pp. 1382–1391, May 2004.
- [8] B. Nie, J. Zhou, and K. Chen, **"Design and Analysis of an Ultra wide-Band Distributed Drain-Pumped Mixer Using 0.18um CMOS Technology, "** *in Microw.& Elec, primeAsia,* pp 29-32 , 2009.
- [9] H. Y. Yang, J. H. Tsai, T. W. Huang, and H. Wang, **"Analysis of a new 33–58-GHz double-balanced drain mixer in 90-nm CMOS technology,** *" IEEE Tran. Microw. Theory Tech.,* Vol. 60, No. 4, pp. 1057–1068, Apr. 2012.
- [10] Y. Zhu, and H. Wu, **"Distributed Amplifiers with Non-Uniform Filtering Structures, "** *IEEE Radio Freq. Integr. Circuits (RFIC) Symposium*, pp. 367-370, Jun. 2006.