Design of 0.4 V operational amplifier using low-power techniques

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ABSTRACT:

In this paper a low-power low-voltage CMOS operational amplifier (op amp) using sub-threshold region of MOSFET for bio-medical instrumentation operating with a 0.4 V supply is described. A two stage operational amplifier is designed and simulated using 0.18 μm CMOS technology. Two types of low-power low-voltage design techniques (a) bulk-driven (b) dynamic threshold voltage MOSFET (DTMOS) are used. With bulk-driven technique, the open loop gain is 69.88 dB, the unity gain-bandwidth (UGBW) is 87.1 kHz, CMRR obtained is 83 dB and phase margin is 88.78 degree with 10pF load. The power consumption is 1.8 μW. With DTMOS technique, the open loop gain is 83.31 dB, the unity gain-bandwidth is 758.6 kHz, CMRR obtained is 157.1 dB and phase margin is 71.5 degree with 10pF load. The power consumption is 1.8 μW. DTMOS technique provides high unity gain-bandwidth and high open loop gain as compared to bulk-driven technique.

KEYWORDS: Bulk-driven, DTMOS, Low-power low-voltage, Op amp, Operational amplifier, Sub-threshold.

1. INTRODUCTION

In the past few years with the rapid growth of market for portable devices such as cell phones, portable computers and medical electronic implant devices, design of analog integrated circuits at low-power with high performance has become an extremely important issue. Low-power op amp can be used as bio-potential amplifier. The basic purpose of a bio-potential amplifier is to amplify and filter the extremely weak bio-potential signals. The challenges of designing a bio-potential amplifier for bio-medical devices are high CMRR, low-noise for high signal quality and low-power dissipation. In bio-medical field low-power op amp require small bandwidth.

Reduction of threshold voltage is necessary for low-power low-voltage operation, so various techniques have been proposed for low-power low-voltage analog integrated circuits design. A MOSFET can be operated at a lower-voltage by forward biasing the source-bulk junction (bulk-driven technique). This approach has been used to design a low-power low-voltage CMOS operational amplifier, but with increasing forward body-bias, the leakage current increases significantly. The DTMOS technique in 1994 (Assaderaghi et al) is proposed to overcome the drawback in a forward-biased MOSFET [1]-[3]. This technique can be used in connection with the back-gate forward-bias technique in designing low-power low-voltage analog, digital and mixed signal CMOS integrated circuits.

Several papers have been focused on design of CMOS operational amplifier and operational transconductance amplifier (OTA) based on DTMOS and bulk-driven techniques. (a) DTMOS technique, in [4]-[7] the authors presented a novel class AB op amp for low-voltage (1 V) applications. In [8] the authors proposed an ultra-low-voltage ultra-low-power operational transconductance for biomedical applications. In [9] the authors presented a 0.8 V class-AB linear OTA for high-frequency applications. In [10] a novel input stage for low-voltage low-power and low-noise operational amplifier has been described. (b) bulk-driven technique in [11] 0.5 V ultra-low-power OTA is presented. In [12] a novel 0.9 V OTA with dual bulk-driven input stage is introduced. In [13] 1 V low-power op amp is proposed.

The organization of this paper is as follows. In Section 2, the DTMOS and bulk-driven techniques are presented. In section 3, the sub-threshold operation is discussed. The structure of proposed op amp is described in Section 4. The simulations results are provided in Section 5 and finally the conclusion is given.

2. LOW-POWER TECHNIQUES

An effective method for reducing power consumption is reduction the power supply voltage. A constraint to implementing digital and analog circuits at low-voltage is the threshold voltage.

2.1. Dynamic Threshold voltage MOSFET

DTMOS technique is the best idea for reduction threshold voltage. The DTMOS technique reduces the transistor off-state leakage current and also reduces the threshold voltage during on-state ($V_{BS} > 0$) according to below equation [14]:

$$V_{th} = V_{th0} + \lambda \left(\sqrt{|2\varphi_f - V_{BS}|} - \sqrt{|2\varphi_f|} \right) \qquad (1)$$

Where V_{BS} is the source-bulk voltage, V_{th0} the threshold voltage for $V_{BS} = 0$, λ is body effect factor with an approximate value between 0.3 to 0.4 $\sqrt{V}$, and φ_f is Fermi potential with a typical value in the range of 0.3- 0.4 V [14].

In DTMOS technique, the bulk is tied to its own gate as shown in Fig. 1.
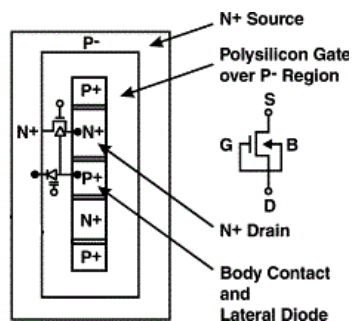

Fig. 1. Dynamic threshold MOSFET device [15].

2.2. Bulk-driven

Bulk-driven technique was first proposed in 1987 (Guzinski et al) to overcome the threshold voltage [16]. The operation of a bulk-driven MOSFET is similar to a JFET as shown in Fig. 2.
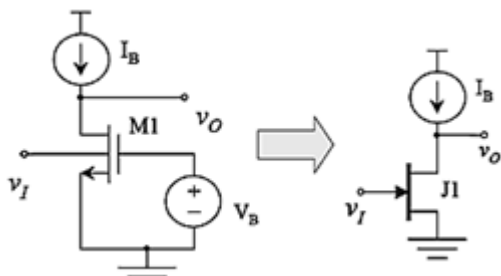

Fig. 2. Bulk-driven MOS transistor and its equivalent JFET.

There are some drawbacks between bulk-driven devices compared to gate-driven devices. (1) Because

of smaller transconductance, which results in higher input-referred noise. (2) The ground-connected gate terminals of the input pair will pick up any noise generated by the negative power supply. Therefore, the power supply rejection has poor performance. (3) Because of smaller control capacitance of the depletion layer, larger parasitic capacitance to the substrate, which results in lower f_T [17].

$$f_{T,Bulk-driven} = \frac{g_{mb}}{2\pi(C_{SB} + C_{DB} + C_{B-sub})} \qquad (2)$$

$$f_{T,Gate-driven} = \frac{g_{mb}}{2\pi C_{GS}} \qquad (3)$$

3. SUB-THRESHOLD OPERATION

Operation of the MOS device in sub-threshold region is very important when low-power circuits are desired. When the V_{GS} in the MOS transistor is less than the threshold voltage (V_{th}), the MOSFET works in sub-threshold region. The drain current I_D of a MOS transistor in sub-threshold region is based on the channel diffusion current and can be given by (4), when referred to source voltage [8].

$$I_D = I_S \left(\frac{W}{L}\right) exp \left(q \frac{V_{GS} - V_{th}}{nKT}\right) \left[1 - exp\left(-q \frac{V_{DS}}{KT}\right)\right] \qquad (4)$$

Where I_S is the characteristic current, T is the absolute temperature, n is the slope factor, K is the Boltzmann constant and q is the charge of the electron or hole.

If $V_{DS} \geq 3KT/q$ then the transistor will be saturated in sub-threshold region. The transconductance g_m can be found as presented in (5), which is a function of current Ids and factor nKT/q [8].

$$g_m = q \frac{I_D}{nKT} \qquad (5)$$

There is linear relationship between transconductance and current. Also transconductance is independent of device geometry. But in strong inversion relationship between transconductance and current is square law and also function of device geometry.

4. OPERATIONAL AMOLIFIER DESIGN

Fig. 3(a) shows the schematic of a two stage low-power low-voltage operational amplifier working at sub-threshold region. Fig. 3(b) shows one typical application of a bulk-driven NMOS as in a differential pair and Fig. 3(c) shows one typical application of a DTMOS NMOS as in a differential pair.

Fig. 3(a) combines a fully differential pair with a current source load and a differential pair with a current mirror load. The active current source M3 and M4 can source the maximum current for the input pair to reduce

thermal noise. Also large sizes are used for the input pair M1, M2 to reduce noise level.

(a)

(b)
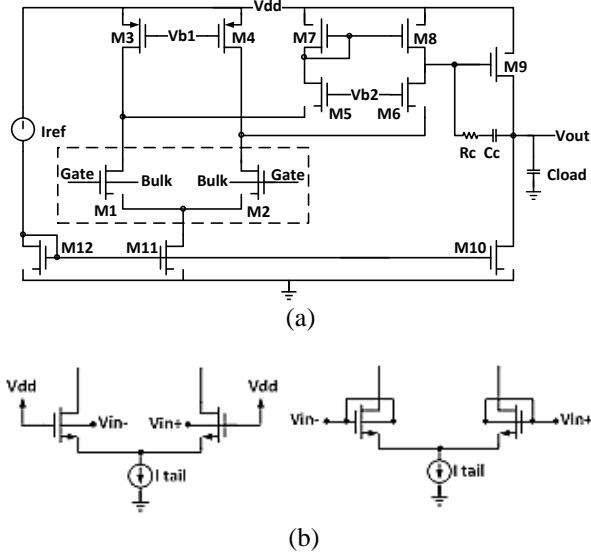
Fig. 3. (a) Schematic of the op amp circuit, (b) Bulk-driven NMOS differential pair, (c) DTMOS NMOS differential pair.

The current mirror M7 and M8 combine with the transconductance of the input pair to define the DC gain. A cascode stage, M5 and M6 can increase the bandwidth and gain of the amplifier. The common source configuration is chosen for the output stage of the operational amplifier. Such a stage can provide about 20-30 dB of gain. A Miller compensation scheme is chosen to achieve desirable phase margin.

4.1. DC gain

The small-signal DC gain of the proposed op amp is given by:

$$A_0 = (g_{m2} + g_{mb2}) * \cdots$$
$$* ([(g_{m6} + g_{mb6})r_{o6}(r_{o2} \parallel r_{o4})] \parallel r_{o8}) * \cdots \quad (6)$$
$$* g_{m9}(r_{o9} \parallel r_{o10})$$

While the transconductance g_{mb} can be calculated as given in (7), [14]:

$$g_{mb} = \frac{\lambda}{2\sqrt{2\varphi_f + V_{sb}}} g_m = \eta g_m \quad (7)$$

The transconductance g_{mb} varies from 20% to 30% of g_m for the same transistor in a CMOS process [14].

4.2. AC analysis

Small-signal analysis of the circuit in Fig. 3(a), results in the following equation (ignoring some smaller parameters such as C_1 and C_2):

$$\frac{V_{out}}{V_{in}} = \cdots$$
$$= \frac{[(g)_{m2} + g_{mb2})g_{m9}R_2R_3 - sg_{m2}R_2R_3C_c(1 - \varepsilon}{1 + s(R_cC_c + R_3C_3 + g_{m9}R_2R_3C_c) + s^2R_cR_2} \quad (8)$$

Where

$$C_1 = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{sb6} + C_g$$
$$C_2 = C_{db6} + C_{gd6} + C_{db8} + C_{gd8} + C_{gs9} + C_g$$
$$C_3 = C_{Load} + C_{db9} + C_{gd9} + C_{db10} + C_{gd10}$$
$$R_1 = r_{o2} \parallel r_{o4} \quad (9)$$
$$R_2 = r_{o8} \parallel [r_{o6}(1 + (g_{m6} + g_{mb6})(r_{o2} \parallel r_{o4}$$
$$R_3 = r_{o9} \parallel r_{o10}$$

C_c and R_c are the compensation capacitor and zero-nulling resistor respectively.

With the supposition that the second pole is far larger than the dominant pole, the dominant pole of equation (8) can be approximated by:

$$P_1 \approx -\frac{1}{g_{m9}R_2R_3C_c} \quad (10)$$

and the second dominant pole is:

$$P_2 \approx -\frac{g_{m9}R_2}{R_cC_c} \quad (11)$$

Also the zero is:

$$Z = \frac{g_{m9}}{(1 - g_{m9}R_c)C_c} \quad (12)$$

For unity gain-bandwidth stability, the magnitude of the second dominant pole should be greater than the UGB, therefore:

$$C_c > \frac{[(g)_{m2} + g_{mb2})R_cC_3}{g_{m9}R_2} \quad (13)$$

According to Equations (11) and (12), we can find that the R_c can control the zero and second dominant pole positions and therefore change the phase margin. If R_c is chosen close to $1/g_{m9}$, then P_2 is maximized and stability is achieved with a minimum C_c.

4.3. Noise analysis

The input-referred noise (includes thermal noise and flicker noise) of the proposed op amp is described as:

$$V_n^2(f) = 2\left[\frac{K_{fn}}{C_{ox}W_2L_2f} + \frac{4KT\gamma}{(g_{m2} + g_{mb2})}\right] + \cdots$$
$$+ 2\left[\frac{K_{fp}}{C_{ox}W_4L_4f} + \frac{4KT\gamma}{g_{m4}}\right]\left(\frac{g_{m4}}{g_{m2} + g_{mb2}}\right)^2 + \cdots$$
$$+ 2\left[\frac{K_{fp}}{C_{ox}W_8L_8f} + \frac{4KT\gamma}{g_{m8}}\right]\left(\frac{g_{m8}}{g_{m2} + g_{mb2}}\right)^2 \quad (14)$$

Where C_{ox} is capacitance per unit area of the gate oxide, W and L are the channel width and length respectively, K_{fn} is NMOS flicker noise coefficient, K_{fp} is PMOS flicker noise coefficient. The derived coefficient γ is equal 2/3 for long-channel transistors and may need to be replaced by a larger value for submicron MOSFETs. It also varies to some extent with the drain-source voltage [14]. The noise contribution of cascode stage M5, M6, output stage M9, M10 and current bias transistor M0 is negligible.

5. SIMULATION RESULTS

The proposed op amp has been simulated with HSPICE in a 0.18 μm CMOS standard technology under 10pF load. Typical Op amp performance such as power consumption, open loop gain, phase margin, unity-gain bandwidth, noise, power supply rejection ratio (PSRR) and common mode signal rejection ratio (CMRR), etc. have been simulated at TT corner for both techniques. Simulation results for AC analysis for gain and phase plot vs. frequency is shown in Fig. 4.
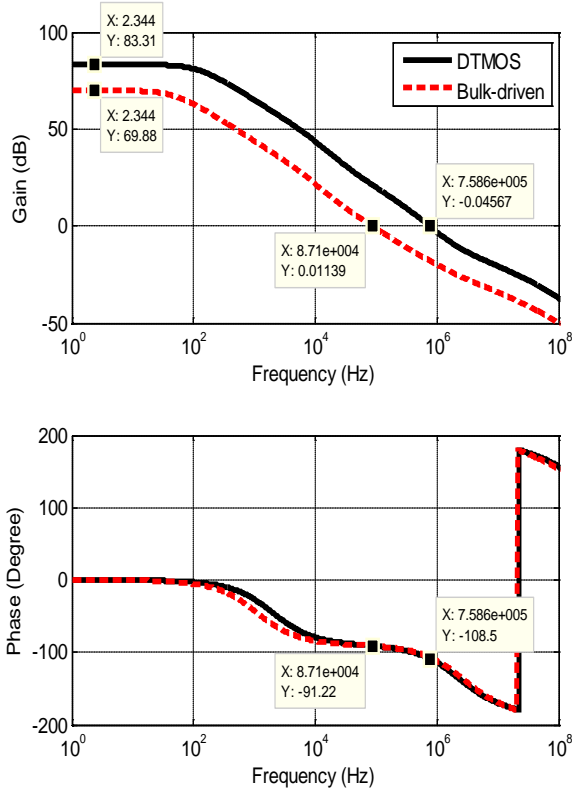

Fig. 4. Simulated open loop gain and phase margin.

With DTMOS technique, the op amp has an open loop gain of 83.31 dB, a unity gain-bandwidth of 758.6 kHz and a phase margin of 71.5 degree. With bulk driven technique, the op amp has an open loop gain of 69.88 dB, a unity gain-bandwidth of 87.1 kHz and a phase margin of 88.78 degree. The presented

topology employing sub-threshold transistors is capable of working at 0.4 V of power supply and consuming only 1.8 μW.

The simulated input-referred voltage noise performance of the circuit is shown in Fig. 5. With DTMOS technique the input-referred noise is 0.4284 μV/√Hz at 1 Hz and 1.355 nV/√Hz at 100 Hz and with bulk-driven technique the input-referred noise is 1.128 μV/√Hz at 1 Hz and 3.547 nV/√Hz at 100 Hz.
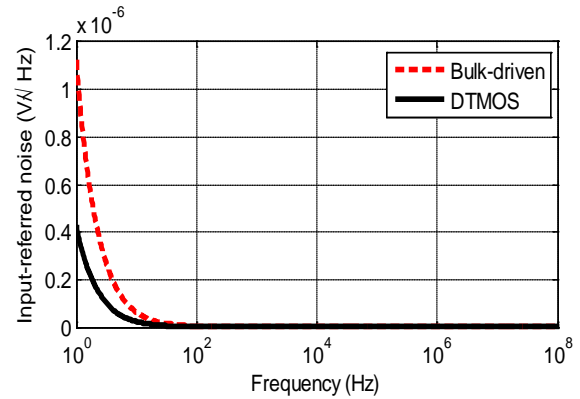

Fig. 5. Simulated input-referred noise.

Table 1 shows a comparison with other low-voltage low-power operational amplifiers. To evaluate this work a figure of merit (FoM) is defined as [8]:

$$FoM = \cdots = \frac{Gain * UGBW}{Power\ supply * Power\ consumption} \quad (15)$$

6. CONCLUSION

The design of a low-power low-voltage, high performance two stage operational amplifier circuit in a 0.18 μm CMOS process is reported in this paper. To design low-power low-voltage op amp, first the bulk-driven technique using sub-threshold region of MOSFET is used. The low gain and unity-gain bandwidth disadvantages of the bulk-driven technique are circumvented by employing DTMOS technique. The simulation results show that the open loop gain of the presented amplifier with bulk-driven technique is equal to 69.88 dB while achieving unity-gain bandwidth of 87.1 KHz. Also with DTMOS technique open loop gain is 83.31 dB and unity-gain bandwidth is 758.6 kHz that much higher compared to bulk-driven technique. The total power consumption of the op amp is as low as 1.8 μW.

Table 1. Comparison between operational amplifiers.

	DTMOS	Bulk-driven	[5]	[8]	[18]
Technology (µm)	0.18	0.18	0.18	0.18	0.18
Power supply (V)	0.4	0.4	1	0.4	0.8
Power consumption (µW)	1.8	1.8	33.1	0.386	100
Gain (dB)	83.31	69.88	60	91	56
Phase margin	71.5º	88.78º	62º	66º	45º
UGBW (kHz)	758.6	87.1	2.73	0.111	3.2
CMRR (dB)	105	83	100	106	80
PSRR (dB)	100.1 @ 100 Hz	81.5 @ 100 Hz	N/A	N/A	88 @ 10 kHz
Slew Rate (V/µs)	10.6	9.2	N/A	0.022	N/A
Output voltage swing (V)	0.37	0.32	0.8	N/A	N/A
Input-referred noise $\left(\frac{nV}{\sqrt{Hz}} \right)$	1.355 @ 100 Hz	3.547 @ 100 Hz	107 @ 1 kHz	10 @ 10 mHz	408 @ 10 kHz
C_{Load} **(pF)**	10	10	5, 10 kΩ	15	20

REFERENCES

[1] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. K. Ko, and C. Hu, "**A dynamic threshold voltage MOSFET (DTMOS) for ultra-low voltage operation**," *International Electron Devices Meeting, Technical Digest*, pp. 809–812, 1994.

[2] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P.K. Ko, Hu. Chenming, "**Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI**," *IEEE Transaction on Electron Device*, Vol. 44, No. 3, pp. 414-422, 1997.

[3] F. Assaderaghi, "**DTMOS: Its derivatives and variations, and their potential applications**," *International Conference on Microelectronic*, pp. 9–10, 2000.

[4] H.F. Achigui, C.J.B. Fayomi, M. Sawan "**A DTMOS-based 1 V op amp**," *IEEE International Conference on Electronics, Circuits and systems* , Vol. 1, pp. 252–255, 2003.

[5] H.F. Achigui, C.J.B. Fayomi, M. Sawan "**A 1 V Low-Power Low-Noise DTMOS Based Class AB Op amp**," *IEEE-NEWCAS,* pp. 307–310, 2005.

[6] H.F. Achigui, C.J.B. Fayomi, and M. Sawan, "**1 V DTMOS based class AB operational amplifier: Implementation and experimental results**," *IEEE Journal of Solid-State Circuits*, Vol. 41, No. 11, 2006.

[7] H.F. Achigui, M. Sawan, C.J.B. Fayomi, "**A 1 V Fully Differential, Fully Balanced Op amp: Implementation and Experimental Results**," *Analog Integrated Circuits and Signal Processing,* Vol. 53, No. 1, pp.19-25, 2007.

[8] E. Kargaran, M. Sawan, Kh. Mafinezhad, H. Nabovati, "**Design of 0.4V, 386nW OTA Using DTMOS Technique for Biomedical Applications**," *55th IEEE International Midwest Symposium on Circuits and Systems*, pp. 270–273, 2012.

[9] A. suadet, T. Thongleam, A. Kanjanop, P. Singhanath, B. Hirunsing, W. Chuenta, V. Kasemsuwan, "**A 0.8 V class-AB linear OTA using DTMOS for high-frequency applications**," *4th International Conference on Modeling, Simulation and Applied Optimization,* pp. 1-5, 2011.

[10] ZhiYuan Li, MingYan Yu, JianGuo Ma, "**A Novel Input Stage Based on DTMOS for Low-Voltage Low-Noise Operational Amplifier**" *APCCAS*, pp. 1591-1594, 2006.

[11] M.Razzaghpour, A.Golmakani, "**An Ultra-Low-Voltage Ultra-Low-Power OTA with Improved Gain-Bandwidth Product**," *in proc. IEEE ICM*, 2008.

[12] Sheng-Wen Pan, Chiung-Cheng Chuang, Chung-Huang Yang, Yu-Sheng Lai, "**A Novel OTA with Dual Bulk- Driven Input Stage,**" *IEEE International Symposium on Circuits and Systems*, pp. 2721-2724, May 2009.

[13] S. Sbaraini, A. Richelli and Zs.M. Kovacs-Vajna, "**EMI susceptibility in bulk-driven Miller opamp**," *Electronics Letters*, Vol. 46, No. 16, August 2010.

[14] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY: McGraw-Hill, 2001.

[15] S. Voldman, D. Hui, D. Young, R. Williams, D. Dreps, J. Howard, M. Sherony, F. Assaderaghi, G. Shahidi, "**Silicon-on-insulator dynamic threshold ESD networks and active clamp circuitry**", *Electrical Overstress/Electrostatic Discharge Symposium*, pp. 29-40, 2000.

[16] A. Guzinski, M. Bialko, and J. C. Matheau, "**Body-Driven Differential Amplifier for Application in Countinous-Time Active-C Filter**," *Proceedings of the European Conference on Circuit Theory and Design*, pp. 315-319, June 1987.

[17] Zuo, Liang, "**Low-Voltage Bulk-Driven Amplifier Design and Its Application in Implantable Biomedical Sensors,**" *PhD diss.*, University of Tennessee, 2012.

[18] G. Raikos, S. Vlassis, "**0.8 V bulk-driven operational amplifier**," *Analog Integrated Circuits and Signal Processing,* Vol.63, No. 3, pp. 425-432, 2010.