A 3.1-10.6 GHZ Ultra-Wideband CMOS Low Noise Amplifier in 0.18 µm CMOS Technology

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ABSTRACT:
A new ultra-wideband 3.1-10.6 GHz low noise amplifier (LNA), designed in chartered 0.18µm technology, is presented in this paper. Series inductive peaking in the feedback loop is used to improve the bandwidth of the LNA. Based on the noise-canceling technique, voltage gain is increased. Measurements show that the S_{11} and S_{22} are less than -10 dB, and the maximum amplifier gain S_{21} gives 12.9dB, and the minimum noise figure is 2.6dB, and the power consumption is 13.6 mW from 1.8V supply voltage.

KEYWORDS: CMOS, Low noise amplifier, Ultra-wideband,Gain.

1. INTRODUCTION

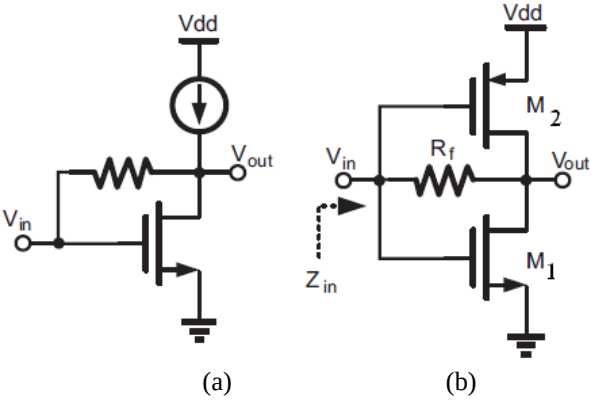
In recent years, the demand of ultra-wideband systems is exponentially increasing due to high data rate, lowcost, wider bandwidth and low power consumption[1]. In 2002, the Federal communication commission (FCC) approved the use 7500 MHz bandwidth for commercial applications in the 3.1-10.6 GHz [2-3]. A low noise amplifier (lna) is typically the first madule and a critical block for wireless front-end RF receiver [4]. Uwb performs for designing circuits such as medical imaging systems, radars, through-wall imaging systems and local area network. lna as the important module of the receiver must provide low power consumption to increase battry life, minimize return loss for good input matching, sufficient gain and low noise figure to improve the sensitivity of a receiver device and small area. Many topologies have been proposed in LNA designs, such as current reused amplifiers [6], cascade amplifiers [7], resistive shunt feedback [8] and distributed amplifiers. The distributed amplifier can improve gains and wideband input matching however it consumes large power. resistive shunt feedback provides gain flatness, stability and broadband input matching but increases NF due to the local feedback. In this paper, a two-stage broadband LNA for ultra-wideband applications in 0.18µm technology is proposed.

2. CIRCUIT DESCRIPTION

The most common resistive-feedback LNA is illustrated in Fig. 1(a), and Fig.1(b) shows an optimized topology which reuses the PMOS current source to reduce power and noise. In short channel process, the input impedance and voltage gain of the LNA in Fig. 1(b) are calculated as[9]:

$$\boldsymbol{Z_{in}} = \frac{\boldsymbol{r_{o1}} \| \boldsymbol{r_{o2}} + \boldsymbol{R_f}}{\mathbf{1} + (\boldsymbol{g_{M1}} + \boldsymbol{g_{M2}})(\boldsymbol{r_{o1}} \| \boldsymbol{r_{o2}})} \quad (1)$$

$$\boldsymbol{A_v} = \frac{[\mathbf{1} - (\boldsymbol{g_{M1}} + \boldsymbol{g_{M2}})\boldsymbol{R_f}](\boldsymbol{r_{on}} \| \boldsymbol{r_{op}})}{\boldsymbol{R_f} + \boldsymbol{r_{o1}} \| \boldsymbol{r_{o2}}} = -(\boldsymbol{g_{M1}} + \boldsymbol{g_{M2}})\boldsymbol{R_f} \quad (2)$$



(a) (b)

Fig.1. (a) Resistive-Feedback LNA,(b)With a current source

3. ANALYSIS OF PROPOSED WIDEBAND LNA

The proposed wideband LNA is illustrated in Fig.3. It consists of a resistive shunt feedback stage and noise canceling stage and an output buffer.

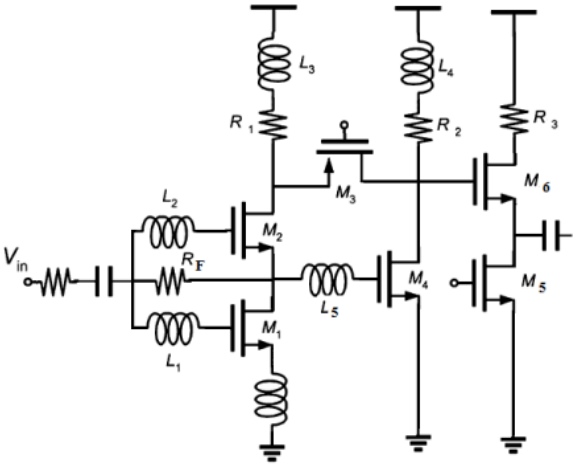


Fig.2. Proposed UWB LNA.

The main part of the LNA is illustrated in Fig. 3(a). two inductors are connected in series to the gates of $M_1$and M_2 transistors. The ac equivalent circuit model is also illustrated in Fig. 3(b). The inductors split the MOS Cgs and Cgdatthe input of the amplifier and enhances bandwidth extension.

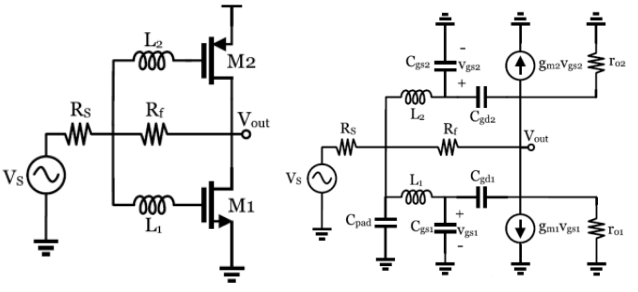


Fig. 3.(a) Resistive shunt feedback LNA with inductive series (b) its equivalent circuit model

3.1. Input Matching

At high frequencies, the input matching reduce by parasitic capacitances.

The input impedance is expressed as:

$$\boldsymbol{Z_1 = j\omega L_1 + 1/j\omega C_{gs1}} \quad (3)$$

$$Z_2 = j\omega L_2 + {}^{1}/_{j\omega C_{gs2}} \quad (4)$$

$$Z_{in} = \frac{Z_1 \| Z_2 \| (R_f + r_{o1} \| r_{o2})}{\left(\frac{g_{m1}(r_{o1} \| r_{o2})}{j\omega C_{gs1} Z_1} + \frac{g_{m2}(r_{o1} \| r_{o2})}{j\omega C_{gs2} Z_2}\right)} \quad (5)$$

3.2. Voltage Gian

Fig. 2 illustrates the noise-cancelling stage. In the noise-cancelling stage M_3 and M_4 are combining the signal and reduce the noise of M_1 [8]. R_1 and R_2 areresistors. In the LNA, M_3 is added, as the part of the current of M_3 flows into M_4, which increases g_{M4}.The cancellation of noise depends on the ratio of M_4 and M_3. The M_4 is performed in a common-source mode with a power gain of A_X.The M_3 is performed in a common-gate mode with a power gain of A_Y.A_X and A_Y are given by:

$$A_X = g_{m4} R_{L2} \quad (6)$$

$$\boldsymbol{A_Y = \frac{V_{D4}}{V_{S2}} \approx \frac{R_2 \| r_{o2} \| R_b}{R_1 \| r_{o2} \| (1/g_{m3}) \| (1/g_{m2})}} \quad (7)$$

Where R_b is the input resistance of the buffer. R_{L2} is equivalent load resistances at the drain of M_4.

At high frequency,Due to the affect of parasitic capacitors, the gain voltageof the UWB LNA reduces.an inter-stage inductor L_5 is embedded between the first and second stages to isolate the parasitic capacitances from each other to improve the gain bandwidth[8]. Due to the Fig.2, L_5, C_{gd},C_{eq} of feedback topology and Cgs_1 of M_1 from a wideband π section LC network.suitable choice of inductor L_5 can resonate with the parasitic capacitors that make gain peaking to compensate the high frequency gain roll-off of the devices, achieving the best flatness gain of the LNA. the value of L_5 is chosen as 2.0 nH to achieve high flat gain and bandwidth response.The simulation effect of L_5 on the S_{21} is shown in Fig.7.

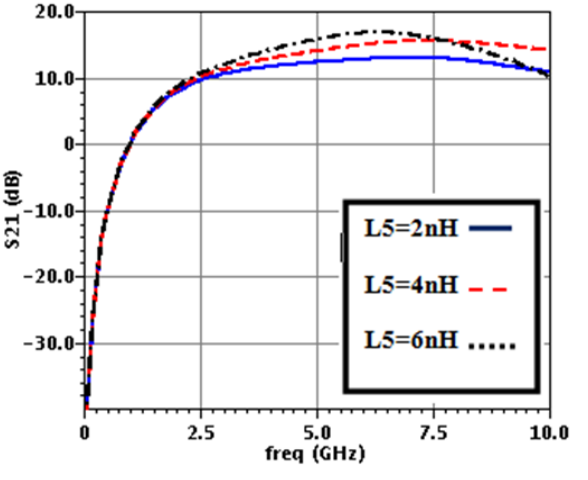


Fig. 4. Effect L_5 on the S_{21}

4. CONCLUTION

The UWB LNA was simulated in TSMC 0.18µm CMOS process. Simulations have been performed using Spectre simulator of cadence. Fig.5 shows the input return loss and output return loss of the UWB LNA, respectively. The simulated input and output return loss is below -10dB. Fig. 6 show the simulated power gain of the UWB LNA. Power gain lna is 10.5 dB. The simulation NF of the lna is illustrated in Fig.7.The minimum NF is 8.7dB.

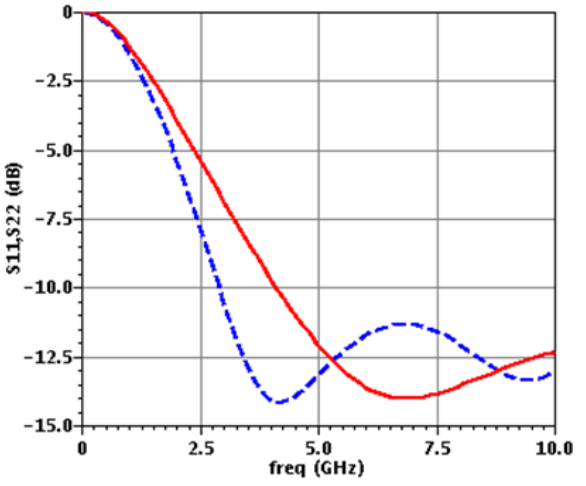


Fig. 5. Input and output return loss

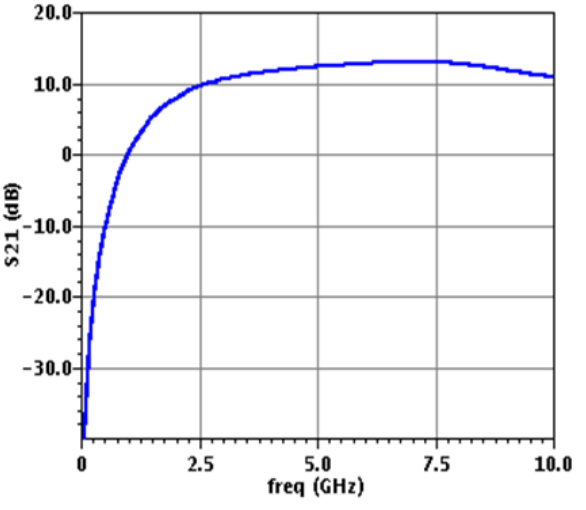


Fig. 6. Power gain

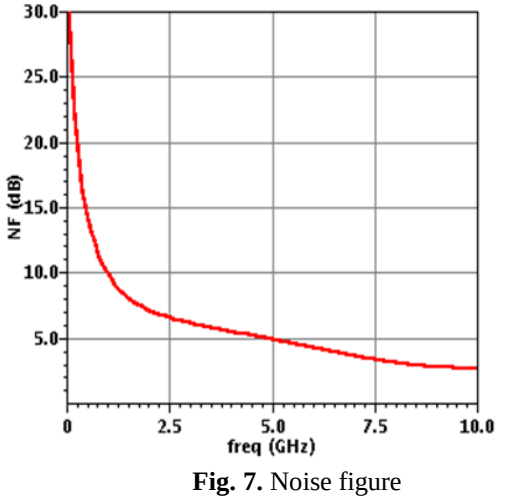


Fig. 7. Noise figure

The design parameters are summarized in Table 1. Table2 illustrates the performance summary of the proposed UWB LNA and makes a comparison with previous published ultra wideband LNA.

Table 1. Design parameters

Transistor size	$(W/L)_1$	$(W/L)_2$	$(W/L)_3$	$(W/L)_4$	$(W/L)_5$	$(W/L)_6$
	100/0.18	50/0.18	20/0.18	52/0.18	40/0.18	70/0.18
Resistor value	R_F	R_1	R_2	R_3	-	-
	200Ω	80Ω	180Ω	56Ω	-	-
Inductor value	L_1	L_2	L_3	L_4	L_5	-
	1.5nH	1.9nH	2.2nH	2.2nH	2nH	-

Table 2. Performance summary and comparsion

Reference	[9]	[11]	[12]	This work
Technology	65nm	65nm	0.18µm	0.18µm
BW(GHz)	0.4-10.6	1-10	3.1-10.6	3.1-10.6
P_{dc}(mW)	12	13.7	14.1	13.6
NF(dB)	3.5	2.7	2.8	2.6
S_{11}(dB)	<-11	<-10	<-10	<-10
S_{22}(dB)	<-10	<-10	<-10.5	<-10
S_{21}(dB)	10.4	10.5	15.6	12.9
FOM	7	2.05	9.16	8.68

REFERENCES

[1] A.Tanaka et al.,"**A 1.1 V 3.1-9.5 GHz MB-OFDM UWB transceiver in 90 nm CMOS**", *Journal of Solid-State circuits*, pp. 120-121, 2004.

[2] Hi Zheng et al., "**A 3.1GHz-8.0 GHz Single-Chip Transceiver for MB-OFDM UWB in 0.18-µm CMOS Process**", *IEEE Journal of Solid-State circuits*, Vol. 44, No.2, pp. 120-121, 2009.

[3] Le-HouChen, "**An Ultra Wideband 0.4-10 GHz LNA in 0.18µm CMOS**", *IEEE Transaction on circuits and systems-II*, Vol.54, No.3, pp. 217-221, 2007.

[4] Meng-Ting Hsu et al., "**Design of low power UWB LNA based on common source topology with current-reused technique**", *Microelectronics Journal*, Vol. 44, pp. 1223-1230, 2013.

[5] Yang Lu.et al., "**A Novel CMOS Low-Noise Amplifier Design for 3.1 to 10.6-GHz Ultra-Wide-Band Wireless Receivers,**. I*EEE Transactionson Circuitsand systems I*, Vol. 53, No. 8, pp. 1683-1691, 2006.

[6] Yi-Jing Lin et al.," **A 3.1-10.6 GHz ultra-wideband CMOS low noise amplifier with current-reused**

technique", *Microwave and Wireless Components Letters*, Vol. 17, No. 3, pp. 232-234, 2007.

[7] Ke-Hou Chen et al., "**An Ultra-Wide-Band 0.4-10 GHz LNA in 0.18µm CMOS",** *IEEE Circuits and systems*. Vol.54, No. 3, pp. 217-221, 2007.

[8] Ke-Hou Chen, Shen-Iuan Liu, "**Inductorless Wideband CMOS Low-Noise Amplifiers Using Noise-Canceling Technique**", *IEEE Transaction on circuits and systems-I*, Vol. 59, No. 2, pp. 305-314, 2012.

[9] Dong Huang et al, "**A resistive-feedback LNA in 65 nm CMOS with a gate inductor for bandwidth extension**", *Microelectronic Journal*, Vol. 46, No. 1, pp. 103-110. 2015.

[10] P. Heydari," **Design and analysis of a performance-optimized CMOS UWB distributed LNA**", *IEEE Journal of Solid-State Circuits*, Vol. 42, No. 9, pp. 1892-1905, 2007.

[11] Ke-Hou Chen, Shen-Iuan Liu," **Inductorless Wideband CMOS Low-Noise Amplifiers Using Noise-Canceling Technique**", *IEEE Transaction on circuits and systems-I*, Vol. 59, No. 2, pp. 305-314, 2012.

[12] Qiuzhen Wan, Chunhua Wang, "**Design of 3.1-10.6 GHz ultra-wideband CMOS low noise amplifier with current reuse technique**", *International Journal of Electronic and Communications*, Vol. 65, No. 1, pp. 1006-1011, 2011.