A 5Gbps, Inductor-less Transimpedance Amplifier for Optical Communications using 0.18µm CMOS Technology

Soorena Zohoori[1], Mehdi Dolatshahi[1*]
1- Department of Electrical Engineering, Najafabad Branch, Islamic Azad University, Najafabad, Iran.
*Corresponding Author: Dolatshahi@iaun.ac.ir

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ABSTRACT:
In this paper, a two-stage 5Gbps transimpedance amplifier (TIA) for an optical communication receiver system is presented. The presented TIA uses a regulated cascode configuration (RGC) as the input stage, which benefits from low input resistance, and is followed by a gain stage with negative feed-back network and a buffer stage in order to provide extra gain to operate properly at 5Gbps. DC operating point stabilizing is also considered in this paper. The proposed TIA is discussed mathematically and related simulations are performed in HSPICE using 0.18µm CMOS technology parameters. Results for the proposed TIA show the transimpedance gain of 42.1dBΩ, bandwidth of 3.6GHz, and power consumption of 12mW at 1.5V supply voltage. Also, Monte-Carlo analysis, noise analysis and effect of temperature variation on frequency response of the TIA are analyzed, which indicate that the proposed TIA is suitable to work as a 5Gbps TIA building block in an optical communication receiver system.

KEYWORDS: Transimpedance Amplifier, Inductor-less, Optical IC, CMOS Technology.

1. INTRODUCTION

Nowadays, demands for high-speed Giga-bit-per-second communication systems for multimedia applications are rapidly growing. Cable and optical fiber communication networks play a key role in modern communication systems. One of the important parts of an optical communication receiver system is its optical receiver (due to the fact that it interconnects the real world to the digital world), and the most critical part in an optical CMOS system, which affects the total receiver performance, is the TIA stage.

Recently, many researchers have reported different structures and techniques for designing high speed transimpedance amplifiers. Till now, two trends in designing TIAs are presented. First approach is to optimize the sensitivity and dynamic range, such as automatic gain control (AGC) [1-2]. The other approach beside considering trade-offs is to resolve the challenge of bandwidth, by using active inductive peaking technique [3], the zero pole cancellation [4], a three-dimensional inductor converter [5] and shunt peaking technique [6], in which a passive inductor is used. But, using inductors as a solution to extend the frequency bandwidth suffers from the requirement of a large occupied area on chip. Moreover, The RGC structure is usually used as TIA blocks in order to alleviate bandwidth reduction. The bandwidth reduction is due to the parasitic capacitance of the photodiode [7]. The advantage of using RGC stage for extending bandwidth of a TIA block in comparison with using inductive peaking technique is that the RGC stage would provide the same results without using a passive inductor, and so the area on chip can be saved [8].

In this paper, an inductor-less transimpedance amplifier for 5Gbps applications is presented utilizing the RGC input stage, which benefits from a low input resistance. RGC stage does not create such a small pole with parasitic capacitance of the photodiode due to its low input resistance. But it also cannot provide proper gain in high frequencies. That is why a gain stage is needed after the RGC stage at high data rates.

So, this paper is organized as follows: in section 2 the system structure is discussed. The proposed TIA circuit is given and discussed in section 3. Simulation results are shown in section 4. Section 5 brings noise analysis of the proposed TIA and finally, conclusion results are given in section 6.

2. SYSTEM STRUCTURE

The TIA stage is supposed to convert the current signal, which is produced by the photodiode, to an amplified voltage. Several parameters, such as transimpedance gain, bandwidth, sensitivity and dynamic range of a TIA mainly affect the performance of the optical communication receiver. As there are always trade-offs among bandwidth, gain, power

dissipation, input referred noise and voltage supply, designing the TIA stages gets more complicated when the parasitic capacitance of the photodiode becomes a bottleneck for Giga-bit-per–second applications.

The block diagram of a TIA stage is shown in figure (1). The block diagram in figure (1) is consists of RGC stage, Common Source (CS) stage, DC cancellation block, limiting amplifier (LA) stage (single-ended to double-ended converter (S2D)) and an output buffer. An OTA is also used as an error amplifier, as shown in figure (1).

3. THE PROPOSED TIA

In figure (2), the proposed TIA structure stage is shown. As it is shown in figure (2), the TIA consists of a RGC (regulated cascode) stage as the first stage, and a gain stage as the second stage of amplification and a buffer. In order to analyze the circuit, we open the closed loop of the TIA. In figure (3), the equivalent small signal circuit of the proposed TIA is also shown. By considering C_1 as the equivalent parasitic capacitance seen at drain of M1, and considering that $r_{o2} \gg R_2$, $r_{o3} \gg R_3$, it ca be defined as follows:

$$R'_f = R_1 \| \frac{R_f}{1+\alpha_2 .\ g_{m3} .\ R_3} \quad (1)$$

$$\alpha_2 = \frac{g_{m2} .\ R_2}{1+g_{m2} .\ R_2} \quad (2)$$

$$C_T = C_{pd} + C_{sb1} + C_{gsB} \quad (3)$$

$$C_Z = C_{gs1} + C_{gdB}. \quad (4)$$

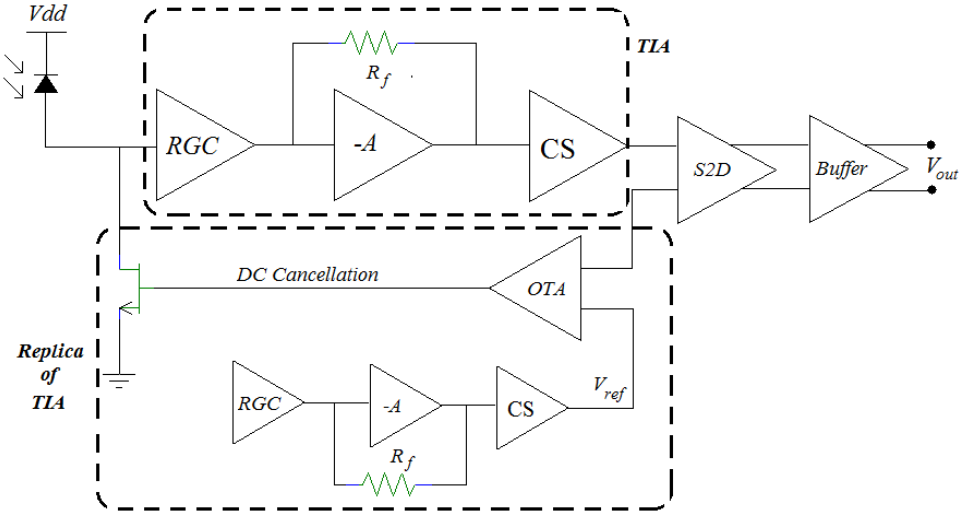


Fig. 1. Block Diagram of the Transimpedance Amplifier

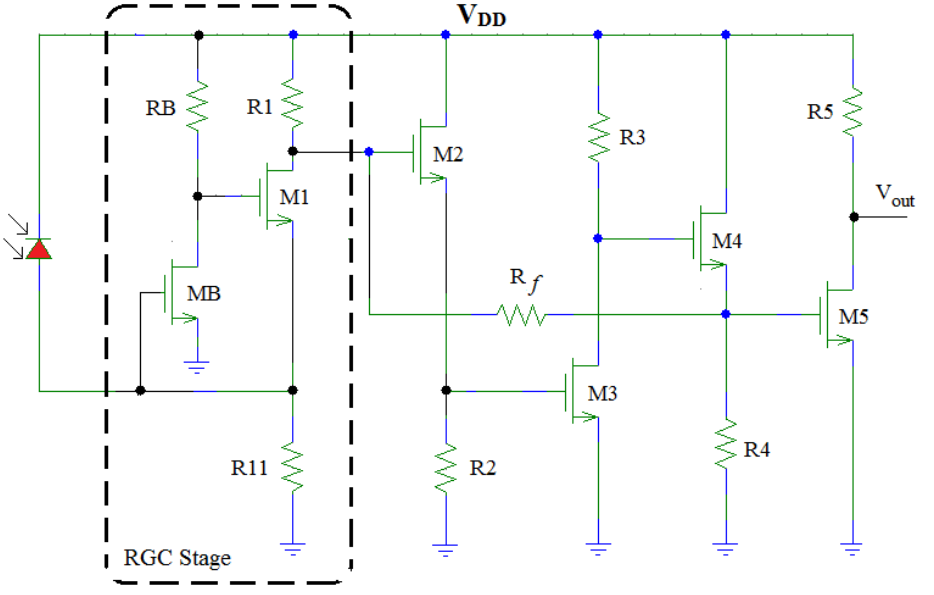


Fig. 2. The Proposed TIA

In order to ease the calculation of the transimpedance gain of the proposed TIA, each stage is calculated separately. At first, the calculation of the transimpedance gain of the RGC stage is considered, and then the calculation of the transimpedance gain of the gain stage is presented. So, the transimpedance gain of the RGC stage can be written as follows:

$$A_{i,RGC} = \frac{I_{eq}}{I_{in}}(s) \approx \frac{1+\frac{s.C_B}{g_{mb}}}{\left[1+\frac{s.C_T}{(1+g_{mb}.R_B)g_{m1}}\right][1+s.R_B(C_B+C_Z)]} \quad (5)$$

In which, C_B is the equivalent parasitic capacitance seen at drain of MB.

Also, transimpedance gain of the second stage can be written as follows:

$$\frac{V_{out}}{I_{eq}}(s) \approx \frac{g_{m2}.g_{m3}.R_2.R_3.R_f'}{1+g_{m2}.R_2}\left(1+\frac{s.C_{gs2}}{g_{m2}}\right) \times \left[1+\frac{s.\left(R_f'.C_{gs2}+g_{m2}.R_2.R_f'.C_1\right)}{1+g_{m2}.R_2}\right]^{-1} \times [1+\frac{s.(C_{gs2}+C_{gs3})}{g_{m2}}]^{-1} \quad (6)$$

Thus, the transfer function of the proposed TIA can be written as follows:

$$\frac{V_{out}}{I_{in}}(s) \approx \frac{g_{m2}.g_{m3}.R_2.R_3.R_f'}{1+g_{m2}.R_2}\left(1+\frac{s.C_{gs2}}{g_{m2}}\right) \times \left(1+\frac{s.C_B}{g_{mb}}\right) \times \left\{\left[1+\frac{s.C_T}{(1+g_{mb}.R_B)g_{m1}}\right].[1+s.R_B(C_B+C_Z)] \times \left[1+\frac{s.\left(R_f'.C_{gs2}+g_{m2}.R_2.R_f'.C_1\right)}{1+g_{m2}.R_2}\right].(1+s.R_2.C_{gs3})\right\}^{-1} \quad (7)$$

Moreover, it is possible to obtain the transimpedance gain from equation (3), as follows:

$$Z_T(0) = \frac{V_{out}}{I_{in}}(0) = \frac{g_{m2}.g_{m3}.R_2.R_3.}{1+g_{m2}.R_2}\left(R_1 \| \frac{R_f}{1+\alpha_2.\ g_{m3}.\ R_3}\right) \quad (8)$$

Also, the dominant pole of the proposed TIA can be written as follows:

$$P_1 = \frac{1+g_{m2}.R_2}{2\pi.R_f'\left(C_{gs2}+g_{m2}\ R_2\ C_1\right)} = \frac{1}{2\pi.R_f'\left(\frac{C_{gs2}}{1+g_{m2}.R_2}+\alpha_2 C_1\right)} \approx \frac{1}{2\pi\left(R_1 \| \frac{R_f}{1+\alpha_2.\ g_{m3}.\ R_3}\right).(C_{db1}+C_{g2})} \quad (9)$$

Equation (8) is explaining that by increasing R_f and R_1 the transimpedance gain will increase. But equation (9) reveals that large value of R_1 and R_f will result in reduction of frequency bandwidth. However, frequency bandwidth and transimpedance gain can be increased by increasing R_3 or by increasing transconductance of M3. Of course, sub-micron CMOS technologies limit the transimpedance gain of amplifiers, so increasing $g_{m3} \times R_3$ is limited. Moreover, as in equation (9), due to the low input resistance of the RGC stage and the fact that the parasitic capacitance of the photodiode is effectively isolated in RGC structure, the input pole is no longer count as the dominant pole in this structure.

In addition, it is worth discussing that sometimes the produced current by the photodiode may experience a peak in its value, and this might result in some changes like distortion in pulse width on the signal path. That clearly explains the requirement of a DC cancellation circuit for wide dynamic circuits. This circuit is supposed to stabilize the DC operating point by reducing the injected average current into the amplifier. This

method separates the average components from the input current produced by the photodiode.

So, without the dc-cancellation circuit, changes in node voltages of the RGC stage may result in changes in amplitude of the input current. In figure (2), voltage at source of M1 changes negligibly, whenever the amplitude of the input current signal is small. Also, V_{gs} of MB and V_{ds} of M1 decrease, if the amplitude of the input current signal increases. MB may also operate in linear region, if the input current increases exponentially. This means a large offset occurs in the RGC stage, which results in providing no waveform at the output node.

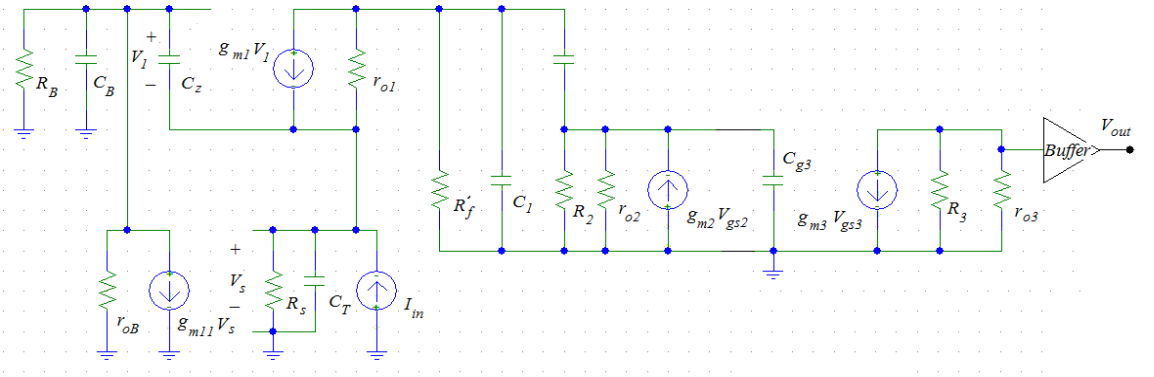


Fig. 3. The Equivalent Small Signal Circuit of the Proposed TIA

4. SIMULATION RESULTS

To verify the circuit performance of the proposed TIA, the proposed TIA is simulated in HSPICE using 0.18µm CMOS technology parameters. Figure (4), shows the frequency response and phase of the proposed TIA. As it can be seen, the transimpedance gain of the proposed TIA is equal to 42.1dbΩ, and its frequency bandwidth is equal to 3.6GHz. Also, power dissipation of the proposed TIA is equal to 12mW at 1.5V supply. Moreover, the simulated results show the phase margin of 70º for the proposed TIA.

However, eye-diagram of the proposed TIA circuit is simulated in HSPICE using PRBS7, and is shown in figure (5), in which the results show that the eye is opened about 70mV.

Also, effect of temperature variation in frequency response of the TIA is shown in figure (6). As it can be seen, in figure (6), for 120^{o}C variation in temperature, the transimpedance gain of the TIA varies from 40.8dBΩ to 42.7dbΩ, and the frequency bandwidth varies from 2.87GHz to 4.42GHz.

In addition, Monte-Carlo analysis for analyzing the mismatch in fabrication process is performed in HSPICE for 200 runs and the results are shown in figure (7). In figure (7-a), the Monte-Carlo analysis is done over frequency response and figure (7-b) shows the Monte-Carlo analysis over the transimpedance gain of the proposed TIA, which shows the mean value of 127.7 and standard deviation of 2.9.

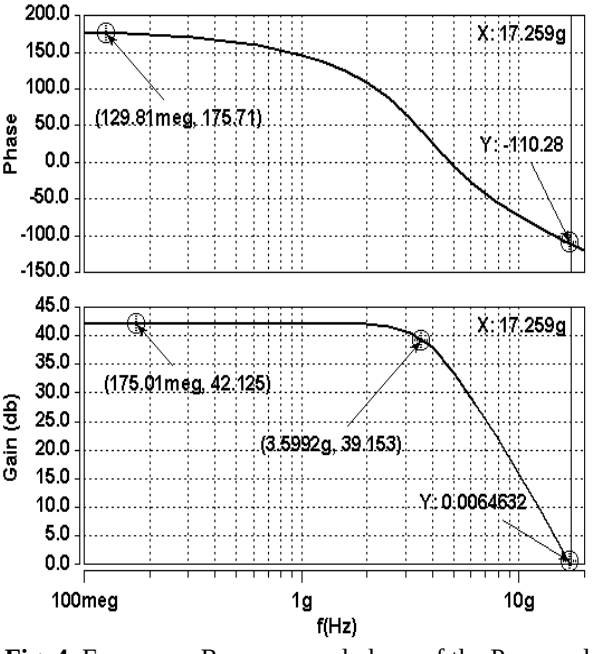


Fig. 4. Frequency Response and phase of the Proposed TIA

Moreover, as it is discussed before, the parasitic capacitance of the photodiode is relatively large, and makes it instructive to analyze the input resistance of the proposed TIA. Figure (8), shows the simulated input resistance and input impedance of the proposed TIA circuit. As it is shown in this figure, the input resistance of the proposed TIA at low frequencies is equal to 32.7Ω while at -3dB frequency is equal to 38.6Ω

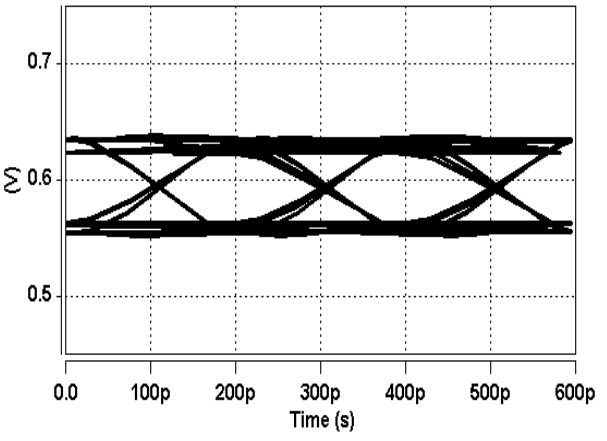


Fig. 5. Simulated eye-diagram

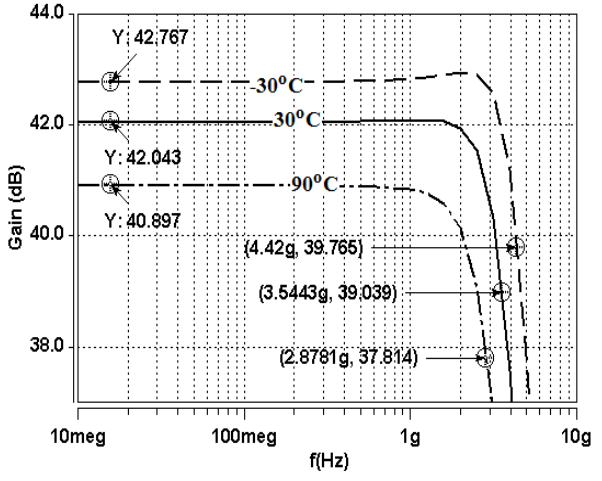
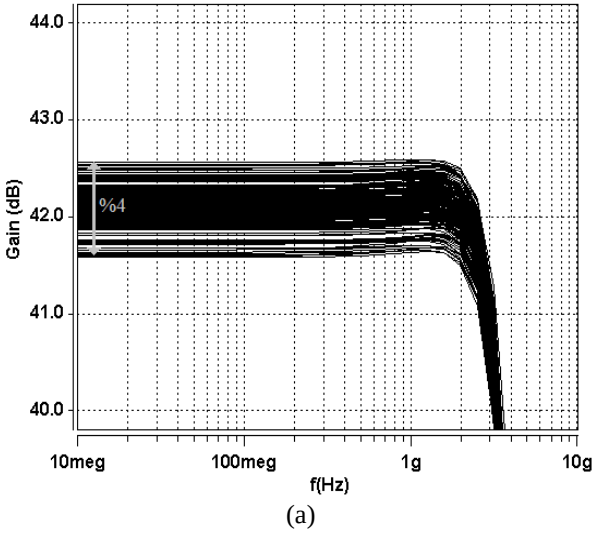
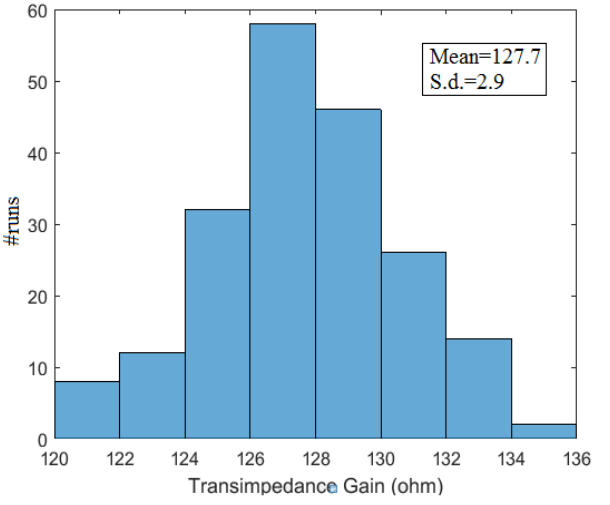


Fig. 6. Effect of Temperature variation on frequency response for 120^{O}C variation



(a)



(b)

Fig. 7. Monte-Carlo analysis (a) on frequency response (b) on transimpedance gain.

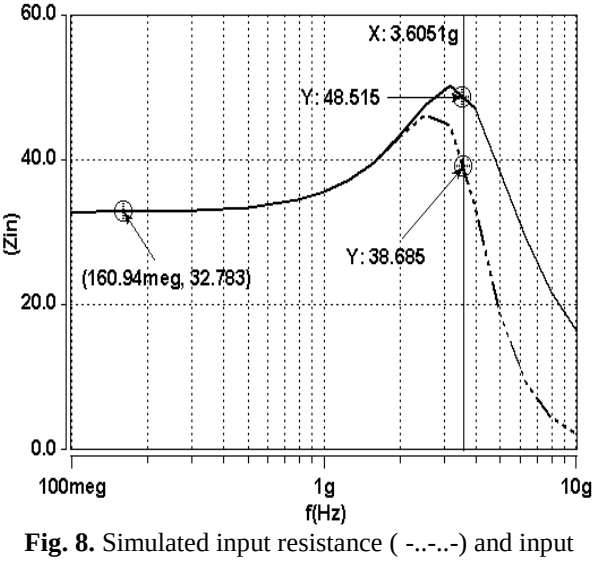


Fig. 8. Simulated input resistance (-..-..-) and input impedance (**—**) of the proposed TIA

5. NOISE ANALYSIS

By neglecting the flicker noise for simplicity, the equivalent input thermal referred noise of the proposed TIA circuit (considering resistors and channel thermal noise), can be written as follows:

$$\overline{I_{n,eq}^2} \approx \overline{I_s^2} + \overline{I_{Rf}^2} + \overline{I_{R1}^2} + \left(\frac{s.C_1}{g_{m3}}\right)^2 .\left(\overline{I_{d3}^2} + \overline{I_{R3}^2}\right) + \left[\frac{R_B\,[1+s.C_T)}{(1+g_{mB}\,.R_B)R_s}\right]^2 \overline{I_B^2} + \left(\frac{s.C_z}{g_{m1}}\right)^2 .\left(\overline{I_{d1}^2} + \overline{I_{Rf}^2} + \overline{I_{R1}^2}\right)$$

$$\approx 4KT\left(\frac{1}{R_s}+\frac{1}{R_f}+\frac{1}{R_1}\right)+\frac{4KT\,\omega^2\left(C_{db1}+C_{gs2}\right)^2}{g_{m3}^2}\left(\gamma+\frac{1}{R_3}\right)$$
$$+\frac{4KT\omega^2\left(C_{gs1}+C_{gdB}\right)^2}{g_{m1}^2}\left(\gamma+\frac{1}{R_f}+\frac{1}{R_1}\right)$$
$$+\frac{4KT\,R_B^2\left[1+\omega^2\left(C_{pd}+C_{gsB}+C_{sb1}\right)^2\right]}{(1+g_{mB}\,R_B)^2R_S^2}(\gamma+\frac{1}{R_B})$$

As it can be extracted from equation (10), in order to reduce the input referred noise current, g_{m3}, g_{m1}, R_s, R_f and R_1 should be increased. Furthermore, the size of M_1, M_2 and M_B should be as small as possible to reduce the noise current produced by the parasitic capacitance.

As equation (5) reveals, large values for R_f and R_1 will result in frequency bandwidth reduction. So, the proper noise current can be achieved by proper choice of $\frac{W}{L}$ ratio for M_1 and M_3 and proper bias current.

So, the output and input referred noise of the proposed TIA circuit is simulated in HSPICE and is shown in figure (9).

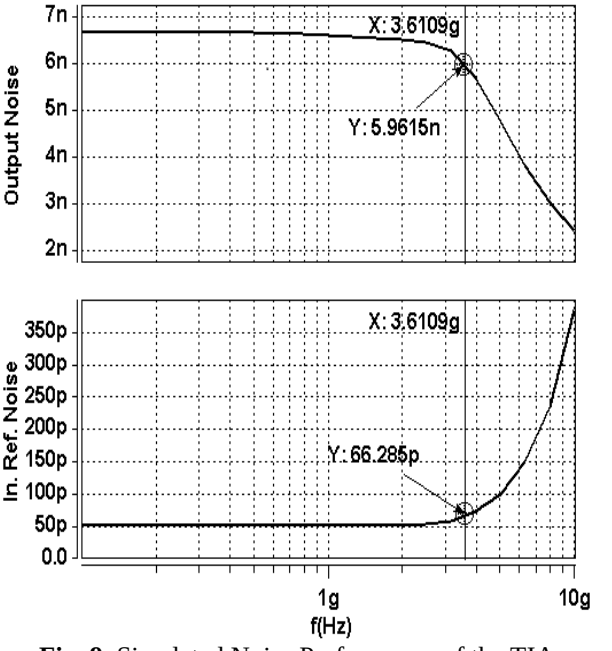


Fig. 9. Simulated Noise Performance of the TIA

Finally, table (1) compares the proposed TIA with other reported ones. However, in order to perform a fair comparison between the proposed TIA and other reported designs, Figure of Merit (FOM) as a standard definition is defined as equation (11), as follows:

$$FOM=\frac{Gain\times BW\times C_{in}}{P_{DC}\times In.Ref.Noise}\ (\frac{dB\Omega.GHz.pF}{mW.\ \mu A_{rms}}) \qquad (11)$$

Table 1. Performance comparison between the proposed TIA and other reported designs

	[9]	[10]	[11]	[12]	[13]	[14]	[15]	[17]	This Work
Year	2016	2013	2015	2016	2016	2017	2017	2016	2017
Technology (CMOS)	0.18µm	0.18µm	0.13µm	0.13µm	0.13µm SiGe BiCMOS	0.18µm	0.13µm SiGe BiCMOS	0.18µm	0.18µm
Supply Voltage (V)	1.8	1.8	1.5	1.5	3.3	1.8	3.3	1.8	1.5
Gain(dBΩ)	58	46	50.1	54	72	59	83.7	55-69	42.1
Power Consumption (mW)	34.8	31.5	7.5	45	261	18	150	6	12
C_{pd} (pF)	0.3	0.25	0.25	-	-	0.3	-	-	1
Bandwidth (GHz)	8.1	8	7	11.5	38.4	7.9	32.1	1	3.6
Input referred noise(μA_{rms})	1.35	3.5	2.6	0.729	2.9	2.01	-	0.29	3.2

No. of passive inductors	2	2	0	2	0	2	0	0	0
FoM	3	0.9	4.4	-	-	3.8	-	-	3.8

6. CONCLUSION

In this paper, a low-power and inductor-less structure is proposed as transimpedance amplifier for 5Gbps applications to operate in an optical communication receiver system. An RGC stage is used as the first stage of the presented TIA to provide proper bandwidth. In order to obtain proper transimpedance gain at high frequencies, a closed-loop gain stage is used after the RGC stage, which is followed by a common-source stage. Simulation results in HSPICE using 0.18µm CMOS technology parameters for the proposed TIA show the bandwidth of 3.6GHz, transimpedance gain of 42.1dbΩ and power consumption of only 12mW at 1.5V supply. Analysis such as eye-diagram, Monte-Carlo, noise analysis and effect of temperature variation are simulated in HSPICE and discussed. Results indicate that the proposed TIA is suitable to work as a 5Gbps transimpedance amplifier for an optical communication receiver system.

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