A 0.8 V 191.9 nW DTMOS Current Mirror OTA in 0.18 µm CMOS Process

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ABSTRACT:
In this paper a low-noise low-power CMOS operational transconductance amplifier (OTA) using dynamic threshold voltage MOSFET (DTMOS) technique is presented. The OTA is designed and simulated using 0.18 µm CMOS technology. The performed simulation results show an input-referred noise of 520.2 nV/√Hz at 1 mHz so reduces to 115.8 pV/√Hz at 1 Hz, and a power consumption of 191.9 nW under 5 pF loads. The dc open loop gain is 53.13 dB, a phase margin of 50° and a unity gain-bandwidth (UGB) of 572.9 kHz while operating at 0.8 V supply voltage. The proposed OTA is suitable for low noise and low-power application such as medical application.

KEYWORDS: Bulk-driven, CMOS, DTMOS, Low-noise, Low-power, Operational amplifier, OTA.

1. INTRODUCTION

In the past few years with the rapid growth of market for portable devices such as cell phones, portable computers and medical electronic implants devices, design of analog integrated circuits at low-voltages with high performance has become an extremely important issue. Reduction of threshold voltage is necessary for low voltage operation, so various techniques have been proposed for low-voltage low-power analog integrated circuits design.

A MOSFET can be operated at a lower voltage by forward biasing the source-bulk junction (forward body-bias). This approach has been used to design a low-voltage low-power CMOS operational amplifier, but with increasing forward body-bias, the leakage current increases significantly. The DTMOS technique in 1994 (Assaderaghi et al, 1994) is proposed to overcome the drawback in a forward-biased MOSFET [1]-[3]. This technique can be used in connection with the back-gate forward-bias technique in designing low-voltage low-power analog, digital and mixed signal CMOS integrated circuits.

Several papers have been focused on design of CMOS opamp and operational transconductance amplifier (OTA) based on DTMOS technique. In [4]-[7] the authors presented a novel class AB op amp for low-voltage (1 V) applications. In [8] the authors proposed an ultra-low-voltage ultra-low-power operational transconductance for biomedical applications. In [9] the authors presented a 0.8 V class-AB linear OTA for high-frequency applications. In [10] a novel input stage for low-voltage low-power and low-noise operational amplifier has been described.

The organization of this paper is as follows. In Section 2, the DTMOS technique is presented. The structure of proposed OTA is described in Section 3. In this section the presented OTA is also designed using bulk-driven method. The simulations results are provided in Section 4 and finally the conclusion is given.

2. DTMOS TECHNIQUE

An effective method for reducing power consumption is reduction the power supply voltage. A constraint to implementing digital and analog circuits at low-voltage is the threshold voltage. DTMOS technique is the best idea for reduction threshold voltage. In DTMOS technique, the bulk is tied to its own gate as shown in Fig. 1.

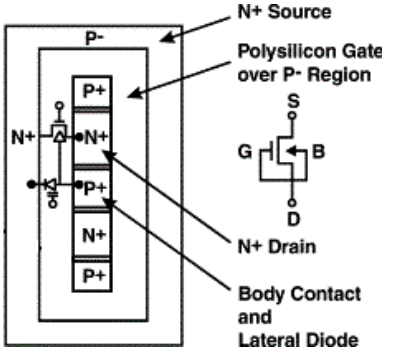


Fig. 1. Dynamic threshold MOSFET device [11].

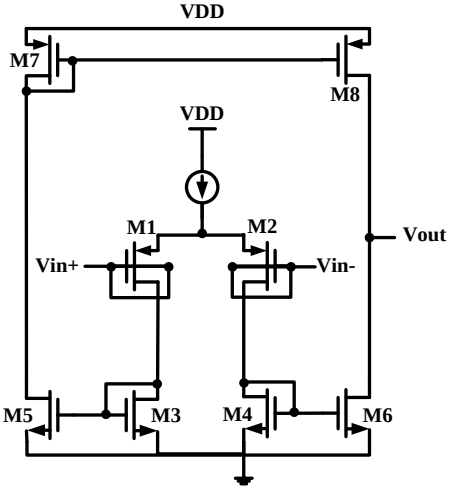
The DTMOS technique reduces the transistor off-state leakage current and also reduces the threshold voltage during on-state ($V_{BS} > 0$) according to below equation [12]:

$$V_{th} = V_{th0} + \lambda\left(\sqrt{|2\varphi_f - V_{BS}|} - \sqrt{|2\varphi_f|}\right) \quad (1)$$

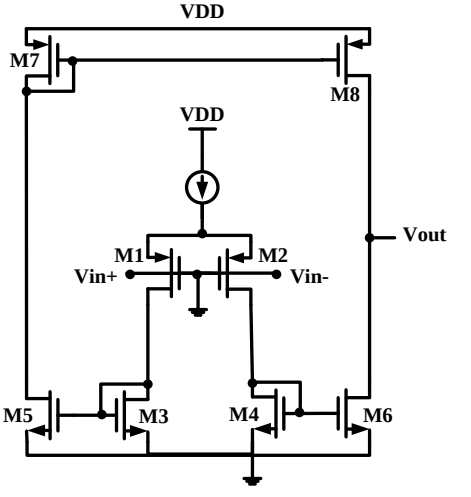
Where V_{BS} is the source-bulk voltage, V_{th0} the threshold voltage for $V_{BS} = 0$, λ is body effect factor with an approximate value between 0.3 to $0.4\sqrt{\text{V}}$, and φ_f is Fermi potential with a typical value in the range of 0.3- 0.4 V [12].

3. DESIGN LOW-NOISE LOW-POWER OTA

Fig. 2 shows the schematic of a low-noise low-power OTA based on DTMOS and bulk-driven technique. These structures combine a fully differential pair with a current mirror load. We used DTMOS and bulk-driven transistors pairs (M1, M2) in differential pair. All transistors is biased in the sub-threshold region



(a): DTMOS technique.



(b): Bulk-driven technique.

Fig. 2. Schematic of the proposed OTA.

3.1 DC gain

The small-signal DC gain of the OTA is given by:

$$A_0 = (g_{m2} + g_{mb2}) * \left(1/g_{m4} \,\square\, r_{o2}\right) * \ldots \\ * g_{m6}\left(r_{o6} \,\square\, r_{o8}\right) \quad (2)$$

While the transconductance g_{mb} can be calculated as given in (3), [12]:

$$g_{mb} = \frac{\lambda}{2\sqrt{2\varphi_f + V_{SB}}} g_m = \eta g_m \quad (3)$$

The transconductance g_{mb} varies from 20% to 30% of g_m for the same transistor in a CMOS process [8].

3.2 AC analysis

Small-signal analysis of the circuit in Fig. 2 (a), results in the following equation:

$$P_1 \approx -\frac{1}{R_1 C_1} \\ C_1 = C_{db8} + C_{dg8} + C_{dg6} + C_{db6} \quad (4) \\ R_1 = r_{o8} \,\square\, \left[r_{o6}\left(1 + (g_{m6} + g_{mb6})(r_{o2} \,\square\, r_{o4})\right)\right]$$

and

$$P_2 \approx -\frac{1}{R_2 C_2} \\ C_2 = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{sb6} + C_{gs6} \quad (5) \\ R_2 = r_{o2} \,\square\, r_{o4}$$

3.3 Noise analysis

The input-referred noise (includes thermal noise and flicker noise) of the proposed OTA is described as:

$$\frac{1}{2}V_n^2(f) = \ldots$$
$$= \frac{\left(\frac{K_{fp}}{C_{ox}W_8L_8f}\right)\left(\frac{g_{m8}}{g_{m6}}\right)^2 + \frac{4kT\gamma}{g_{m6}}\left(\frac{g_{m8}+g_{m6}}{g_{m6}}\right) + \frac{K_{fn}}{C_{ox}W_6L_6f}}{(g_{m2}+g_{mb2})*\left(\frac{1}{g_{m4}}\,\square\, r_{o2}\right)*g_{m6}(r_{o6}\,\square\, r_{o8})} + \left[\frac{K_{fn}}{C_{ox}W_4L_4f} + \frac{4kT\gamma}{g_{m4}}\right]\left(\frac{g_{m4}}{g_{m2}+g_{mb2}}\right)^2 + \frac{K_{fp}}{C_{ox}W_2L_2f} + \frac{4kT\gamma}{g_{m2}+g_{mb2}} \quad (6)$$

Where C_{ox} is capacitance per unit area of the gate oxide, W and L are the channel width and length respectively, K_{fn} is NMOS flicker noise coefficient, K_{fp} is PMOS flicker noise coefficient, k is the Boltzmann constant and T is the absolute temperature. The derived coefficient γ is equal 2/3 for long-channel transistors and may need to be replaced by a larger value for submicron MOSFETs. It also varies to some extent with the drain-source voltage [12].

4. SIMULATION RESULTS

The presented OTA has been simulated with HSPICE in a 0.18 µm CMOS staard technology under 5pF load. The simulated AC results for DTMOS OTA and bulk-driven OTA are shown in Fig.3.

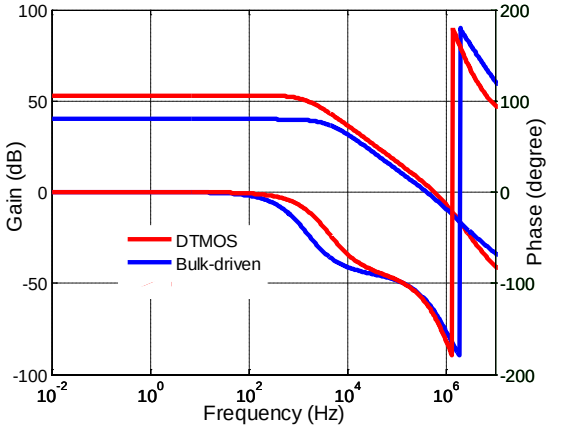


Fig. 3. Simulated open loop gain and phase margin.

This Figure show the, DC gain of 53.13 dB with unity gain-bandwidth up to 572.9 kHz for DTMOS OTA and DC gain of 39.97 dB with unity gain-bandwidth up to 395.9 kHz for bulk-driven technique. The phase margin for DTMOS OTA is 50º and the input-referred noise is 520.2 nV/√Hz at 1 mHz. The noise performance for DTMOS OTA is shown in Fig. 4.

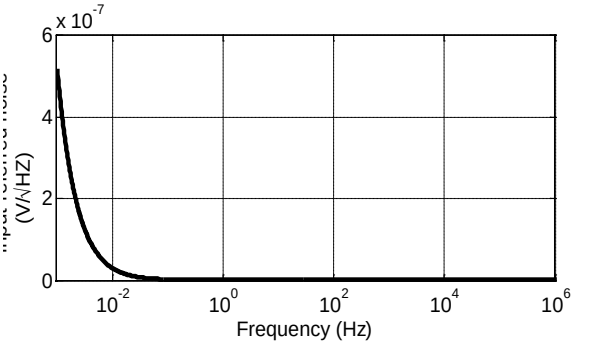


Fig. 4. Simulated input-referred noise.

Table 1 shows a comparison with other low-voltage operational amplifiers. To evaluate this work a figure of merit (FoM) is defined as [8]:

$$FoM = \frac{Gain * UGB}{Power\ supply * Power\ consumption} \quad (7)$$

5. CONCLUSION

A 0.8 V low-noise low-power CMOS operational amplifier was proposed in this paper. The proposed op amp utilizes DTMOS technique. The simulation results show that the DC gain of the presented amplifier is equal to 53.13dB while achieving unity gain bandwidth of 572.9 kHz and phase margin 50º. The total power consumption of the op amp is 191.9 nW. This low-noise low-power architecture is very useful in biomedical applications in which the power budget is limited. Also simulation results are shown that DTMOS technique is superior compared to the bulk-driven technique.

REFERENCES

[1] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. K. Ko, and C. Hu, **"A dynamic threshold voltage MOSFET (DTMOS) for ultra-low voltage operation,"** in *Int. Electron Devices Meeting, Techn. Digest*, 1994, pp. 809–812.

[2] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P.K. Ko and Hu. Chenming, **"Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI,"** *IEDM Trans*, vol. 44 Mar 1997, pp. 414-422.

[3] F. Assaderaghi, **"DTMOS: Its derivatives and variations, and their potential applications,"** in *Proc. 12th Int. Conf. Microelectron.*, 2000, pp. 9–10.

[4] H.F. Achigui, C.J.B. Fayomi and M. Sawan **"A DTMOS-based 1 V op amp,"** *Proc. IEEE ICECS*, vol. 1, pp. 252–255, Dec. 2003.

[5] H.F. Achigui, C.J.B. Fayomi and M. Sawan **"A 1 V Low-Power Low-Noise DTMOS Based Class AB Op amp,"** *Proc. IEEE NEWCAS*, pp. 307–310, 2005.

[6] H.F. Achigui, C.J.B. Fayomi and M. Sawan, **"1 V DTMOS based class AB operational amplifier: Implementation and experimental results."** *to*

appear, IEEE J. Solid-State Circuits, vol. 41, no. 11, Nov. 2006.

[7] H.F. Achigui, M. Sawan and C.J.B. Fayomi, **"A 1 V Fully Differential, Fully Balanced Op amp: Implementation and Experimental Results,"** *Analog Integr Circ Sig Process* (2007) 53:19–25.

[8] E. Kargaran, M. Sawan, Kh. Mafinezhad and H. Nabovati, **"Design of 0.4V, 386nW OTA Using DTMOS Technique for Biomedical Applications"** in *Proc. 55th IEEE International Midwest Symposium on Circuits and Systems*, 2012, pp. 270–273.

[9] A. suadet, T. Thongleam, A. Kanjanop, P. Singhanath, B. Hirunsing, W. Chuenta and V. Kasemsuwan, "**A 0.8 V class-AB linear OTA using DTMOS for high-frequency applications**" in *Proc. ICMSAO*, 2011, pp. 1-5.

[10] ZhiYuan Li, MingYan Yu, JianGuo Ma, **"A Novel Input Stage Based on DTMOS for Low-Voltage Low-Noise Operational Amplifier"** in *Proc. APCCAS*, 2006, pp. 1591-1594.

[11] S. Voldman, D. Hui, D. Young, R. Williams, D. Dreps, J. Howard, M. Sherony, F. Assaderaghi and G. Shahidi, **"Silicon-on-insulator dynamic threshold ESD networks and active clamp circuitry"** in *Proc. Electrical Overstress/Electrostatic Discharge Symposium*, 2000, pp. 29-40.

[12] B. Razavi, ***Design of Analog CMOS Integrated Circuits***. New York, NY: McGraw-Hill, 2001.

[13] G. Raikos and S. Vlassis, **"0.8 V bulk-driven operational amplifier**," *Analog Integr Circ Sig Process* (2010) 63:425–432.

Table 1. Comparison proposed OTA with other low-voltage operational amplifiers.

	DTMOS	**Bulk-driven**	**[5]**	**[8]**	**[13]**
Technology (µm)	0.18	0.18	0.18	0.18	0.18
Power supply (V)	0.8	0.8	1	0.4	0.8
Power consumption (µW)	0.192	0.196	33.1	0.386	100
Gain (dB)	53.13	39.97	60	91	56
Phase margin	50°	55°	62°	66°	45°
UGB (MHz)	0.573	0.396	2.73	0.111	3.2
CMRR (dB)	72.1	53.5	100	106	80
PSRR (dB)	65.15 @ 100 Hz	49.8 @ 100 Hz	N/A	N/A	88 @ 10 kHz
Slew Rate (V/µs)	17.3	13.3	N/A	0.022	N/A
Output voltage swing (V)	0.65	0.63	0.8	N/A	N/A
Input-referred noise $\left(nV/\sqrt{Hz}\right)$	0.115 @ 1 Hz	2.5 @ 1 Hz	107 @ 1 kHz	10 @ 10 mHz	408 @ 10 kHz
C_{Load} **(pF)**	5	5	5, 10 kΩ	15	20
FOM ($dB.MHz/V.\mu W$**)**	198.2	100.64	4.95	65.42	2.24