A 0.4 V low frequency voltage-controlled ring oscillator Using DTMOS technique

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ABSTRACT:
In this paper, an ultra-low power ultra-low voltage five-stage low frequency voltage-controlled single-ended ring oscillator using dynamic threshold voltage MOSFET (DTMOS) is presented. The proposed oscillator is designed and simulated using TSMC 0.18μm RF CMOS technology with 0.4 V power supply. In this design all transistors working at the sub-threshold (weak inversion) region. The output frequency ranges from 26.6-210.5 kHz with control voltages of 0 V to 0.4 V. Its power consumption and phase noise at a 100 kHz offset at the minimum (maximum) oscillation frequency is respectively 6.42nW (8.62 nW) and -120.5 dBc/Hz (-113.15 dBc/Hz).

KEYWORDS: Current starved, DTMOS, Single-ended, Sub-threshold, Voltage-controlled ring oscillator, VCO.

1. INTRODUCTION

The voltage-controlled oscillators (VCO) are the necessary component in analog and digital circuits. There are many different implementations of VCOs such as ring oscillator and LC tank. LC oscillators have good phase noise performance, but low frequency swing and the on chip combination of inductor and capacitor consumes large layout area. On the other hand, ring oscillators usually have a wide tuning range and occupy less on chip integration area [1]. Due to flexibility for on chip integration, CMOS ring oscillators have become an essential building block in many digital and communication systems. They are used as VCOs in applications such as clock recovery circuits for serial data communications, disk-drive read channels, on-chip clock distribution and integrated frequency synthesizers [2]. The key metrics of a VCO include oscillation frequency, tuning range, phase noise, and power consumption.

A ring oscillator is comprised of a number of delay stages (odd number of inverters), with the output of the last stage feedback to the input of the first. The oscillation frequency is determined by the number of stages and the delay in each stage. Sometimes to achieve low frequency increase the delay for each stage is used instead of increasing the number of stages [1].

Several papers have been focused on design of low power low voltage ring oscillator, In [3] an ultra-low power ring oscillator for passive UHF RFID transponders is proposed. In [4] two low power high-tuning range CMOS ring oscillator VCOs are presented. In [5] a three stage ultra-low power, low voltage ring oscillator is presented. In [6] a low power and high speed CMOS voltage-controlled ring oscillator is presented. In [7], [8] low power voltage controlled ring oscillator for medical applications is proposed.

The organization of this paper is as follows. In Section 2, the DTMOS technique is presented. In section 3, the sub-threshold operation is discussed. The structure of proposed single-ended ring oscillator is described in Section 4. The simulations results are provided in Section 5 and finally the conclusion is given.

2. DTMOS TECHNIQUE

An effective method for reducing power consumption is reduction the power supply voltage. A constraint to implementing digital and analog circuits at low voltage is the threshold voltage. DTMOS technique is the best idea for reduction threshold voltage. The DTMOS technique in 1994 (Assaderaghi et al) is proposed to overcome the drawback in a forward-biased MOSFET [9]-[11]. This technique can be used in designing low voltage low power analog, digital and mixed signal CMOS integrated circuits. In this technique, the bulk is tied to its own gate as shown in Fig. 1.

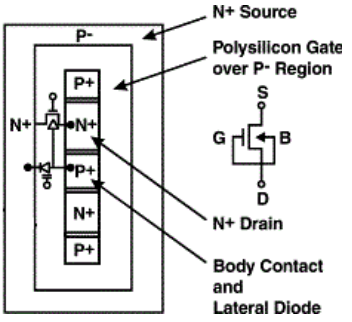

Fig. 1. Dynamic threshold MOSFET device [12].

The DTMOS technique reduces the transistor off-state leakage current and also reduces the threshold voltage during on-state (V_{BS} > 0) according to below equation [13]:

$$V_{th} = V_{th0} + \lambda\left(\sqrt{|2\varphi_f - V_{BS}|} - \sqrt{|2\varphi_f|}\right) \quad (1)$$

Where V_{BS} is the source-bulk voltage, V_{th0} the threshold voltage for $V_{BS} = 0$, λ is body effect factor with an approximate value between 0.3 to 0.4 $\sqrt{V}$, and φ_f is Fermi potential with a typical value in the range of 0.3- 0.4 V [13].

3. SUB-THRESHOLD OPERATION

When the V_{GS} in the MOS transistor is less than the threshold voltage (V_{th}), the MOSFET works in sub-threshold region. The drain current I_D of a MOS transistor in sub-threshold region is based on the channel diffusion current and can be given by (2), when referred to source voltage [13].

$$I_D = I_S\left(\frac{W}{L}\right) exp\left(q\frac{V_{GS} - V_{th}}{nKT}\right)\left[1 - \exp\left(-q\frac{V_{DS}}{KT}\right)\right] \quad (2)$$

Where I_S is the characteristic current, T is the absolute temperature, n is the slope factor, K is the Boltzmann constant and q is the charge of the electron or hole. If $V_{DS} \geq 3KT/q$ then the transistor will be saturated in sub-threshold region. The transconductance g_m can be found as presented in (3), which is a function of current Ids and factor nKT/q [14].

$$g_m = q\frac{I_D}{nKT} \quad (3)$$

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4. CIRCUIT DESCRIPTION

The schematic of the proposed five-stage voltage-controlled ring oscillator is shown in Fig. 2. For 0.4 V power supply operation, the DTMOS technique is used to reduce the threshold of the MOS transistors in the current starved (CS) delay cell and bias circuit. So the oscillation frequency should not be sensitive to variation of power supply and temperature, current starved delay cell is selected. Also CS improves the efficiency of the system by reducing the power consumption. The operation of current starved VCO is similar to the ring oscillator. Middle MOSFETs M2 and M3 operate as a typical inverter, while upper and lower MOSFETs (M4 and M1) operate as current sources. The current sources limit the current available to the inverter. In other words, the inverter is starved for current [15]. The currents in bias circuit transistors are mirrored in each stage and oscillation frequency can be adjusted by control voltage.

To determine the design equations for use with the current starved VCO, consider the first stage of ring oscillator shown in Fig. 2.

$$C_{tot} = \frac{5}{2}C'_{ox}\left(W_pL_pW_nL_n\right) + C_{load} \quad (4)$$

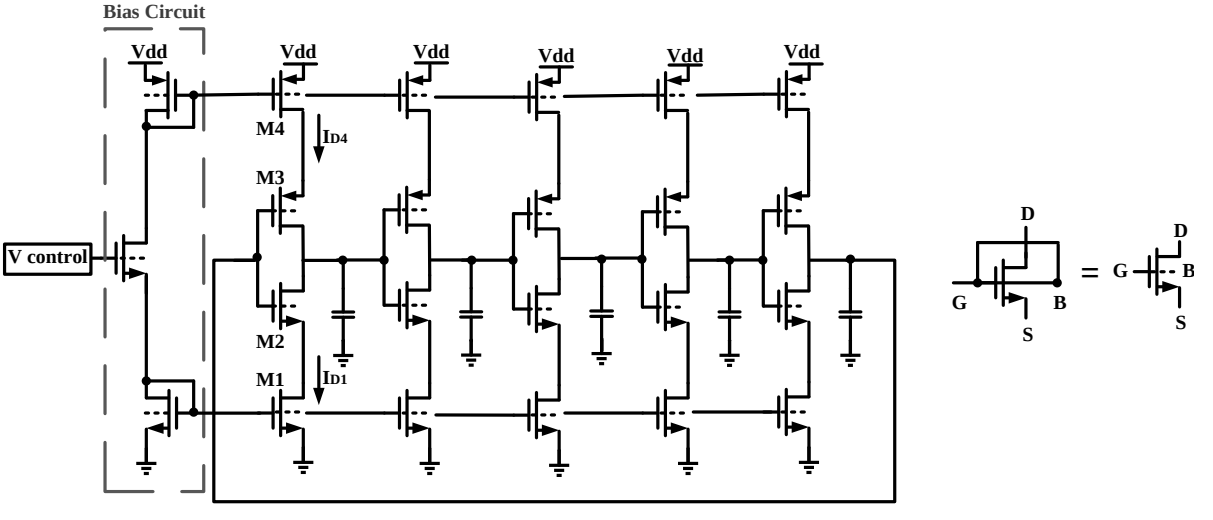

Fig. 2. Schematic of proposed current starved five-stage voltage-controlled single ended ring oscillator.

Where C'_{ox} is the oxide capacitance per area, W_p, L_p are the channel width and length respectively for PMOS and W_n, L_n are the channel width and length respectively for NMOS.

The time it takes to charge C_{tot} from zero to V_{SP} with the constant-current I_{D4} is given by:

$$t_1 = C_{tot}.\frac{V_{SP}}{I_{D4}} \quad (5)$$

Where V_{SP} is the switching point voltage. While the time it takes to discharge C_{tot} from V_{dd} to V_{SP} is given by:

$$t_2 = C_{tot}.\frac{V_{dd} - V_{SP}}{I_{D1}} \quad (6)$$

If $I_{D4} = I_{D1} = I_D$, then the sum of t_1, and t_2 is simply:

$$t_1 + t_2 = C_{tot}.\frac{V_{dd}}{I_D} \quad (7)$$

The oscillation frequency of the current starved VCO for N (an odd number > 5) of stages is:

$$f_{osc} = \frac{1}{N(t_1 + t_2)} = \frac{I_D}{N.C_{tot}.V_{dd}} \quad (8)$$

The average power dissipated by the VCO is:

$$P_{avg} = V_{dd}.I_D \quad (9)$$

5. SIMULATION RESULTS

The CS five-stage voltage-controlled single-ended ring oscillator with DTMOS technique is designed in sub-threshold region using TSMC 0.18µm RF CMOS technology with 0.4 V power supply and under 1pF load. The simulations are done in Agilent software Advanced Design System (ADS). The frequency of oscillation is 26.6 kHz at the control voltage of 0 V and the frequency of oscillation is 210.5 kHz at the control voltage of 0.4 V. Also the center frequency of the proposed VCO is 115.4 kHz. The VCO output waveform with 0 V control voltage and 0.4 V control voltage are shown in Fig. 3 and Fig. 4 respectively.

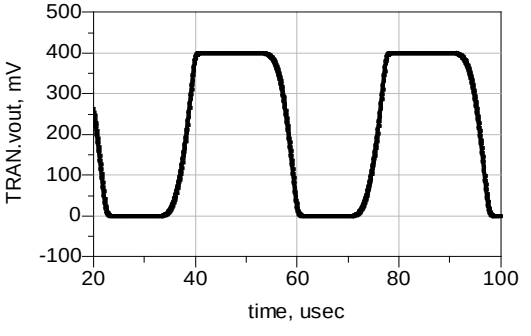

Fig. 3. Transient response of the VCO at frequency of 26.6 kHz.

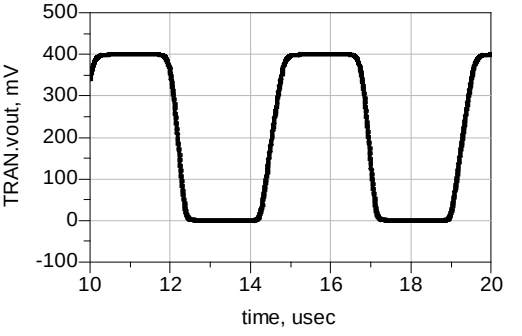

Fig. 4. Transient response of the VCO at frequency of 210.5 kHz.

The phase noise at a 100 kHz offset at the minimum (maximum) oscillation frequency is -120.5 dBc/Hz (-113.15 dBc/Hz) and shown in Fig. 5 and Fig. 6 respectively.

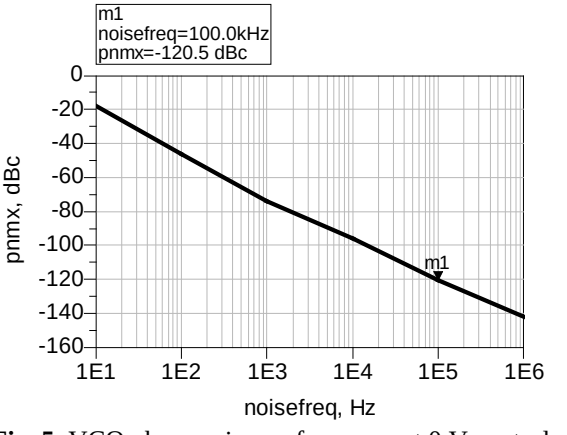

Fig. 5. VCO phase noise performance at 0 V control voltage.

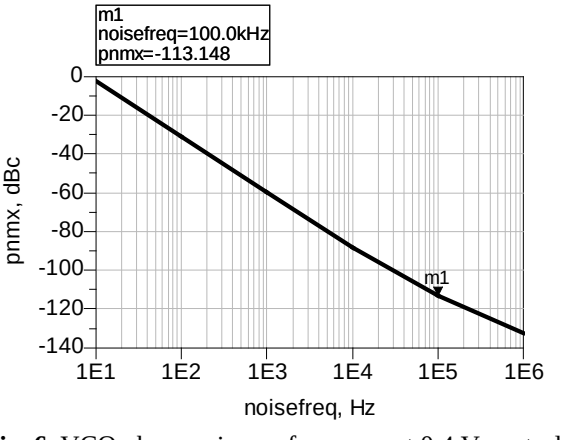

Fig. 6. VCO phase noise performance at 0.4 V control voltage.

The power consumption versus control voltage is shown in Fig. 7. The minimum and maximum power dissipation is respectively 6.42 nW and 8.62 nW.

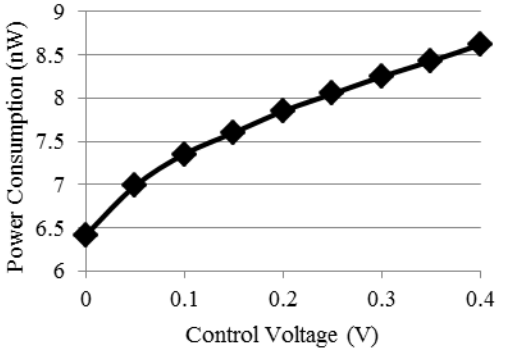

Fig. 7. Power consumption versus control voltage.

Fig. 8 shows the simulation result for output frequency versus control voltage characteristic of the proposed VCO.

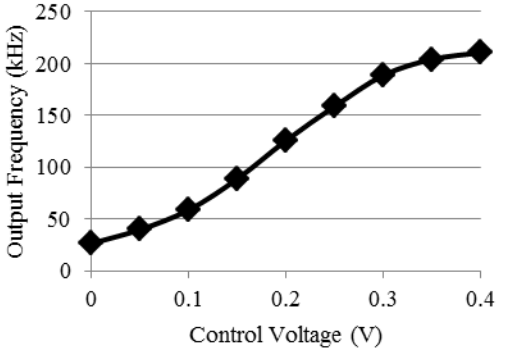

Fig. 8. Output frequency versus control voltage.

Fig. 9 shows the sensitivity of VCO power supply. When the power supply is changed from 0.3 V to 0.5 V, the minimum (maximum) frequency varies from 7.7 kHz to 71.7 kHz (83 kHz to 406 kHz).

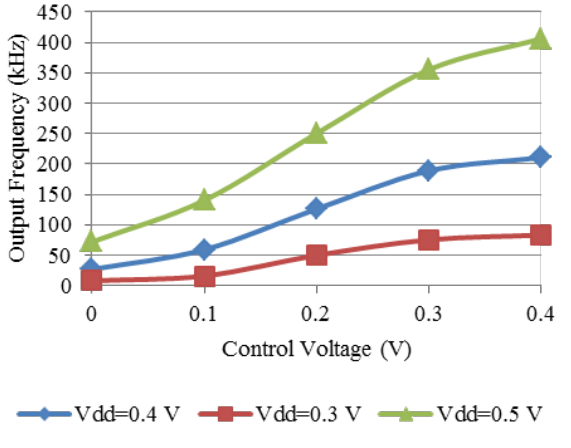

Fig. 9. Sensitivity of the VCO in function of the of the Power supply.

The variations of the output frequency with temperature are shown in Fig. 10. The temperature is changed from -55˚C to 80˚C; the minimum (maximum) frequency varies from 35 kHz to 20.5 kHz (225.3 kHz to 200.3 kHz).

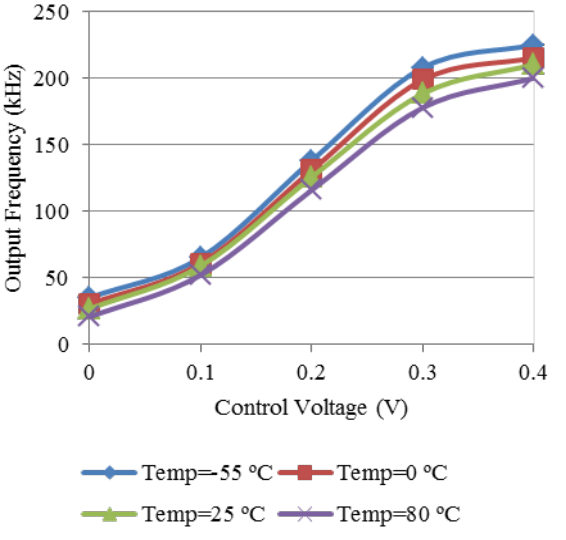

Fig. 10. Output frequency versus temperature variation.

The well-known figure of merit (FOM) for oscillator performance is described as [16]:

$$\text{FOM} = \cdots \\ \text{L}[\Delta\omega] + 10\log_{10}\left(\frac{P_{dc}}{1\ \text{mW}}\right) - 20\log_{10}\left(\frac{\omega_0}{\Delta\omega}\right) \quad (10)$$

Where, $\text{L}[\Delta\omega]$ is the phase noise below carrier $\Delta\omega$ is the offset frequency where phase noise is measured, ω_0 is the central frequency of oscillation and P_{dc} is the power consumption. This FOM is used to compare different voltage-controlled single-ended and differential ring oscillators, the comparison results are shown in Table 1.

6. CONCLUSION

In this paper current starved 5-Stage voltage-controlled single-ended ring oscillator is designed and simulated using TSMC 0.18µm RF CMOS technology with 0.4 V power supply. DTMOS technique is used to reduce the threshold voltage of MOS transistors which working at sub-threshold region. The output frequency ranges from 26.6-210.5 kHz with control voltages of 0 V to 0.4 V. Its power consumption at maximum output frequency is 8.62 nW. The phase noise at a 100 kHz offset at the maximum oscillation frequency is -113.15 dBc/Hz. These specifications are highly attractive for its use in ultra-low power ultra-low voltage and low

phase noise applications particularly in medical applications.

Table 1. Comparison of the VCO performance.

Design	Process (µm)	Power Supply (V)	Power (µW)	Frequency (MHz)	Offset Frequency (MHz)	Phase Noise (dBc/Hz)	FOM (dBc/Hz)
[4]	0.13	1.2	5100	6300-13900	1	-81.5	-142.5
[5]	0.18	0.5	85	120-1300	1	-72	-145
[6]	0.35	3.3	7010	200-2100	0.1	-90	-163
[7]	0.13	1.2	17000	180-5000	10	-118	-158
[8]	0.09	1	2	400-935	1	-65	N/A
This work*	0.18	0.4	0.00862	0.0266-0.2105	0.1	-113.15	-165

- Type of oscillators in [4], [8]: Single-ended ring
- Type of oscillators in [5], [6], [7]: Differential ring

***** The results are reported at 0.4 V control voltage

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