Modified Series Resonance Fault Current Limiter for Connection Distributed Generation to micro grid

M. M. Moghimian[1], M. Radmehr[2*], M. Firouzi[3]

Abstract – The integration of distributed generation (DG) and renewable energy sources (RES) into microgrids has significantly increased fault current levels, challenging system protection and stability. To ensure reliable operation while accommodating growing DG capacity, microgrids require advanced solutions to manage fault currents without compromising transient stability. Fault current limiters (FCLs) emerge as an effective solution to suppress fault currents, enhance protection coordination, and facilitate seamless microgrid operation during fault conditions. This paper proposes a modified series resonant fault current limiter (MSRFCL) designed for controllable fault current suppression in microgrids. The new topology addresses the limitations of conventional SRFCLs by integrating adaptive control capabilities, ensuring compatibility with microgrids' voltage sag conditions. To validate the proposed FCL's efficacy, comprehensive simulations were conducted in PSCAD/EMTDC, analyzing fault current mitigation, fault ride through performance and protection under varying microgrid scenarios.

Keywords: Micro Grids (MGs), Modified Series Fault Current Limiter (MSFCL), STATCOM, Wind Turbin e Generator (WTG)

1. Introduction

The growing integration of distributed generation (DG) systems in modern power networks has made microgrids (MGs) essential for safe and reliable DG operation [1]. However, increasing short-circuit currents - primarily caused by new DG integrations - pose critical challenges in grid-connected MGs [1, 2]. These elevated fault currents can cause equipment damage through excessive electromechanical stress, insulation failure, and dangerous over-voltage transients, ultimately threatening MG reliability [3]. While traditional solutions like equipment upgrades or grid reconfiguration exist, they often compromise system reliability or prove cost-prohibitive [3, 4]. Fault current limiters (FCLs) have emerged as superior alternatives, effectively limiting fault currents without modifying MG configuration or affecting normal operation [4, 5]. Three main FCL types have been developed: superconducting (SFCLs), resonant (RFCLs), and solid-state FCLs (SSFCLs) [6, 7]. SFCLs offer advantages like low loss and fast response but require expensive superconducting materials and cooling systems [8, 9].

SSSFCL provide fast response and controllability but generate high power losses due to flowing steady-state current from semiconductor switches. RFCLs, while cost-effective, can cause over-voltage and resonance issues in MGs [10]. The fundamental operating principle exploits the unique impedance characteristics of resonant circuits: series resonance creates minimal impedance (acting as a short-circuit) during normal operation, while parallel resonance generates extremely high impedance (behaving as an open-circuit) during fault conditions. These properties make resonant circuits particularly suitable for fault current limitation applications. The critical design challenge lies in developing effective switching mechanisms that can transition between these impedance states - from low to high impedance for series resonant FCLs during fault conditions. Also, transition conversely from high to low impedance for parallel resonant FCLs during normal operation. This transition must occur rapidly and reliably to ensure proper system protection. Different RFCLs have been developed to address this impedance transition requirement, each with distinct advantages and limitations regarding response time, reliability, and impact on system operation. Authors in Ref [11], proposes series resonant FCL controlled by a mechanical switch to alternate between near-zero impedance and current-limiting XL due to capacitor-bypassed during faults as shown in Fig. 1(a). However, its protection capability is limited by the switch's slow response to short-circuits. Reference [12] introduces a hybrid resonant FCL topology that integrates both series (Ls-Csp) and parallel (Csp-Lp) resonant circuits as

1, 2* Department of Electrical Engineering, AK. C., Islamic Azad University, Aliabad Katoul, Iran. E-mail: Mohammadmehdi.moghimian@iau.ac.ir

3 Department of Electrical Engineering, AK. C., Islamic Azad University, Abhar, Iran

*** Corresponding Author** : m_radmehr@aliabadiau.ac.ir

Received: 2025.07.30; Accepted: 2025.09.20

demonstrated in Fig. 1(b). Under normal operating conditions, current flows through the series LC path, exhibiting near-zero impedance characteristics. During fault events, thyristors (T1/T2) are triggered to activate the parallel resonant branch, creating high impedance for effective current limitation. Reference [13] presents a hybrid FCL combining a diode bridge (D1-D4, IGBT, Ld) for near-zero impedance normal operation and a damped parallel resonant branch (Lp-Cp-Rsh) for fault current limitation, achieving fast (<1ms) switching via IGBT control and effective oscillation damping through Rsh. The design reduces costs by employing dry-type capacitors and maintains grid stability with minimal PCC voltage sag during faults. However, it requires precise fault detection and complex control coordination between the bridge and resonant sections, while semiconductor devices face significant stress during resonant operation. Reference [14] introduces a series resonance bridge-type FCL that combines compensation capacitors and surge arresters to limit fault currents while maintaining cost efficiency (no superconducting components).

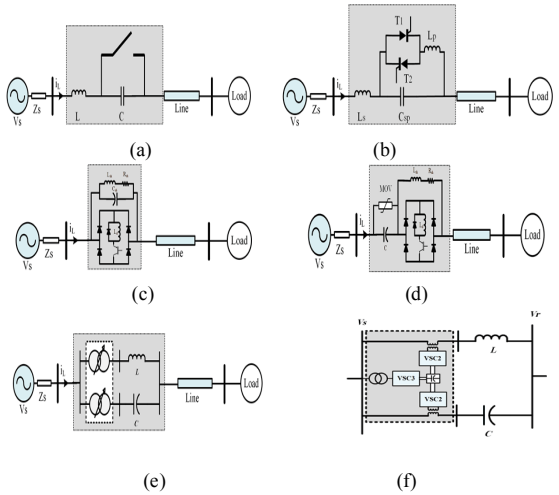

Fig.1: RFCLs proposed, (a) Ref [11], (b) Ref [12], (c) Ref [13], (d) Ref [14], (e) Ref [15], (f) Ref [16]

During normal operation, current flows through the capacitor

and closed diode bridge, switching to a resonant path (via inductor discharge) upon fault detection. The integrated surge protection ensures stable current clamping, with fast semiconductor switching enabling rapid transition between operational modes. Fig. 1(e) illustrates the Interphase Power Controller (IPC) structure, comprising passive components (reactors, capacitors) and phase-shifting transformers (PSTs). Developed by CITEQ [15], this series-type power flow controller was specifically designed to overcome limitations of high short-circuit levels while operating at fundamental power system frequency. Reference [16] addresses IPC limitations by introducing three voltage-source converters (VSC) as shown in Fig. 1(f), forming the Unified IPC (UIPC). This power electronics-enhanced version maintains all IPC functionalities while improving dynamic response and control flexibility. Reference [17] introduces a series RFCL (SRFCL) incorporating a metal-oxide varistor (MOV) connected in parallel with the resonant capacitor. It has simple and cost effective configuration, which effectively limits fault current with automatic operation. However, it is very sensitive to MOV voltage threshold selection where improper calibration can compromise limiter performance. To address these constraints, this work proposes an enhanced controllable series resonant FCL (CSRFCL) topology that replaces the passive MOV with an active IGBT-based switching module.

2.Controllable SRFCL

Fig. 2(a) demonstrates the schematic circuit of the MOV-controlled SRFCL. As illustrated, a MOV is connected in parallel with capacitor C. During normal operation, the MOV remains inactive below its preset voltage protection threshold (VTH). When a fault occurs, the capacitor voltage (VC) rises until reaching VTH, activating the MOV nonlinear resistance characteristic to limit the short-circuit current. The MOV must withstand energy absorption for several cycles until circuit breaker operation. By clamping VC, the capacitor current (iC = C dVC/dt) is consequently limited. This dual-action protection mechanism provides automatic fault response without requiring external control signals. While the MOV-parallel capacitor configuration effectively reduces fault currents [17], this approach exhibits two following critical limitations:

1) inherent inability to actively control current magnitude, and
2) Sensitivity to MOV voltage threshold selection where improper calibration can compromise limiter performance.

To address these constraints, we present an improved controllable SRFCL featuring, replacement of passive MOV with active IGBT-R pair (T1/T2 with series resistance), dynamic impedance adjustment via pulse-width modulation (PWM) control and Real-time fault current regulation capability. As shown in Fig. 2(b), the proposed CSRFCL comprises as following components:

- Two anti-parallel IGBTs (T1/T2) in series with current-limiting resistor (R)
- Gate drive circuitry for precise switching control
- Fault detection system with adjustable current thresholds

This modification introduces three key advantages:

3) Precise current regulation through gate signal control
4) Adaptive fault response independent of fixed voltage thresholds
5) Dynamic impedance adjustment for optimal limitation across fault types

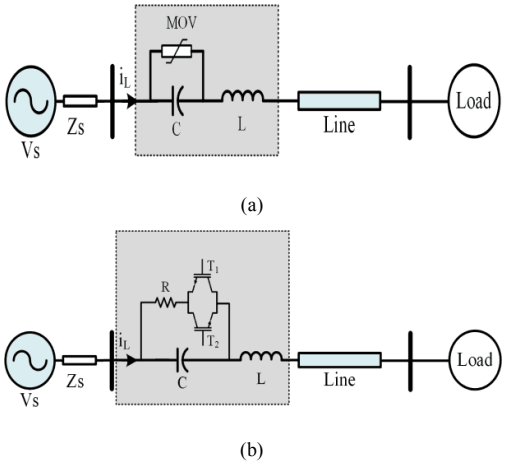

Fig. 2: power circuit, (a) MOV-Controlled RFCL [17], (a) (b) CRFCL

2.1 Principle Operation of CRFCL

Considering Fig. 2(b), the proposed CSRFCL structure employs two anti-parallel switches (T_1 and T_2) in series with a resistor, replacing the MOV. Under normal grid conditions, both T_1 and T_2 remain in the off state, blocking current flow. However, upon fault detection, the control system dynamically adjusts the effective resistance by activating the switches and regulating their switching duration, as determined by the following equation:

$$R_D = \frac{R}{D} \qquad (1)$$

In (1), R represents the limiting resistor connected in parallel with the capacitor, and D denotes the duty cycle of switches T_1 and T_2 . By introducing a variable resistance RD, controlled by the duty cycle D, a variable impedance is achieved. This impedance is derived from the following equation:

$$Z_{FCL} = jX_L - \frac{jR_DX_C}{R_D - jX_C} \qquad (2)$$

Fig. 3 demonstrates the CRFCL Impedance characteristics of the CRFCL based on duty cycle of the anti-parallel IGBTs switching. The switching time modulation of the IGBT switches alters the impedance characteristics of the current limiter. Fig. 3 illustrates the controllable impedance characteristics of the limiter for the parameter values L = 0.5 H, C = 10.13 mF, and R = 20 Ω. In this figure, the duty cycle D (of switches T_1 and T_2) varies from D = 0.01 to D = 0.99. As observed, increasing the duty cycle from D = 0.01 to D = 0.99 causes the impedance magnitude to rise from nearly 0 Ω to approximately 30 Ω, while the impedance phase angle increases from 0° to 70°.

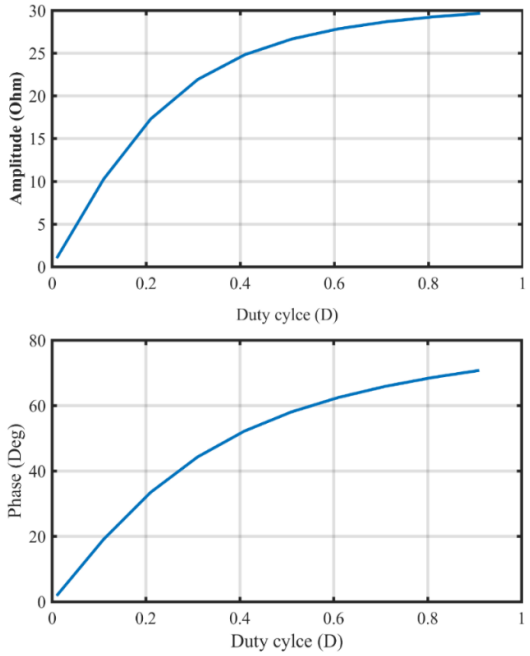

Fig. 3: CRFCL Impedance characteristics

2.2 Control System

To ensure optimal performance of the IGBT-based controllable series resonant FCL (T1/T2 with series resistance), a fast and adaptive control system is essential. Considering the use of switches T1 and T2 in the CRSFCL, to control the limiter performance, a suitable control system is required to detect the fault and determine the appropriate value of the duty cycle D to create the appropriate impedance according to the fault conditions and voltage drop in the network. Considering the use of this structure in a microgrid to improve the voltage drop transition conditions, the control system must have the following conditions:

1- Rapid fault detection plays an effective role in improving stability and preventing further voltage drop at the DG connection point. Therefore, the proposed control system should detect the fault in the shortest possible time

and introduce the limiter into the network.

2-The control system must be able to ensure that in asymmetrical short-circuit fault conditions, the CSRFCL operation does not affect other phases and only the phases that have a fault enter the network.

3- The control system must be designed in such a way that it is capable of creating a variable resistance and, as a result, a variable impedance.

According to the above, in order to detect the fault and control the D value of switches T1 and T2 of the CSRFCL during the fault, a voltage-based control system is used in each phase. In this control system, which can be seen in Fig. 4, the dq component of each phase of the connection voltage (voltage Vs) is selected as the fault detection signal and D value control.

In this study, to detect the fault and turn off the switches T1 and T2 in the faulty feeder, first the dq component of the connection voltage Vs is calculated. Then the value of Vdq in each of the phases a, b, c is composed of two components Vq and Vd, where the Vd component is the instantaneous component and Vq is the perpendicular component of the Vs in each of the phases a, b, c. To create the Vq component of the voltage, a delay time T/4 is applied to the Vd component. Then the Vdq component of the voltage Vs is obtained from the following equation:

$$V_{dq}^{abc} = \sqrt{(V_d^{abc})^2 + (V_q^{abc})^2} \qquad (3)$$

After computing the Vdq component for each phase (a, b, c), it is compared with the reference voltage (Vref) in the respective phase. When Vdq falls below Vref, the control system identifies a fault and activates switches T_1 and T_2 in the affected feeder, thereby inserting the limiting resistor into the circuit. To determine the optimal duty cycle (D) for generating an impedance proportional to the voltage sag level at the connection point, the Vdq component is compared with a sawtooth waveform of frequency fs. Based on the magnitude of the voltage sag, the control system generates the appropriate D. To ensure the control system operates exclusively during fault conditions, a logical AND gate is employed. This ensures that the computed D is applied to the limiter only under short-circuit faults with voltage sags. During normal grid operation, switches T_1 and T_2 remain in the off state.

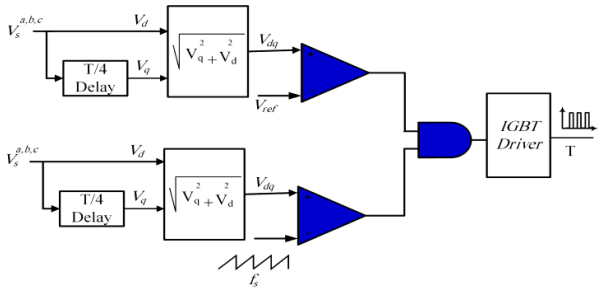

Fig. 4: CSRFCL control system

3. Simulation Results

In this study, simulation tests were conducted using PSCAD/EMTDC software. To analyze the performance of a 2MW-DFIG connected to microgrid under symmetrical three-line-to-ground (3LG) fault for low and severe voltage sag conditions. They were applied to connection line 2, as illustrated in Fig. 5. The fault initiation occurs at t = 10s and persists for 7.5 cycles (0.15s). This fault duration is significantly shorter than the timescale affecting wind speed transients, therefore the wind speed is maintained constant at 16 m/s. To demonstrate the effectiveness of the CSRFCL, three distinct cases were simulated for 3LG faults under both low and severe voltage sag scenarios:

Case 1: System without FCL protection
Case 2: System equipped with conventional SRFCL
Case 3: System incorporating the proposed CSRFCL

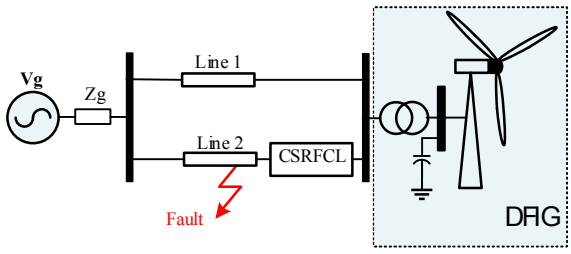

Fig. 5: study system

3.1 Scenario 1: Severe Voltage Sag Condition

Fig. 6 presents the RMS voltage at the DFIG point of common coupling (PCC) during a three-phase-to-ground (3LG) fault for the three investigated cases. As shown in this figure, the PCC voltage drops to 0.01 pu, 0.75 pu and 0.8 pu for Cases 1, 2 and 3, respectively. Fig. 7 illustrates the DFIG output power during a short-circuit fault for all three operational cases. As shown in the figure, in Case 1 the output power drops to 0.1 pu due to the voltage sag at the PCC. After fault clearance, the power oscillates transiently, peaking at 1.2 p.u. before stabilizing to its pre-fault value. In Case 2, the power output is stabilized during

the fault, limiting the reduction to 0.5 p.u. without complete collapse. However, by employing the CSRFCL, both the power reduction during faults and the resulting oscillation amplitudes are significantly mitigated.

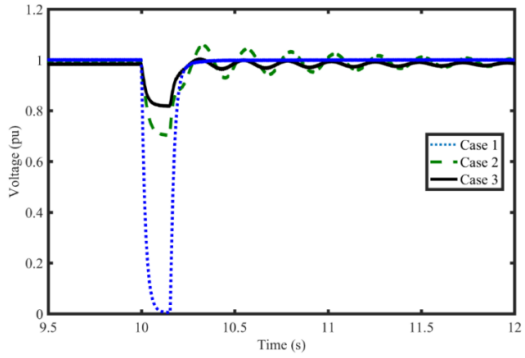

Fig. 6: PCC Voltage

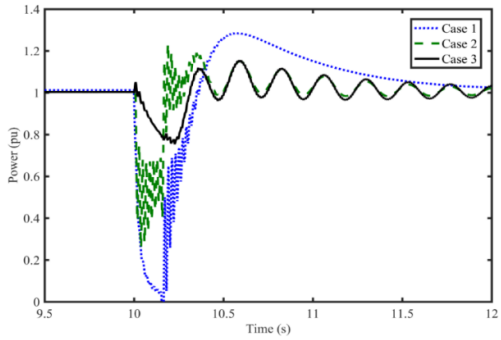

Fig. 7: Output power

Figures 8(a), 8(b), and 8(c) respectively display the rotor current for Case 1, Case 2, and Case 3. As observed in these Figures, the rotor current surges to approximately 4 p.u. in Case1 followed by transient oscillations before returning to its pre-fault value During fault conditions. In Case 2, the rotor current amplitude is effectively limited to 2 p.u. during the fault. With the CSRFCL implemented in Case 3, the rotor current remains nearly unchanged, demonstrating superior fault current mitigation. Figures 9(a), 9(b), and 9(c) illustrate the power DFIG output current for Case 1, Case 2, and Case 3, respectively. The analysis reveals that in Case 1, upon fault occurrence, the rotor current surges to approximately 4 p.u. The system experiences sustained oscillations before returning to pre-fault conditions. In Case 2, the rotor current amplitude is effectively limited to 2.1 p.u. during the fault. Also, represents a 47.5% reduction compared to Case 1. In Case 3 , The current amplitude variations are maintained within ±0.15 p.u. of nominal. In addition, demonstrates 96% improvement in stability compared to Case 1.

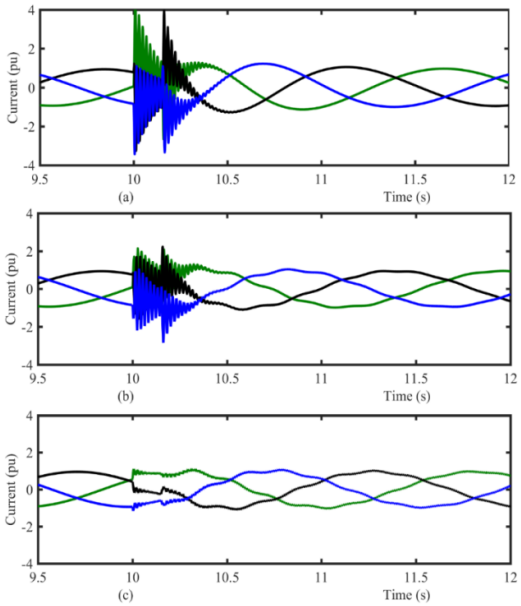

Fig. 8: rotor Current for, (a) Case 1, (b) Case 2 and (3) case 3

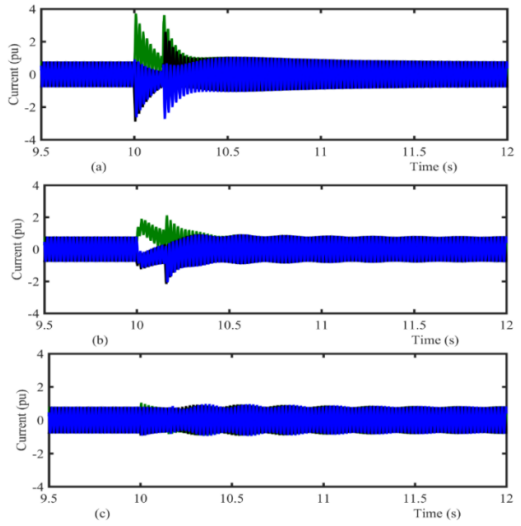

Fig. 9: Stator Current for, (a) Case 1, (b) Case 2 and (3) case 3

3.2. Scenario 1: Low Voltage Sag Condition

In this section, to demonstrate the effectiveness and comparison of the use of the CSRFCL and a MOV-equipped SRFCL, low voltage drop conditions are modeled. Therefore, a 3LG fault at time t=10s on line 2 is simulated for a fault resistance Rf=5Ω according to Fig. 5. Fig. 10 displays the RMS voltage values at the PCC during fault conditions across all test cases. In the unprotected system (Case 1), the PCC voltage drops to 0.8 pu, creating a severe voltage sag condition for the DFIG. When employing the

MOV-SRFCL (Case 2), the voltage drop improves to 0.85 pu, while the CSRFCL (Case 3) demonstrates superior performance by maintaining the voltage at 0.9 pu. Fig. 11 show the output power of DFIG for all cases. The power output characteristics reveal significant differences between cases. Both the unprotected system and MOV-SRFCL configuration experience power reduction to approximately 0.7 pu, whereas the CSRFCL maintains output at 0.9 pu during the fault while simultaneously reducing oscillation amplitudes. This enhanced performance is further evident in the rotor current behavior shown in Fig.12 (a)-(c). The unprotected system (Case 1) exhibits a current surge to 0.5 pu followed by sustained oscillations before eventually stabilizing. The MOV-SRFCL (Case 2) successfully limits the current amplitude to 2 pu, while the CSRFCL (Case 3) maintains near-nominal current conditions throughout the fault event, demonstrating exceptional stability and control.

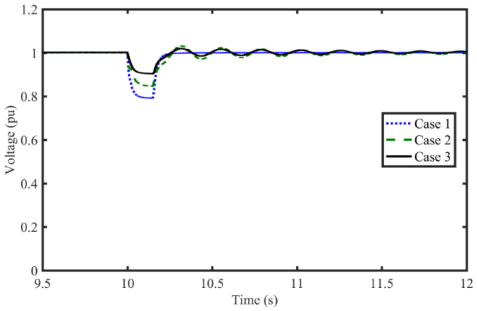

Fig.10: PCC voltage for all cases

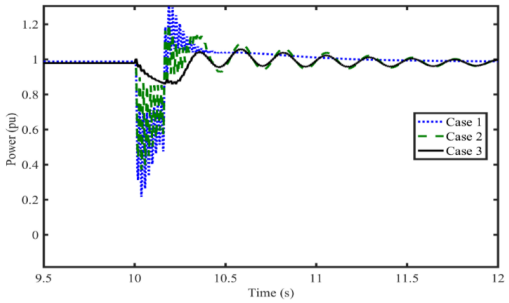

Fig.11: Output power for all cases

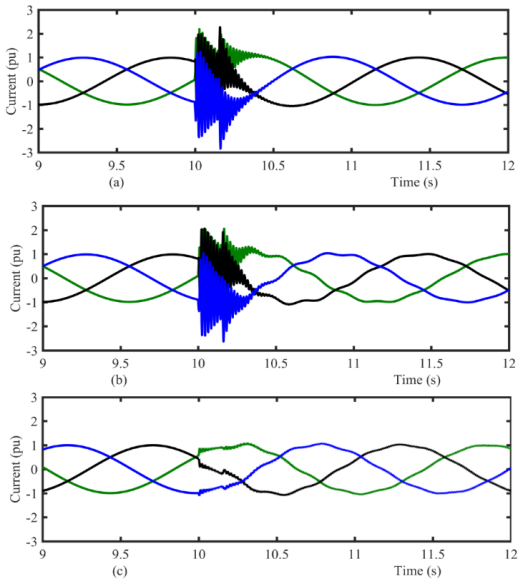

Fig.12: Rotor current for all cases

4. Conclusion

This paper investigates the effectiveness of CSRFCL in protecting DFIG. The study examines system performance under both symmetrical and asymmetrical fault conditions through PSCAD/EMTDC simulations, with comparative analysis between the proposed controllable CSRFCL and conventional MOV-based SRFCL. Considering simulation results, key findings include:

The CSRFCL reduces fault current injection into the grid while maintaining PCC voltage at 0.85 p.u. (three-phase faults) and 0.95 p.u. (single-phase faults), satisfying voltage ride-through requirements.

Its variable impedance characteristic dynamically compensates for voltage sags, unlike fixed-impedance MOV limiters.

Significant mitigation of rotor overcurrents (up to 47% reduction) during faults, which prevents damage to RSC power electronics and ensures system reliability.

Both SRFCLs types perform comparably under severe voltage sags (>50% drop). The CSRFCL demonstrates superior performance during moderate sags (20-50% drop), maintaining 12-15% better voltage stability through adaptive impedance adjustment.

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