Islamic Azad University

Journal of

Optoelectronical Nanostructures

Volume 10, Issue 1, Spring 2025, page 44-59

IRANIAN SOLAR ENERGY SCIENTIFIC SOCIETY

Research Paper

A Novel Design of an Active Low 2:4 Decoder using Quantum-dot Cellular Automata

Reza Pourtajabadi[1], Maryam Nayeri*[,1], Mohamad Reza Shayesteh[1]

[1]Department of Electrical Engineering, Yazd Branch, Islamic Azad University, Yazd, Iran

Received: 2024.03.29
Revised: 2025.01.21
Accepted: 2025.03.10
Published: 2025.05.05

Use your device to scan and read the article online

Keywords:
Quantum-dot cellular automaton, Majority voter gate, Active low decoder, Combinational circuit, Coplanar architecture

Abstract

Quantum-dot cellular automata (QCA) is a nanoscale technology with unique features compared to the silicon-based technology that has been recently used in the design of combinational and sequential logic circuits. Today, QCA is a well-known technology for the design of digital systems and provides a modern pattern for information processing and communication with higher speed, higher integration scale, higher switching frequency, and less power consumption compared to silicon-based technology. In this paper, the QCA technology is used to design an active-low 2:4 decoder using an active-high decoder. The initial scheme is optimized and an independent active-low decoder is presented. In the optimized structure, the number of cells, and the occupied space are decreased significantly followed by power consumption reduction and an increase in the output signal level compared to the initial scheme. The number of required clock phases to generate the output is also reduced to three. Design and simulation are carried out in QCA Designer.

Citation: Reza Pourtajabadi, Maryam Nayeri, Mohamad Reza Shayesteh. A Novel Design of an Active Low 2:4 Decoder using Quantum-dot Cellular Automata. **Journal of Optoelectronical Nanostructures.** 2025; 10 (1): 44-59

***Corresponding author:** Maryam Nayeri
Address: Department of Electrical Engineering, Yazd Branch, Islamic Azad University, Yazd, Iran
Email: nayeri1399@gmail.com
DOI: https://doi.org/10.71577/jopn.2025.1210151

1. INTRODUCTION

Today, moving towards nanotechnology is inevitable due to CMOS limitation constraints. Although reducing the dimensions increases the computational power, results in some problems, including the internal connections due to dimension miniaturization, high leakage current, and inefficient power distribution [1]. So, semiconductor-based transistors are hard to miniaturize. considering the supply voltage reduction, power loss resulting from leakage current and internal connections is a great challenge for transistor circuits. Thus, nanotechnology is an alternative solution to resolve these problems [2-5]. After introducing QCA in 1993 [6], various devices were developed using this technology. Recent studies show that QCA can achieve high switching speed, high-density circuits, and operation at room temperature [7]. The developments of modeling using Spice and verification of QCA capabilities indicate the continuous attractiveness of this technology. Recently, various molecular QCA models have been implemented, and their power is analyzed [8].

Among the practical applications of quantum dots technology, we can mention such as highly efficient photovoltaic solar cells [9], optoelectronic devices – lasers [10], optical amplifiers [11], single-photon sources [12], and photo detectors [13].

In this technology, computations using cellular automata are based on an array of quantum-dot devices. QCA is not the only nanoscale solution to resolve these problems, and it provides novel techniques for computations and data transmission [14].

The QCA technology is a tool for presenting the binary information of the cell that does not have current flow and the device operates by coupling the cells as a result of an electromagnetic field. Based on the unique property of this technology, logical states are not stored like the conventional electronic industry, but they are presented by a nanoscale cell that can encode data regarding the position of the electrons. QCA transmits data using the clocking technique that operates based on increasing or decreasing the tunneling barrier [15].

This paper is given the following structure: Section 2 describes the first principles of QCA. A decoder is presented in Section 3. Section 4 presents the proposed active-low QCA decoder and its optimal scheme. Section 5 presents the simulation results and examines the performance of the decoder. Finally, the paper is concluded.

2. PRINCIPLE OF QCA

A cell is required to construct QCA devices. Each cell is comprised of a nanoscale square structure including four quantum dots at four corners and two free

electrons [16]. The electrons cannot tunnel between neighbour cells, while they can tunnel between the adjacent points of a cell. Inserting two electrons in one cell results in Columbic interaction as a result of which the two electrons are configured diagonally with maximum distance from each other. The square QCA cell has only two diameters indicating two steady states of the electron configuration, called the electron polarization. Fig. 1 shows two possible configurations of QCA cell with stable polarization of P=+1 and P=-1, indicating the logic "1" and "0".

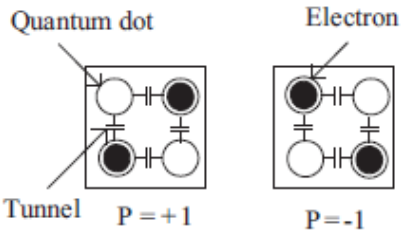

Fig. 1. QCA cell polarization

A. QCA IMPLEMENTATION TECHNIQUES

There exist four distinct classifications of QCA cells, contingent upon the materials employed in their construction.

1) METAL QCA

The metallic QCA cell is comprised of four aluminum dots designated as D1 through D4, which are interconnected via aluminum oxide tunnel junctions and associated capacitors [17]. The dots E1 and E2 function as Single Electron Transistor (SET) electrometers for the purpose of output detection. An illustration of the cell is provided in Fig. 2 [18]. The metal-based QCA latch has been realized and showcased in Reference [19], where it was operated at a temperature of 70mK.

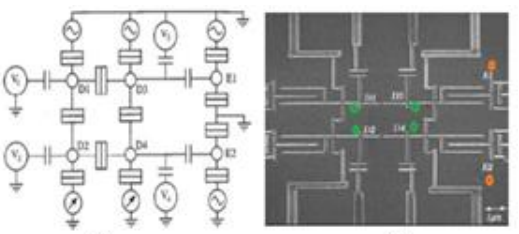

Fig. 2 Metal QCA cell (a) a streamlined schematic representation of a four-dot metal QCA cell (b) scanning electron microscopy image of the aforementioned QCA cell [18]

2) MOLECULAR QCA

Molecular QCA is regarded as a highly promising approach for the realization of QCA circuits. This technology functions effectively at ambient temperature while exhibiting a high device density and rapid operational speed. The configuration of the Molecular QCA cell is delineated in Reference [20]. The encoding of binary information occurs through specific charge arrangements. The representation of the Molecular QCA cell is illustrated in Figure 3 [21].

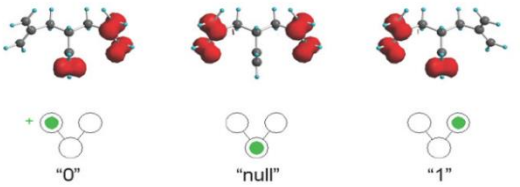

Fig. 3. Three states of six dot molecular QCA [21]

3) SEMICONDUCTOR QCA

Semiconductor materials like InAs/GaAs and GaAs/AlGaAs are employed in the production of quantum dots [22]. QCA cells can be constructed utilizing the same cutting-edge complementary metal-oxide-semiconductor (CMOS) technology that utilizes these semiconductor materials. The polarization of a cell is contingent upon the distribution of charge, and the computational process occurs through the interaction or coupling between a cell and its adjacent cells.

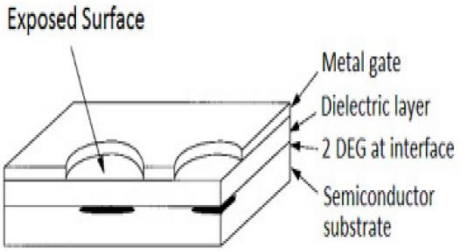

Fig. 4. The physical representation of the semiconductor QCA cell

4) Magnetic QCA

The magnetic realization of QCA was introduced by Cowburn and Welland [23]. A nanomagnet, comprising a singular circular nanodot, serves as the QCA cell. These nanodots, constructed from magnetic supermalloy, are arranged in a linear

configuration, and an oscillating magnetic field is applied to the dot. The magnetic QCA cell demonstrates functionality at ambient temperature. An illustration of a three-input majority gate within the magnetic QCA framework is presented in Fig. 5.

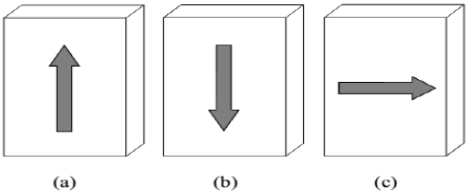

Fig. 5. Binary logical representation within magnetic QCA. (a) Logical state '1', (b) Logical state '0', and (c) Absence of state

B. QCA Majority Logic Gate

The QCA structures are formed by configuring the cells beside each other. A wire is formed by putting cells one after the other. QCA cells tend to spend a minimum amount of energy on each other. Therefore, the adjacent cells influence each other and the input signal propagates to the output and each cell tracks the polarization wire of its previous cell, considering the cell configuration. Signal transmission via binary wire is shown in Fig. 6. Unlike other devices, QCA wires have a very low energy loss, because no electric current passes the cells [24].

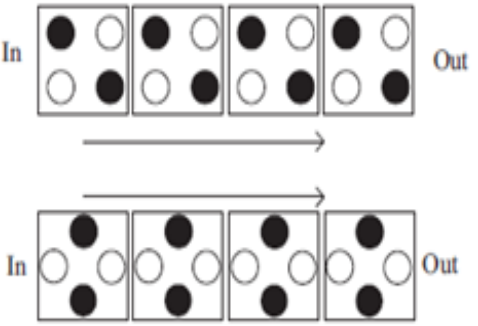

Fig. 6. Signal propagation in binary wires

Fig. 7 shows the inverter gate used in this study. This gate converts binary "1" to "0" and vice versa.

The main element in the QCA circuits is the three-input majority voter gate, which is shown in Fig. 4 and is described by Equation (1). The majority logic based on the induction method can reduce the time constraint and complexity of the QCA circuit [25].

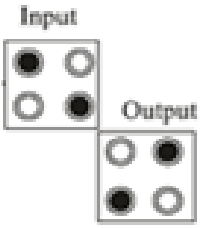

Fig. 7. Cell inverter gate

The three-input majority value affects the polarization of the central cell and generates an output. To implement the above gate in CMOS technology, 26 resistors are required, but in QCA technology, the MV[1]3 gate can be implemented by 5 cells. As shown in Fig. 8, using the majority voter gate, two-input AND gate and two input OR gate are achieved. To construct the AND gate, one input is fixed to "0" like Eq. (2), and to construct the OR gate, one input is fixed to "1" as in Eq. (3).

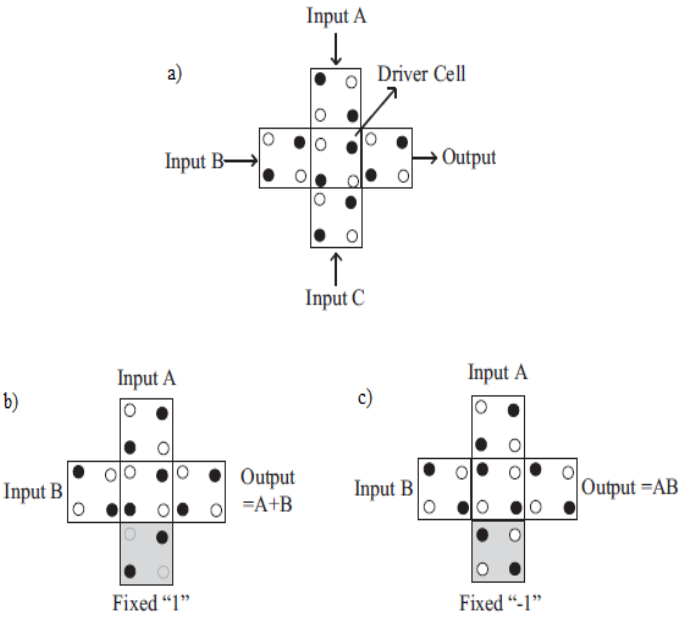

Fig. 8. a) Majority voter gate. b) OR gate. c) AND gate

[1] Majority voter gate

$$M(a,b,c) = ab + ac + bc \quad (1)$$
$$M(a,b,0) = AND(a,b) = ab \quad (2)$$
$$M(a,b,1) = OR(a,b) = a + b \quad (3)$$

The QCA circuits are divided into four sections that are excited and set up by four phases of the clock signal. As shown in Fig. 9, each clock has a phase difference of 90 degrees with the subsequent clock. In each area, the clock has four states, including high, high to low, low, and low to high. In the high to low state, the cell starts calculation, and in the low state, the cell value is fixed. When the clock phase changes from low to high, the cell loses its value, and in the high state, the cell is inactive [26]. The cell in each area demonstrates a behaviour similar to a latch.

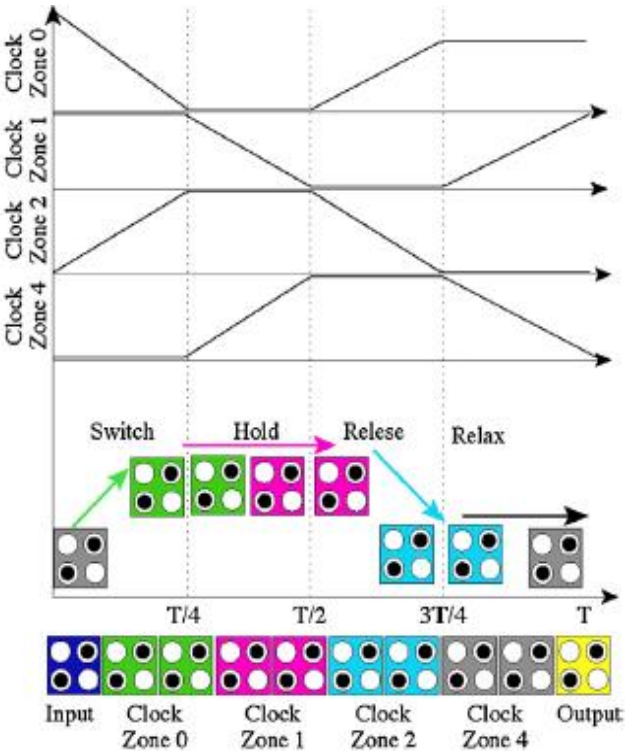

Fig. 9. QCA clocking

3. DECODER

Decoders play an essential role in computer architecture. They are used in different sections like RAM[1] or lookup tables [27]. A decoder is a device that selects one of the output lines after activation. Most decoders have n inputs and 2^n outputs. Decoding is essential in applications like multiplexing, 7-segments, and memory address decoders.

The block diagram of an active-low 2:4 decoder is shown in Fig. 10. In this diagram, four AND gates and six inverter gates are used; an inverter gate is inserted at the output of each AND gate. The outputs O_1 to O_4 of the decoder are obtained based on Eq. (4) to Eq. (7).

$$O_1 = \overline{A'B'} \tag{4}$$

$$O_2 = \overline{A'B} \tag{5}$$

$$O_3 = \overline{AB'} \tag{6}$$

$$O_4 = \overline{AB} \tag{7}$$

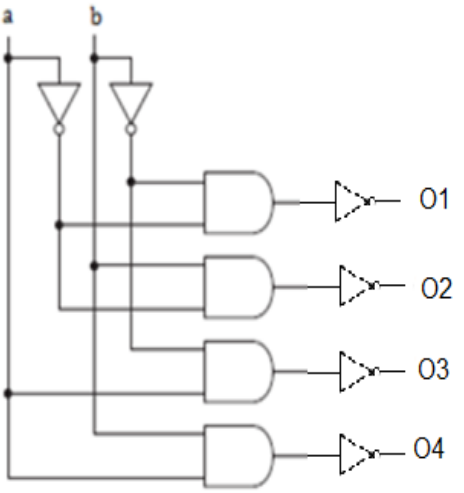

Fig. 10 Active low 2:4 decoder block diagram

1 Random access memory

Table I also represents the true table of the active-low decoder.

TABLE I
TRUTH TABLE OF AN ACTIVE HIGH 2:4 DECODER.

Input		Output			
A	B	O4	O3	O2	O1
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	1

4. PROPOSED DECODER

In this scheme, four MV3 gates are used. One input of each majority voter fate is fixed on logic "0" with P=-1, as a result of which it operates like an AND gate. To invert the input A at MV3 1 and 2 and invert the input B at MV3 1 and 3 (according to Table I), two-cell inverter is used that reduces the number of cells and the occupied area of the circuit. To invert each output, a two-cell inverter is inserted at the output of each majority voter gate.

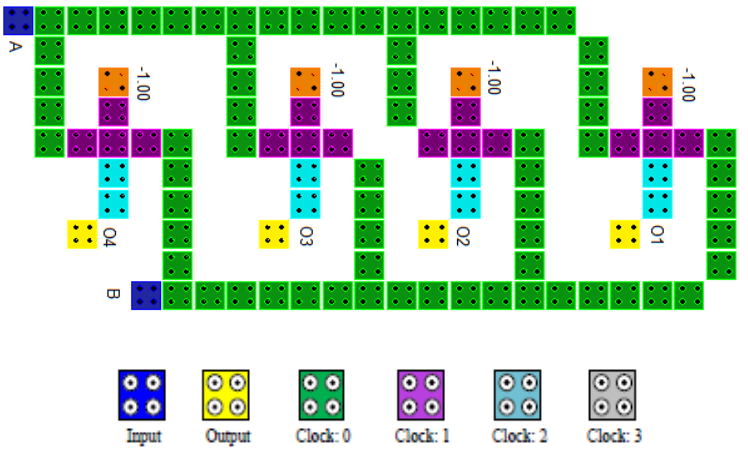

Fig. 11 First proposed circuit of a 2:4 active low decoder

The maximum number of cells in one clock area of the proposed circuit is 21, and the number of QCA cells of the proposed circuit is 102. Fig. 11 shows the initial circuit.

Since inserting an inverter gate at the output of each MV3 reduces efficiency, increases power consumption, increases the number of cells and occupied area, and reduces the output signal level. In the optimized circuit, without inserting an inverter gate at the output of each MV gate and by changing the polarization of the fixed cell, all four MV3 gates of the corresponding active-high decoder change from P=-1 to P=+1 and the binary value changes from "0" to "1", and finally the AND gates are converted to OR gates. The optimal active-low decoder is shown in Fig. 12.

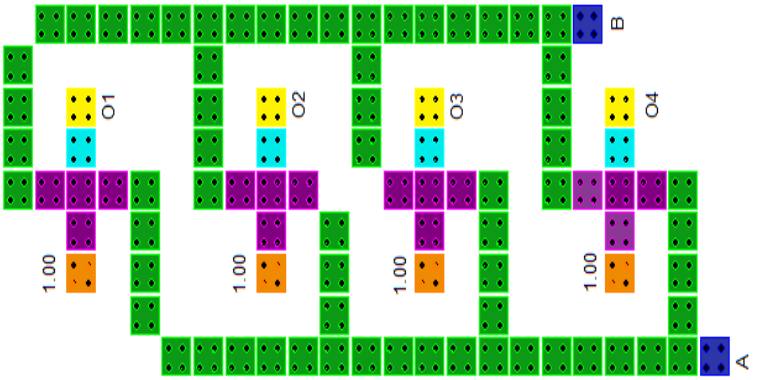

Fig. 12 Optimized circuit of a 2:4 active low decoder

5. RESULT AND DISCUSSION

The proposed circuit is comprised of 94 cells, demonstrating an 8% reduction compared to the initial scheme. Reducing the number of cells reduces the occupied area of the circuit, increases the output signal level, and decreases the power consumption. The occupied area and the output signal level of the optimized circuit are improved by 20% and 40%, respectively compared to the initial structure. Fig. 13 shows the simulation results of the optimized active-low decoder. The output of this circuit is generated after three clock phases. According to the simulation results, for each input, only one of the outputs is "0" and the other outputs are "1", demonstrating the correct operation of the circuit.

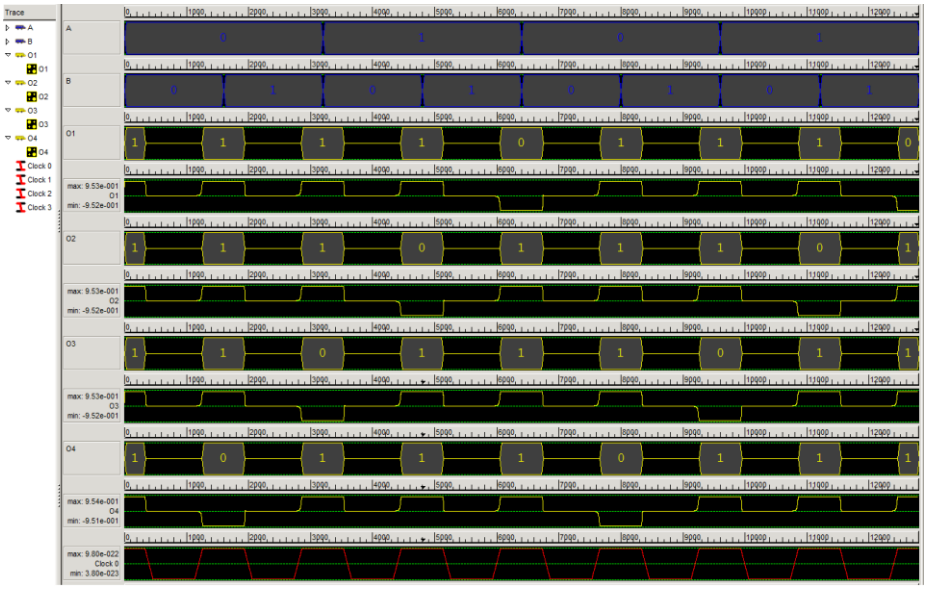

Fig. 13 Simulation result of the optimized circuit

Table II compares the proposed method and the scheme presented in Ref [28-30]. Comparison is made based on the number of cells, occupied area, number of gates, and number of clock phases to generate output, indicating improved performance compared to the previous scheme.

TABLE II

COMPARISON BETWEEN THE PROPOSED CIRCUIT AND REF [25-27]

	Proposed Circuit	First Proposed in[28]	Second Proposed in [28]	Proposed in[29]	Proposed in[30]
Cell Count	94	110	159	212	137
Area Covered (um^2)	0.082	0.13	0.177	0.25	0.15
Number of Gate	4	4	4	6	4
Clock Phases	3	3	3	6	5

Table III shows the percentage improvement achieved in term of Cell count and Area Covered compared to previous schemes in Ref [28-30].

TABLE III
PERCENTAGE IMPROVEMENT COMPARED TO REF. [25-27].

	First Proposed in[28]	Second Proposed in [28]	Proposed in[29]	Proposed in[30]
Cell Count	15	40	55	31
Area Covered	37	53	67	45

6. CONCLUSION

Decoding and encoding play an essential role in communication systems. In this paper, first, a new active-low 2:4 decoder is designed using QCA technology. Then, it is optimized considering the QCA characteristics. In the optimized circuit, the number of cells is reduced as a result of which the occupied area on the chip and the power consumption is reduced. Another characteristic of the optimized scheme is that without changing the circuit structure, and by changing the polarization of the fixed cells, the active-low decoder changes to active-high. The optimized circuit is comprised of 94 cells in an approximate area of 0.08um^2, indicating a significant improvement compared to previous schemes. Also, one of the important advantages of the presented circuit is using the simplest inverter gate (two-cell inverter) and achieving a high signal level. In future studies, the presented decoder can be combined to develop larger decoders. The circuit layout and its performance are performed using QCA Designer.

REFERENCES

[1] J. C. Jeon, *Designing nanotechnology QCA–multiplexer using majority function-based NAND for quantum computing*. J Supercomput **77**. (2021). 1562–1578. https://link.springer.com/article/10.1007/s11227-020-03341-8

[2] A. B. Newaz, M. Billah, M. M. R. Bhuiyan, M. Abdullah-Al-Shafi, K. Ahmed, & M. Asaduzzaman, *Ultra-efficient convolution encoder design in quantum-dot cellular automata with power dissipation analysis*, Alexandria Engineering Journal. 57, (2018), 3881–3888. https://www.sciencedirect.com/science/article/pii/S1110016818301820

[3] F. Khatib, and M. Shahi, *Ultra-fast all-optical symmetry 4× 2 encoder based on interface effect in 2D photonic crystal*. Journal of Optoelectronical Nanostructures, 5(3), (2020), pp.103-114. https://jopn.marvdasht.iau.ir/article_4407.html

[4] E. Rafiee, and F. Abolghasemi, *An All-Optical NOR Gate based on Two-Dimensional Photonic Crystals*, Journal of Optoelectronical Nanostructures, 8(1), (2023), pp.47-57. https://jopn.marvdasht.iau.ir/article_5896.html

[5] Z. Rohani, and A. A. Emrani Zarandi, *Designing a Novel high-speed ternary-logic multiplier using GNRFET Technology*. Journal of Optoelectronical Nanostructures, 8(1), (2023) pp.1-12. https://jopn.marvdasht.iau.ir/article_5800.html

[6] C. S. Lent, P. Tougaw, W. Porod, and G. Bernstein, *Quantum cellular automata*, Nanotechnology, 4(1), (1993), 49-57. https://iopscience.iop.org/article/10.1088/0957-4484/4/1/004/meta

[7] D. Manna, C. Mukherjee, A. Banerjee, M. Dhar, S. Panda, and B., Maji, *Towards Energy-Efficient Cost-Effective Toffoli Gate Design using Quantum Cellular Automata*. In 2023 IEEE Devices for Integrated Circuit (DevIC), (2023), 56-60. https://ieeexplore.ieee.org/abstract/document/10135003

[8] E. Blair, *Electric Field Inputs for Molecular Quantum-dot Cellular Automata Circuits*," in IEEE Transactions on Nanotechnology, 18, (2019), 453-460. https://ieeexplore.ieee.org/abstract/document/8693662

[9] R. D. Schaller and V. I. Klimov, *High efficiency carrier multiplication in PbSe nanocrystals*, Implications for solar energy conversion, Physical Review Letters, 92, (2004), 186-196. https://journals.aps.org/prl/abstract/10.1103/PhysRevLett.92.186601

[10] N. Kirstaedter, N. N. Ledentsov, M. Grundmann, D. Bimberg, V. M. Ustinov, S.S. Ruvimov, M.V. Maximov, P.S. Kopev, ZH.I. Alferov, U. Richter, P.Werner, U. Gosele, J. Heydenreich, *Low-threshold, large To injection-laser emission from (InGa)As quantum dots*, Electronics Letters, 30, (1994), 1416-1417. https://www.elibrary.ru/item.asp?id=25882085

[11] P. Bhattacharya, S. Ghosh, and A. D. Stiff-Roberts, *Quantum dot opto-electronic devices*, Annual Review of Materials Research, 34, (2004), 1-40. https://www.annualreviews.org/content/journals/10.1146/annurev.matsci.34.040203.111535

[12] C. Santori, M. Pelton, G. Solomon, Y. Dale, and Y. Yamamoto, *Triggered single photons from a quantum dot*, Physical Review Letters, 86, (2001), 1502-1505. https://journals.aps.org/prl/abstract/10.1103/PhysRevLett.86.1502

[13] S. Maimon, E. Finkman, G. Bahir, S. E. Schacham, J. M. Garcia, and P. M. Petroff, *Intersublevel transitions in InAs/ GaAs quantum dots infrared photodetectors*, Applied Physics Letters, 73, (1998), 2003-2005. https://pubs.aip.org/aip/apl/articleabstract/73/14/2003/69140/Intersublevel-transitions-in-InAs-GaAs-quantum

[14] R. Roy, S. Sarkar, and S. Das, *Multilayer Structure of a New Portable, Low-Cost and Reversible Arithmetic and Logic Unit using High-Speed and Low-Power QCA Technology with Good-Scalability*, International Journal of Recent Technology and Engineering (IJRTE), 8(4), (2019), 10568-10575. https://www.ijrte.org/download/volume-8-issue-4/

[15] S. Dindigul, *Efficient Design of Logical Structures and Functions using Nanotechnology Based Quantum Dot Cellular Automata Design*, International Journal of Computer Applications, 3(5), (2010), 35-42. https://www.ijcaonline.org/archives/volume3/number5/726-1019/

[16] L. W. Cheng, and B. L. Wei, *XOR module based adder applications design using QCA.* Journal of VLSI circuits and systems 5(2) (2023), 36-42. https://vlsijournal.com/index.php/vlsi/article/view/70

[17] B. Y. Galadima and G. S. M. Galadanci, *QCA-BASED design of reversible hamming code encoding, decoding and correcting circuits*, International Journal of Basic and Applied Sciences, 13(2), (2024), 18-20. https://www.sciencepubco.com/index.php/ijbas/article/view/32777

[18] I. Amlani, A. O. Orlov, G. L. Snider, C. S. Lent, and G. H. Bernstein, *Demonstration of a functional quantum-dot cellular automata cell*, Journal of Vacuum Science & Technology Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena 16(6) (1998), 3795-

3799. https://pubs.aip.org/avs/jvb/article-abstract/16/6/3795/1080050/Demonstration-of-a-functional-quantum-dot-cellular

[19] A. O. Orlov, R. K. Kummamuru, R. Ramasubramaniam, G. Toth, C. S. Lent, G. H. Bernstein, G. L. Snider, *Experimental demonstration of a latch in clocked quantum-dot cellular automata*, Applied Physics Letters, 78, (2001), 1625-1627. https://pubs.aip.org/aip/apl/article-abstract/78/11/1625/514471/Experimental-demonstration-of-a-latch-in-clocked

[20] E. P. Blair, and C. S. Lent. *Quantum-dot cellular automata: an architecture for molecular computing*. Simulation of Semiconductor Processes and Devices. *SISPAD 2003*. IEEE, 2003, 14-18. https://ieeexplore.ieee.org/abstract/document/1233626

[21] Y. Lu, and C. S. Lent. *Theoretical study of molecular quantum dot cellular automata*. Journal of Computational Electronics, 4(2), (2005), 115-118. https://link.springer.com/article/10.1007/s10825-005-7120-y

[22] C. S. Lent, B. Isaksen, and M. Lieberman. *Molecular quantumdot cellular automata*. Journal of the American Chemical Society, 125(4) , (2003), 1056-1063. https://pubs.acs.org/doi/abs/10.1021/ja026856g

[23] A. Imre, G. Csaba, L. Ji, A. Orlov, G. H. Bernstein, and W. Porod. *Majority logic gate for magnetic quantum-dot cellular automata*. Science 311, 5758 (2006), 205-208. https://www.science.org/doi/abs/10.1126/science.1120506

[24] R. Pourtajabadi and M. Nayeri, *A Novel Design of a Multi-Layer Decoder Using QCA*, Journal of Optoelectronical Nanostructures, 4(1), (2019), 39-50. https://jopn.marvdasht.iau.ir/article_3384.html

[25] A. Kumar, and B. Subhashish. *A Review of Quantum Dot Cellular Automata for High Speed Applications*. Annuals of the Romanian Society for Cell Biology (2021), 9614-9621. http://annalsofrscb.ro/index.php/journal/article/view/3704

[26] P. Jayanta, M. Noorallahzadeh, and J. S. Sharma, *Regular clocking scheme based design of cost-efficient comparator in QCA*, Indonesian Journal of Electrical Engineering and Computer Science, 21(1), (2021), 44-55.

https://ijeecs.iaescore.com/index.php/IJEECS/article/view/22478

[27] H. Balijepalli, and M. Niamat, *Design of a Nanoscale Quantum-dot Cellular Automata Configurable Logic Block for FPGAs*, International Midwest Symposium on Circuits and Systems, (2012), 622-625. https://ieeexplore.ieee.org/abstract/document/6292097

[28] K. Makanda, and J. C. Jeon, *Combinational Circuit Design Based on Quantum-Dot Cellular Automata*, International Journal of Control and Automation, 7(6), (2014), 369-378. https://www.earticle.net/Article/A230052

[29] M. Kumar and T. N. Sasamal, *An Optimal Design of 2-to-4 Decoder circuit in Coplanar Quantum dot Cellular Automata*, Energy Procedia 117, (2014), 369-378. https://www.sciencedirect.com/science/article/pii/S1876610217324074

[30] S. Riki and F. S. Hassani, *A Robust Single Layer QCA Decoder Using A Novel Fault Tolerant Three Input Majority Gate*, Journal of Optoelectronical Nanostructures, 7(3), (2022), 23-45. https://jopn.marvdasht.iau.ir/article_5336.html