A New Asymmetric Cascaded Multilevel Inverter with Reduced Switches and dc Sources Count

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Abstract

In this manuscript, a basic unit topology of cascaded multilevel H-Bridge inverter along with the extended topology is proposed in which H-Bridge is utilized to generate positive and negative voltage outputs. A dc source magnitude calculation method is proposed using which the equations for calculating number of IGBTs, isolated dc sources, gate driver circuits and output voltage levels are derived. The proposed topology is compared with recent similar topologies in different aspects using the mentioned equations. The comparison results reveal that the proposed topology has superiority over similar topologies and requires lower number of power electronic switches, gate driver circuits and isolated dc voltage sources which will decrease complexity and cost of the inverter design. Finally, the accurate performance of proposed inverter will be verified through software simulation in PSCAD/EMTDC platform.

Keywords: Cascaded multilevel H-Bridge, symmetric series multilevel inverter, asymmetric series multilevel inverter

1. Introduction

Recent improvements in developing the multilevel inverters (MLIs) and their applications in medium and high voltage, and the advantages they have over traditional two-level inverters, has made MLIs a suitable alternative for replacing these inverters [1,2]. Generating output voltage with lower total harmonic distortion (THD), having very low common voltage, lower switching frequency, lower electromagnetic interference (EMI), lower switching losses, higher efficiency and…, has made MLIs a popular choice for industrial applications [3]. Having overmentioned advantages over traditional two-level inverters, has made multilevel inverters a suitable option for applications such as high voltage direct current (HVDC), hybrid electrical vehicles (HEVs), Flexible AC Transmission System (FACTS), motor drives, grid-connected photovoltaic systems and uninterruptible power supply (UPS) systems [4-7]. The most common multilevel inverter topologies are, Neutral Point Clamped MLIs (NPC MLIs) [8], Flying Capacitor multilevel inverters (FC MLIs) [9] and Cascaded H-Bridge MLIs (CHB MLIs) [10].

To improve the quality of output voltage in multilevel inverters, number of output voltage levels could be increased to minimize the output voltage THD which will create a possible drawback for MLIs. Number of power electronic components will increase in order to generate higher numbers of output voltage levels, which

increases the volume, cost and complexity of the inverters. To deal with this issue, efforts in proposing topologies with reduced number of components has been an ongoing research area for the recent years which has led to introduction of different topologies in this regard [11-15].

Topologies introduced in [11,12], are using symmetrical dc magnitude calculation method with equal dc sources, which in comparison to asymmetric dc magnitude calculation, that uses dc sources with different magnitudes, requires lower volume and is less costly for inverter prototyping, but at the same time it has lower number of output voltage levels. Asymmetric topologies presented in [13-15], use bi-directional common emitter switches, which includes two IGBTs, and two parallel diodes and requires only one gate driver circuit. Topology [15], is composed of two series half-bridges, each of which is connected to an isolated dc source. Although the topology requires more power electronic switches, and gate driver circuits, it guarantees lower voltage stress on the switches. Higher number of IGBTs issue in topology [12], could be notably solved by using uni-directional switches, which have and IGBT and a parallel diode, but it still requires high number of isolated dc sources.

In this manuscript, initially the basic unit of proposed inverter which is capable of generating only positive output voltages, is presented. Then to increase the output voltage levels, the basic unit is extended to form the proposed inverter topology, and to generate the negative voltage outputs, an H-Bridge is added to the output of the inverter. Furthermore, the required equations are derived and to increase number of output voltage levels, an algorithm is proposed to calculate magnitude of dc voltage sources. To verify the performance of the proposed inverter and to study the merits and drawbacks of the proposed inverter over previously introduced topologies, it will be compared with most recent MLI topologies. Finally, the accurate performance of proposed MLI, will be verified through simulation results of a 31-level MLI in PSCAD/EMTDC software platform.

2. Proposed Topology

A 16-level multilevel inverter has been proposed in this manuscript, which consists of 4 uni-directional power electronic switches, 5 bi-directional switches, 2 dc voltage sources in the right side and 2 dc voltage source in the left side. The correct switching pattern for this topology, should prevent short circuiting the voltage sources, so the switch pairs $S_{R,1}$ and $S_{R,2}$, $S_{L,3}$ and $S_{L,2}$, K_1, K_2 and $S_{L,1}$should work in a complementary way, and should not be turned at the same time. Table I presents the output voltage for different states of switches for the topology shown in Fig. 1, in which 1 and 0 represent ON and OFF states of switches respectively.

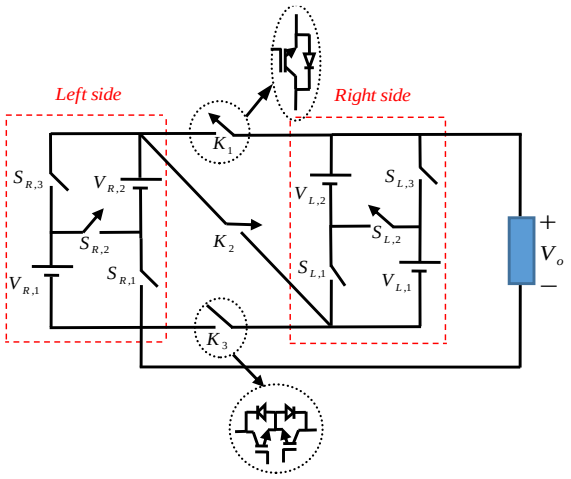


Fig. 1. The basic unit for proposed topology

Table I. Switching states for basic unit of proposed topology

$S_{R,1}$	$S_{R,2}$	$S_{R,3}$	$S_{L,1}$	$S_{L,2}$	$S_{L,3}$	K_1	K_2	K_3	V_o
0	0	0	0	0	0	1	1	1	**0**
1	0	0	0	0	0	1	0	0	$(V_{R,2})V_{dc}$
0	0	1	0	0	0	1	0	0	$(V_{R,1})V_{dc}$
0	1	0	1	0	0	1	0	0	$(V_{R,1} + V_{R,2})V_{dc}$
0	0	0	1	0	0	0	0	1	$(V_{L,2})V_{dc}$
1	0	0	1	0	0	0	1	0	$(V_{R,2} + V_{L,2})V_{dc}$
0	0	1	1	0	0	0	1	0	$(V_{S,2} + V_{L,2})V_{dc}$
0	1	0	0	0	0	0	1	0	$(V_{R,1} + V_{R,2} + V_{L,2})V_{dc}$
0	0	0	0	0	1	0	0	1	$(V_{L,1})V_{dc}$
1	0	0	0	0	1	0	1	0	$(V_{R,2} + V_{L,1})V_{dc}$
0	0	1	0	0	1	0	1	0	$(V_{R,1} + V_{L,1})V_{dc}$
0	1	0	0	0	1	0	1	0	$(V_{R,1} + V_{R,2} + V_{L,1})V_{dc}$
0	0	0	0	1	0	0	0	1	$(V_{L,1} + V_{L,2})V_{dc}$
1	0	0	0	1	0	0	1	0	$(V_{R,2} + V_{L,1} + V_{L,2})V_{dc}$
0	0	1	0	1	0	0	1	0	$(V_{R,1} + V_{L,1} + V_{L,2})V_{dc}$
0	1	0	0	1	0	0	1	0	$(V_{R,1} + V_{R,2} + V_{L,1} + V_{L,2})V_{dc}$

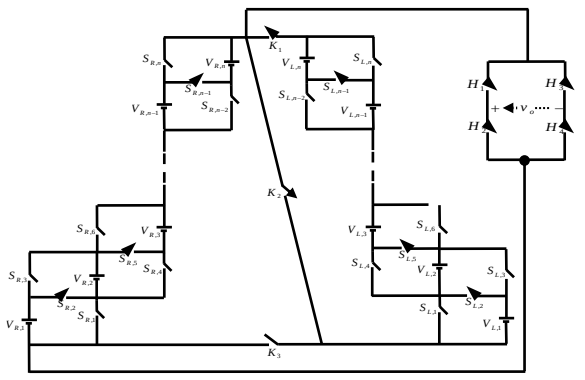


Fig. 2. The proposed Multilevel inverter topology

Error! Reference source not found. The topology shown in **Error! Reference source not found.**, is the extended version of the basic topology shown in Fig. 1, which uses an H-Bridge to generate negative and positive voltage levels in the output.

Number of IGBTs used in the proposed multilevel inverter shown in **Error! Reference source not found.**, (N_{IGBT}), number of isolated dc voltage sources (N_{source}), number of gate driver circuits $(N_{variety})$ could be calculated based on below equations,

$$N_{IGBT} = 10n - 2 \quad (1)$$

$$N_{source} = 2n \quad (2)$$

$$N_{\text{driver}} = 6n + 1 \quad (3)$$

$$N_{variety} = 2n \quad (4)$$

In which, n is the number of dc voltage sources in each side of the inverter. Based on Table, the maximum output voltage and number of generated output voltage levels can also be calculated as;

$$V_{o,max} = (V_{R,1} + V_{R2} + \cdots + V_{Rn} + V_{L1} + V_{L2} + \cdots + V_{L,n})V_{dc} \quad (5)$$

$$N_{step} = 2(V_{R,1} + V_{R,2} + \cdots + V_{R,n} + V_{L,1} + V_{L,2} + \cdots + V_{L,n}) + 1 \quad (6)$$

3. Algorithm for Calculation of dc Source Magnitude

Proper algorithm for calculation of dc source magnitude is of importance in generating different output voltage levels and in avoiding generation of duplicate voltage levels. Therefore, using dc sources with optimum values will increase number of output voltage levels using the same number of basic units.

Based on the proposed algorithm for calculation of dc voltage source magnitude, to avoid generating duplicate output voltage levels for generation of the output voltage levels as presented in Table, magnitude of dc voltage source in each basic unit is calculated by;

$$V_{R,i} = 2^{i-1}V_{dc} \quad i = 1,2,3,\ldots,n \quad (7)$$

$$V_{L,i} = 2^n(2^{i-1})V_{dc} \quad i = 1,2,3,\dots,n \tag{8}$$

$$V_{o,max} = (2^{2n} - 1)V_{dc} \tag{9}$$

$$N_{step} = 2^{2n+1} - 1 \tag{10}$$

4. Comparison of the Proposed Topology with Common Topologies

To verify the superiority of the proposed topology, a comprehensive comparison on different aspects is performed between this topology and other recently proposed MLI topologies. The first comparison is performed on number of IGBTs, used in different topologies, which based on **Error! Reference source not found.**-a is less than other topologies proposed in [16-26] for $N_{step} \geq 25$. Comparison of number of gate driver circuits is performed in **Error! Reference source not found.**-b, which shows the primacy of proposed topology over other topologies in [16-26] in using lower number of gate driver circuits for $N_{step} \geq 40$. **Error! Reference source not found.**-c reveals that ratio of number of dc voltage sources over number of output voltage levels is equal between proposed topology and the topology in [18] which is lower than all other recent MLI topologies.

Table2. Switching states for the proposed topology

$S_{R,1}$	$S_{R,}$	$S_{R,3}$	⋯	$S_{R,n-1}$	$S_{R,n}$	$S_{L,1}$	$S_{L,2}$	$S_{L,3}$	⋯	$S_{L,n-1}$	$S_{L,n}$	K_1	K_2	K_3	H_1	H_2	H_3	H_4	V_o
0	0	0	⋯	0	0	0	0	0	⋯	0	0	1	1	1	1	0	0	1	$\mathbf{0}$
1	0	0		0	0	0	0	0		0	0	1	0	0	1	0	0	1	$(V_{R,2})V_{dc}$
0	0	1		0	0	0	0	0		0	0	1	0	0	1	0	0	1	$(V_{R,1})V_{dc}$
									⋯										⋮
0	0	1	⋯	0	0	0	1	0	⋯	0	0	0	1	0	1	0	0	1	$(V_{R,1}+V_{L,1}+V_{L,2})V_{dc}$
0	1	0		0	0	0	1	0		0	0	0	1	0	1	0	0	1	$(V_{R,1}+V_{R,2}+V_{L,1}+V_{L,2})V_{dc}$
									⋯										⋮
0	1	0	⋯	1	0	0	1	0	⋯	1	0	0	1	0	1	0	0	1	$((V_{R,1}+V_{R,2}+\cdots+V_{R,n}+V_{L,1}+V_{L,2}+\cdots+V_{L,n})V_{dc}$
1	0	0		0	0	0	0	0		0	0	1	0	0	0	1	1	0	$-(V_{R,2})V_{dc}$
0	0	1		0	0	0	0	0		0	0	1	0	0	0	1	1	0	$-(V_{R,1})V_{dc}$
									⋯										⋮
0	0	1	⋯	0	0	0	1	0	⋯	0	0	0	1	0	0	1	1	0	$-(V_{R,1}+V_{L,1}+V_{L,2})V_{dc}$
0	1	0		0	0	0	1	0		0	0	0	1	0	0	1	1	0	$-(V_{R,1}+V_{R,2}+V_{L,1}+V_{L,2})V_{dc}$
									⋯										⋮
0	1	0	⋯	1	0	0	1	0	⋯	1	0	0	1	0	0	1	1	0	$-(V_{R,1}+V_{R,2}+\cdots+V_{R,n}+V_{L,1}+V_{L,2}+\cdots+V_{L,n})V_{dc}$

Table 3. Quantitative comparison of proposed topology and the recent MLI topologies to generate 75 levels of output voltage

REF →	16	17	18	19	20	21	22	23	24	25	26	PROPOSED
N_{level}	75	75	75	75	75	75	75	75	75	75	75	**75**
N_{IGBT}	76	47	22	78	23	78	66	115	42	34	40	**20**
N_{driver}	76	47	22	78	24	66	66	115	42	34	24	**20**
N_{source}	1	19	6	37	1	37	37	37	18	12	19	**6**
Capacitors	-	-	-	-	12	-	-	-	-	-	-	-
Diodes	-	-	-	-	1	-	-	-	16	-	-	-

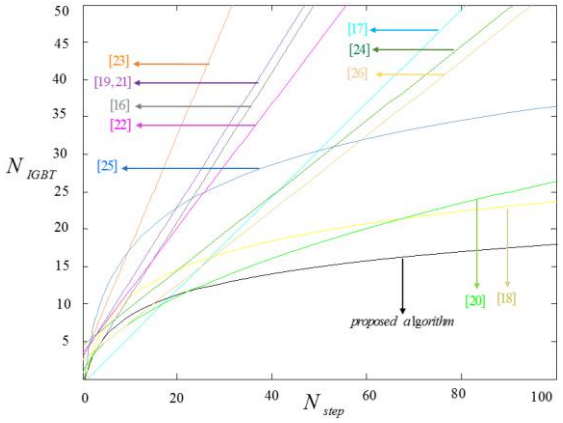


Fig. 3a. Plot of variations of N_{IGBT}, to N_{step}

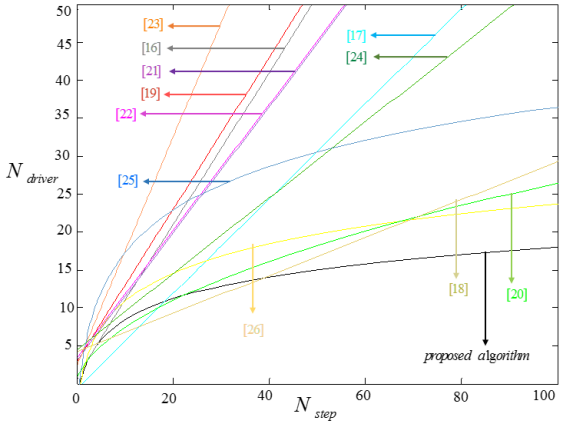


Fig. 3b. Plot of variations of N_{IGBT}, to N_{step}

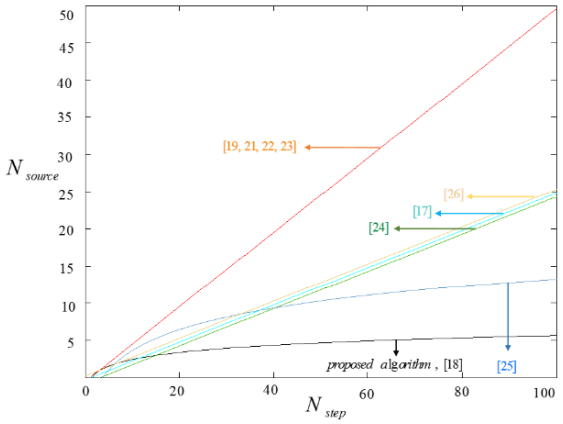


Fig.3c. Plot of variations of N_{source} to N_{step}

Table verifies the over mentioned comparisons by a quantitative comparison on number of power electronic components for inverters at least with 75 levels, between different MLI topologies. Based on this table, the proposed topology uses 20 IGBTs, 20 gate driver circuits and 6 dc voltage sources to generate 75 levels of voltage in the output. However, topologies presented in [16-26] are using 40, 34, 42, 115, 66, 78, 22, 47, and 76 IGBTs 24, 78, 22, 47, 76, 24, 34, 42, 115, 66 and 66 gate driver circuits and 19,12,18,37, 37, 37, 1, 37, 6, 19 and 1 dc voltage source respectively, to generate the same number of output voltage levels in the output.

5. Simulation Results

To verify the performance of the proposed topology, a 31-level cascaded multilevel inverter with output voltage of 150 V and frequency of 50 Hz, is modelled in PSCAD/EMTDC platform with an R-L load of 50 ohms, 90 mH. For the simulation of topology shown in Fig. , based on the proposed dc source magnitude calculation algorithm, values of dc sources $V_{R,1}, V_{R,2}, V_{L,1}, V_{L,2}$ are 10, 20, 40 and 80 volts respectively. In this topology for generating 31 levels of voltage, 4 dc voltage sources, 18 IGBTs and 13 gate driver circuits have been used.

There are several different modulation methods that could be used for generating the switching patterns of MLIs, out of which to keep the switching frequencies lower, the fundamental frequency switching method is used to generate the switching patterns of the MLI switches. In this simulation all the power switches are assumed to be ideal, and output voltage and current waveforms for the proposed inverter is shown in Fig. . Fig. -9 show the standing voltage on OFF switches, maximum of which is 20, 30, 20, 80, 120, 80, 120, 55, 40, 150, 150, 150, 150, volts which leads to a total standing voltage of 1165 the proposed 31-level multilevel inverter. It is worth mentioning that the

standing voltage for $S_{R,1}$ has both positive and negative values which proves $S_{R,1}$ to be a bi-directional switch while standing voltage for $S_{R,2}$ only takes positive and zero values which shows that $S_{R,2}$ is a uni-directional switch. THD for output current and voltage is 0.15% and 1.15% respectively. Based on Fig. -b, the output current waveform is almost sinusoidal and free of high order harmonics that has a lower THD value compared to output voltage waveform, which is a result of R-L load acting as a low pass filter.

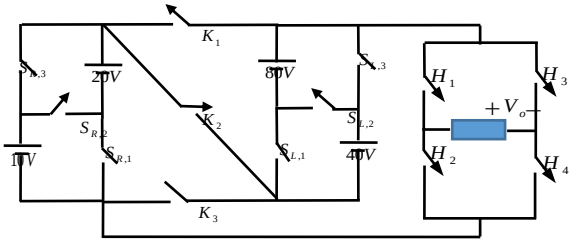
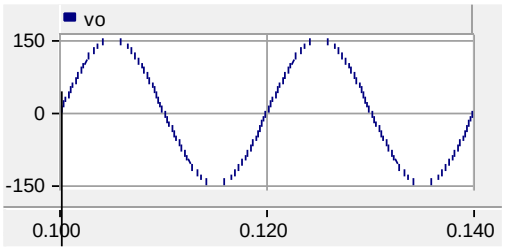


Fig. 4. proposed 31-level MLI



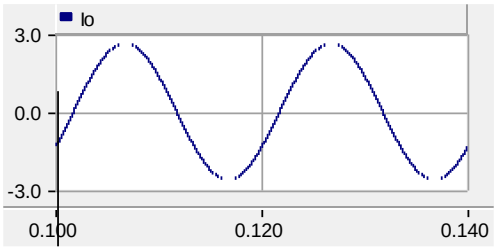


Fig. 5. a) Output Voltage Waveform, b) Output Current Waveform

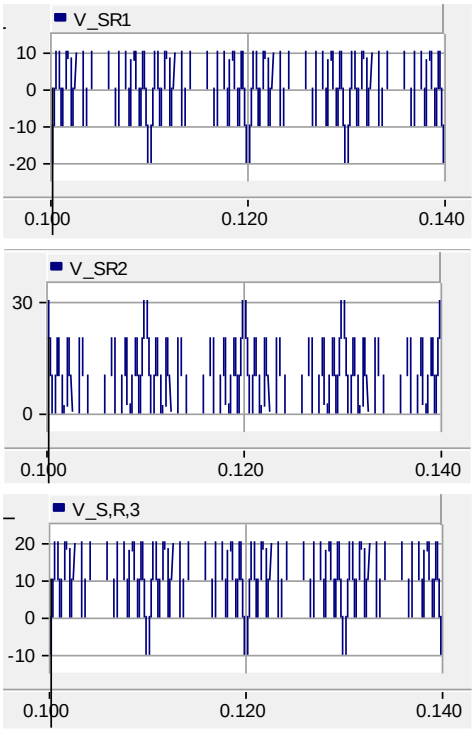


Fig. 6. Standing voltage of different switches in the 31-level MLI

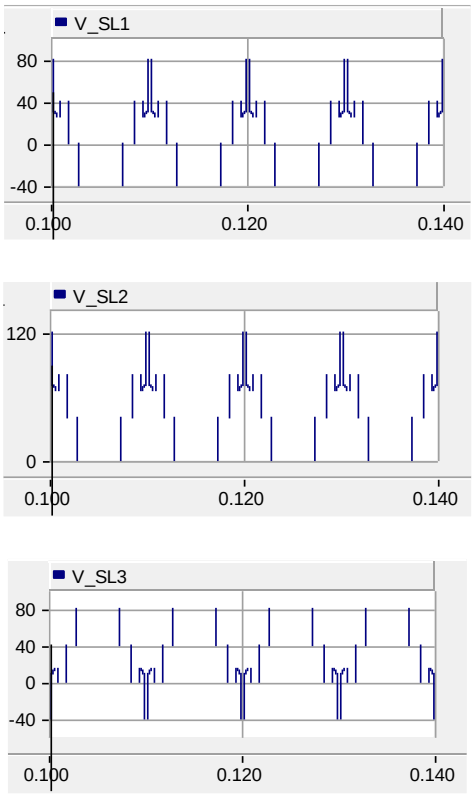


Fig. 7. Standing voltage of different switches in the 31-level MLI

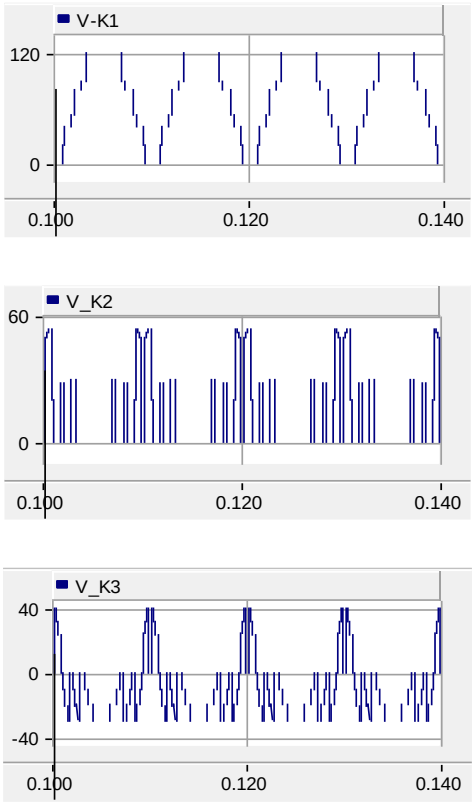


Fig. 8. Standing voltage of different switches in the 31-level MLI

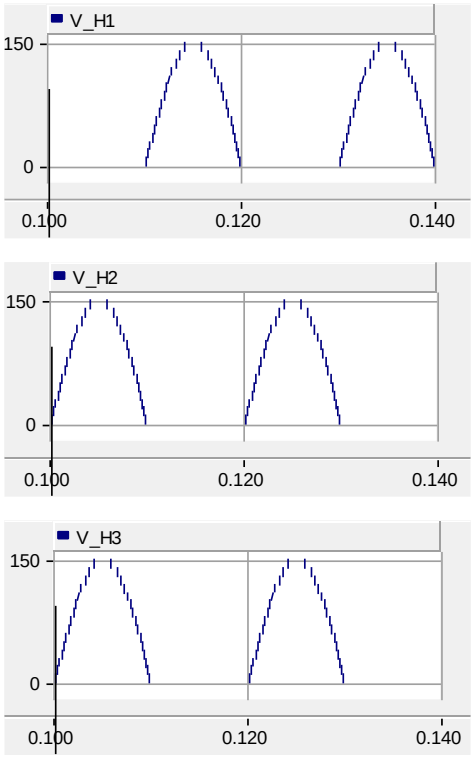


Fig. 9. Standing voltage of different switches in the 31-level MLI

6. Conclusion

In this manuscript, a new basic unit is proposed for a multilevel inverter with reduced number of components. The proposed basic unit, is able to generate 16 levels of output voltage levels using 14 IGBTs and 4 dc sources. To increase the number of output voltage levels, cascaded connection of basic units is presented. To define the merits and drawbacks, the proposed MLI topology is compared with several recently proposed MLIs. The comparisons reveal that, number of IGBTs, gate driver circuits, and dc sources is less for the proposed topology compared to other topologies for generation of the same number of voltage levels in the output, which leads to decreased volume, cost, control complexity and higher efficiency. As an example, to generate 75 levels of output voltage, proposed topology uses 20 IGBTs, 20 gate driver circuits and 6 dc sources whereas the topology in [21], uses 78 IGBTs, 66 gate driver circuits and 37 voltage sources. Finally, to verify the performance of the proposed topology, a 31-level MLI of proposed topology is modelled in PSCAD/EMTDC platform and the results has been reported in the paper.

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