Islamic Azad University

Journal of

Optoelectronical Nanostructures

Autumn 2023 / Vol. 8, No. 4

Research Paper

Voltage Difference Technique in Junctionless Tunneling FET for Suppression of Ambipolar Conduction

Morteza Rahimian*[,1]

[1] Faculty of Electrical, Biomedical and Mechatronics Engineering, Qazvin Branch, Islamic Azad University, Qazvin, Iran

Received: 10 Oct. 2023
Revised: 21 Nov. 2023
Accepted: 1 Dec. 2023
Published: 15 Dec. 2023

Use your device to scan and read the article online

Abstract:

A detailed study of a novel configuration for junctionless tunneling FET (J-TFET) with extremely low off- (I_{off}) and ambipolar current (I_{amb}) is reported in this paper. In order to achieve desirable on/off current ratio (I_{on}/I_{off}), we have employed voltage difference technique on the gate electrode based on the potential distribution benefits. Main and side gates with an optimum voltage difference creates a stepped potential profile along the channel. This raises the drain side's bands, reduces the electric field, puts restriction on the flow of charge carriers, and finally remarkable reduction of I_{amb} from 6.52×10^{-10} A/µm to 1.14×10^{-17} A/µm. Also an extremely low subthreshold swing (*SS*) (22 mV/dec) is achieved thanks to the sharp transition from off- to the on-state. Finally we have investigated the electrical performance of the proposed device for sub-30 nm channel length to examine its immunity against short channel effects. Therefore, our approach renders the novel structure more desirable for the future low power applications.

Keywords:
Off-state current; Ambipolarity; Junctionless TFET; Tunneling barrier width; Band-to-band tunneling (BTBT); 2D simulation.

Citation: First Author's Full Name, Second Author's Full Name, Third Author's Full Name. The effect of Cinnamon supplementation on lipid profile in response to aerobic exercise. **Journal of Optoelectronical Nanostructures. 2023; 8 (4): 51- 62**
DOI: 10.30495/JOPN.2023.32088.1294

***Corresponding author:** Morteza Rahimian
Address: Faculty of Electrical, Biomedical and Mechatronics Engineering, Qazvin Branch, Islamic Azad University, Qazvin, Iran. **Tell:** 00982833665275 **Email:** morteza.rahimian@qiau.ac.ir

1. INTRODUCTION

Consecutive power consumption is an immediate concern for continued scaling of devices **[1-3]**. Thus, there is a strong push toward focusing on tunneling field-effect transistors (TFETs) as a meet candidate for low power applications, because their conduction relies strongly on the tunneling mechanism (BTBT) **[4-6]**. This mechanism presents the possibility of low subthreshold swing (*SS*) under the 60 mV/dec of the conventional MOSFETs together with high on/off current ratio (I_{on}/I_{off}) **[7-10]**.

However, TFETs suffer from some major concerns including: **1)** low I_{on} **[7-16]**; **2)** extremely high ambipolar current (I_{amb}), an inherent property of conduction irrespective of gate voltage polarity **[17-22]** which relies strongly on the tunneling chance near the drain side; **3)** large variation in doping concentration due to the abrupt highly doped junctions of the scaled TFETs over a few nanometers **[23-24]**. Beside other shortcomings, to overcome the last challenge, junctionless TFET (J-TFET) without any stringent requirement for controlling a precise and steep p-n junction was numerically studied to attend as an encouraging approach for conventional TFET **[25-32]**.

In this paper, we will introduce a novel J-TFET structure to obtain desirable I_{on}/I_{off} ratio thanks to modified band diagrams near the drain side. Voltage difference technique is utilized on the gate electrode, in order to deplete electrons effectively, and widen the tunneling path extensively all near the drain side to diminish ambipolar current noticeably.

2. DEVICE PARAMETERS AND SIMULATION MODELS

To realize the proposed structure emphasizing on voltage difference technique (VDJ-TFET), we first begin with a junctionless MOSFET with uniform n^+ doped. To obtain the J-TFET, the charge plasma concept is utilized with an appropriate workfunction (Pt, Platinum, *WF*= 5.93 eV) of a metal electrode using the ATLAS device simulator **[33]** as shown in **Fig. 1(a)**. This converts N^+ doped source region into a P^+. Also, the VDJ-TFET consists of a main gate and a side gate of L_{MG} and L_{SG} in length, respectively, which both have the same workfunction (*WF*= 4.2 eV) as illustrated in **Fig. 1(b)**. The voltage difference between the gates controls the channel to improve the electrical performance especially I_{amb}. The voltage for the side gate (V_{SG}) is

greater than that of the main gate (V_{MG}) as much as V_{Diff}. In order to examine the characteristics of the VDJ-TFET, we have applied several values for the V_{Diff}. The gap length between the gates is 2 nm. Parameters for the VDJ-TFET structure are listed in **Table I**. The VDJ-TFET has the same typical parameters as for the J-TFET unless otherwise stated.

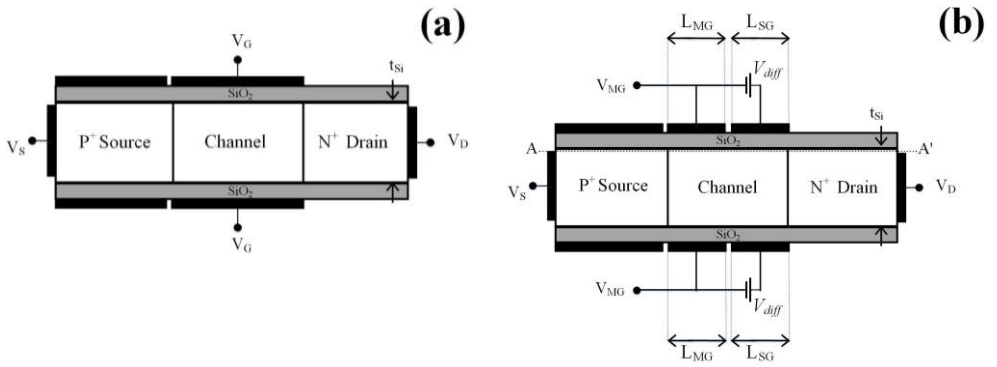

Fig. 1. Cross sectional views of the (a) J-TFET, and the (b) VDJ-TFET structures.

Table. I: Parameters used for simulation of devices

Parameters	VDJ-TFET	J-TFET
Channel length	30 nm	30 nm
Main-Gate (MG) and Side-Gate (SG) length	14 nm	-
Gap length between the MG and the SG	2 nm	-
Thickness of silicon film (t_{si})	10 nm	10 nm
Thickness of gate oxide (t_{ox})	1 nm	1 nm
Doping Concentration of the silicon film (N_A)	1×10^{19} cm^{-3}	1×10^{19} cm^{-3}

To account for the lateral tunneling, nonlocal BTBT model **[12-14]** is employed. This model explains carrier transport through the energy band profile along the entire tunneling path. The doping-dependent and field-dependent mobility degradations were taken into consideration using the Philips and Lombardi mobility models, respectively. We have also employed the direct recombination (Auger) as well as the band gap narrowing (BGN) models because of the high carrier concentration in the silicon layer **[33]**. The Shockley-Read-Hall (SRH) model is utilized for the thermal generation-recombination mechanism. Worth noting that the quantum confinement model as given by Hänsch et al. **[34]** is taken into account. However, this can be neglected because the thickness of silicon film in our simulation is more than 7 nm **[31-34]**.

Fig. 2 exhibits calibration of an experimental TFET against results of the simulation models under similar conditions as those reported in **[5]**. As can be seen from the figure, obtaining results from the transfer characteristics (I_{DS}-V_{GS}) are in well agreement against experimental data. This indicates that our simulation study effectively consider the impact of lateral BTBT (L-BTBT).

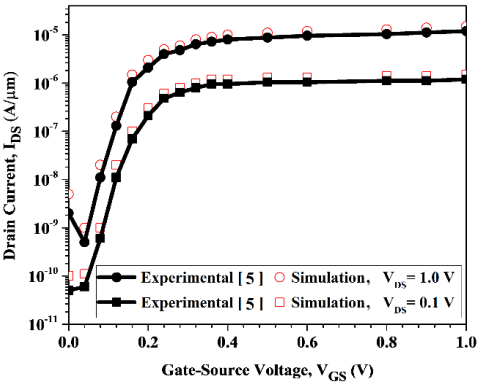

Fig. 2. Calibration of transfer characteristics (I_{DS}-V_{GS}) against experimental results **[5]**.

3. RESULT AND DISCUSSION

Fig. 3(a) demonstrates the effect of the voltage difference on the VDJ-TFET's band diagrams in the region of ambipolar conduction (V_{GS}= -1.0 V, V_{DS}= 1.0 V) with V_{Diff} taken as parameter. To decrease the I_{amb}, the tunneling path between the channel and the drain regions needs to be extend enough **[18-24]** which can be provided by changing the V_{Diff} values. Increasing the V_{Diff} from

0.0 V (act as a J-TFET) to 1.0 V realizes a stepped profile in the band diagram of the VDJ-TFET. This provides widening of the tunneling path from 6 nm to 12 nm that leads to negligible probability of the electrons tunneling and thus in turn noticeable reduction of the ambipolar conduction. In **Fig. 3(b),** the effective impact of V_{Diff} on I_{amb} alleviation is exhibited when the VDJ-TFET's transfer characteristics (I_{DS}-V_{GS}) are plotted. As it is obvious from the figure, a significant improvement in I_{amb} extracted at V_{GS}= -1.0 V is observed when V_{Diff} is enhanced. High amount of V_{Diff} is responsible for further step of the band diagrams near the drain side which extends the tunneling width. As can be seen from **Fig. 3(b)**, the effect of V_{Diff} on the *SS* and I_{on} parameters is negligible while they remain almost constant by different values of the V_{Diff}. This is so desirable, because the main focus of employing V_{Diff} technique is on the I_{amb} improvement.

Fig. 4(a) demonstrates the I_{amb} taken out at V_{GS}= -1.0 V, as a function of the V_{Diff} for various amounts of the V_{DS}. Since, the V_{Diff} assigns the width of the drain side's tunneling path, I_{amb} is strongly decreased as the V_{Diff} is enhanced. Also, the *SS* value versus the drain current is shown in **Fig. 4(b)**. As well as J-TFET, the VDJ-TFET exhibits the capability of realizing favorable *SS* values over wide ranges of the I_D. Thus not only the I_{amb} but also the *SS* of the VDJ-TFET exhibit superior operation for low power applications.

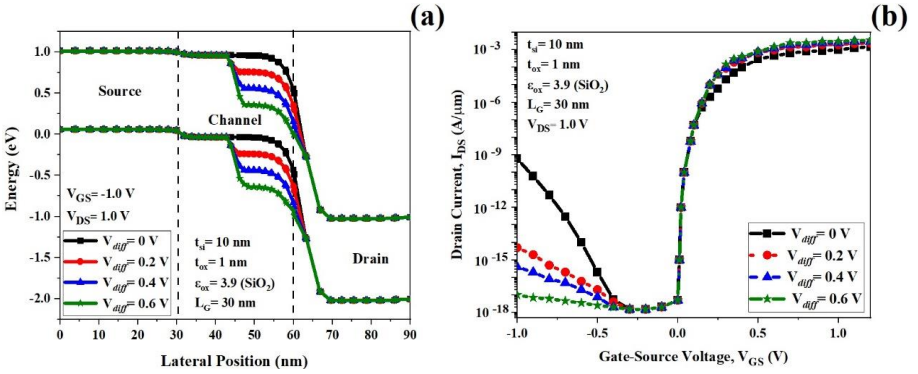

Fig. 3. (a) Band diagrams of the VDJ-TFET at V_{GS}= -1.0 V, (b) The VDJ-TFET's transfer characteristics with voltage difference between the MG and SG as a parameter.

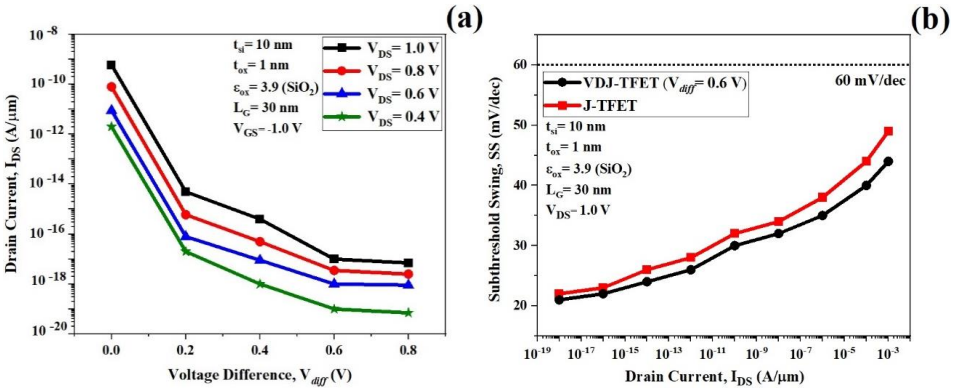

Fig. 4. (a) I_{amb} as a function of V_{diff} for different values of the V_{DS} at V_{GS}= -1.0 V, (b) subthreshold swing versus drain current for the VDJ-TFET and J-TFET structures, when line of *SS*= 60 mV/dec is drawn as a reference.

To study the impact of V_{Diff} on the I_{amb}, refer to **Fig. 5(a)**, where we have exhibited the potential profile of the VDJ-TFET at V_{GS}= -1.0 V. As it is clear from the figure, V_{Diff} provides a step potential with a sharply increase along the channel of the VDJ-TFET, but not in the J-TFET structure. This can be regarded as a main factor to extend tunneling path adjacent to the drain region which reduces I_{amb} noticeably. The electric field as a function of the V_{Diff} is also investigated in **Fig. 5(b)** at V_{GS}= -1.0 V. Although the electric field steeply enhances under the gap thanks to the bending of the band diagram, increasing the V_{Diff}, will alleviate the high amount of the electric field near the channel-drain region.

This discontinuity in the electric field can be interpreted as a decrease in the BTBT rate as shown in **Fig. 6(a)**. This plot depicts the rate of the BTBT with V_{Diff} taken as parameter. As can be seen, for larger V_{Diff}, the electron's tunneling probability from the valence band of the channel into the conduction band of the drain is small, leading to lower electrically induced free carriers at the drain side, and thus in turn reduced I_{amb}. **Fig. 6(b)** displays the electron concentration across the VDJ-TFET as a function of the V_{Diff}. Observe that as the V_{Diff} is increased, the electrons in the drain region are further depleted due to the extended tunneling path near the channel-drain junction.

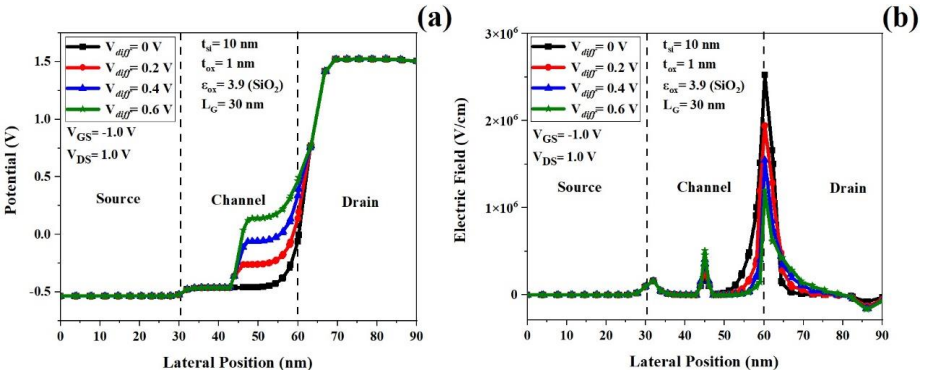

Fig. 5. The VDJ-TFET's (a) potential and (b) electric field along lateral direction for different value of the V_{diff}.

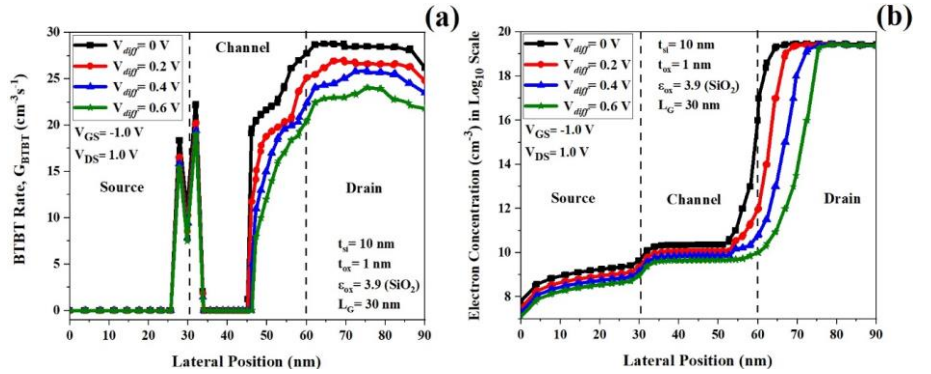

Fig. 6. (a) BTBT rate and (b) electron concentration for different values of the V_{diff} across lateral direction in the VDJ-TFET structure.

In **Fig. 7**, simulations are performed by measuring the dependence of the I_{off}, I_{on}/I_{off}, I_{amb}, and *SS* on the channel length to investigate the application of the VDJ-TFET in sub-20 nm regime. As it is obvious from the figure, only a slight variation is achieved when channel length is taken as a comparative parameter. Sub-30 nm channel length of the VDJ-TFET primarily retains the 30 nm characteristics and does not considerably degrade from the short channel effects (SCEs). Thus, the VDJ-TFET can be scaled down into the sub-30 nm regimes without any drastic influence of the SCEs.

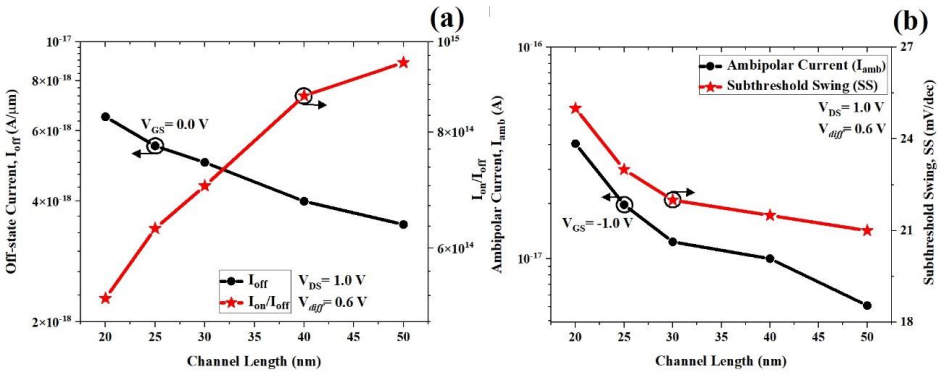

Fig. 7. Dependence of (a) I_{off} and I_{on}/I_{off}, (b) I_{amb} and subthreshold swing on the channel length variation.

4. CONCLUSION

Ambipolar current (I_{amb}) is a detrimental problem in tunneling FETs (TFETs) which should be alleviated noticeably for low power applications. In this letter, a novel design is introduced for providing a Junctionless TFET (J-TFET) with highly diminished ambipolar current. In the proposed structure (VDJ-TFET), an extended tunneling path near the channel-drain junction is achieved by gate voltage difference (V_{diff}). Higher V_{diff} leads to widening of the tunneling path which acts as a barrier for tunneling to occur and thus in turn remarkable reduced I_{amb}. Also we have optimized the V_{diff} value to obtain superior performance. Therefore the VDJ-TFET can be a proper substitution for the conventional J-TFET in the reliable low power applications.

REFERENCES

[1]M. Rahimian and Ali. A. Orouji. *Investigation of the electrical and thermal performance of SOI MOSFETs with modified channel engineering*. Mater Sci Semicond Process., 16 (5) (Oct. 2013) 1248-1256. Available: https://doi.org/10.1016/j.mssp.2012.12.001

[2]M. Rahimian, Ali. A. Orouji and A. Aminbeidokhti. *A novel deep submicron SiGe-on-insulator (SGOI) MOSFET with modified channel band energy for electrical performance improvement*. Curr. Appl Phys., 13 (4) (Jun. 2013) 779-784. Available: https://doi.org/10.1016/j.cap.2012.12.005

[3]P. Bahrami, M. R. Shayesteh, M. Pourahmadi, H. Safdarkhani. *Improvement of the Drive Current in 5nm Bulk-FinFET Using Process and Device Simulations*. J Opt Nanostructures., 5 (1) (Feb. 2020) 65-81. Available: https://dorl.net/dor/20.1001.1.24237361.2020.5.1.5.0

[4]A. M. Ionescu and H. Riel. *Tunnel field-effect transistors as energy efficient electronic switches*. Nature., 479 (7373) (Nov. 2011) 329-337. Available: https://doi.org/10.1038/nature10679

[5]W. Y. Choi, B. G. Park, J. D. Lee, and T. J. K. Liu. *Tunneling Field-Effect Transistors (TFETs) with Subthreshold Swing (SS) Less Than 60 mV/dec*. IEEE Electron Device Lett., 28 (8) (Aug. 2007) 743–745. Available: https://doi.org/10.1109/LED.2007.901273

[6]M. Roohy, R. Hosseini. *Performance Study and Analysis of Heterojunction Gate All Around Nanowire Tunneling Field Effect Transistor*. J Opt Nanostructures., 4 (2) (May. 2019) 13-28. Available: https://dorl.net/dor/20.1001.1.24237361.2019.4.2.2.2

[7]M. A. Eshkalak, R. Faez. *A Computational Study on the Performance of Graphene Nanoribbon Field Effect Transistor*. J Opt Nanostructures., 2 (3) (Aug. 2017) 1-12. Available: https://dorl.net/dor/20.1001.1.24237361.2017.2.3.1.9

[8]M. Rahimian and M. Fathipour. *Improvement of electrical performance in junctionless nanowire TFET using hetero-gate-dielectric*. Mater Sci Semicond Process., 63 (1) (Jun. 2017) 142–152. Available: https://doi.org/10.1016/j.mssp.2016.12.011

[9]D. Keighobadi, S. Mohammadi, M. Mohtaram. *Recessed Gate Cylindrical Heterostructure TFET, a Device with Extremely Steep Subthreshold Swing*. Trans. Electr. Electron. Mater., 23 (Apr. 2021) 81–87. Available: https://doi.org/10.1007/s42341-021-00321-4

[10]G. Musalgaonkar, Sh. Sahay, R. S. Saxena and M. J. Kumar. *Nanotube Tunneling FET With a Core Source for Ultrasteep Subthreshold Swing: A Simulation Study*. IEEE Trans. Electron Devices., 66 (10) (Oct. 2019) 4425–4432. Available: https://doi.org/10.1109/TED.2019.2933756

[11]M. Rahimian, and M. Fathipour. *Asymmetric junctionless nanowire TFET with built-in n^+ source pocket emphasizing on energy band modification*. J. Comput. Electron., 15 (4) (Dec. 2016) 1297–1307. Available: https://doi.org/10.1007/s10825-016-0895-1

[12]Z. Ahangari. *Switching Performance of Nanotube Core-Shell Heterojunction Electrically Doped Junctionless Tunnel Field Effect Transistor*. J Opt Nanostructures., 5 (2) (May. 2020) 1-12. Available: https://dorl.net/dor/20.1001.1.24237361.2020.5.2.1.8

[13]M. M. Ghiasvand, Z. Ahangari, H. Nematian. *Performance Optimization of an Electrostatically Doped Staggered Type Heterojunction Tunnel Field Effect Transistor with High Switching Speed and Improved Tunneling Rate*. J Opt Nanostructures., 7 (1) (Jan. 2022) 19-36. Available: https://doi.org/10.30495/jopn.2022.29617.1249
[14]M. K. Anvarifard, Ali A. Orouji. *Energy Band Adjustment in a Reliable Novel Charge Plasma SiGe Source TFET to Intensify the BTBT Rate*. IEEE Trans. Electron Devices., 68 (10) (Oct. 2021) 5284–5290. Available: https://doi.org/10.1109/TED.2021.3106891
[15]M. Rahimian, and M. Fathipour. *Junctionless nanowire TFET with built-in n-p-n bipolar action: physics and operational principle*. J. Appl. Phys., 120 (22) (Nov. 2016) 225702. Available: https://doi.org/10.1063/1.4971345
[16]R. M. Imen Abadi, S. Ali S. Ziabari. *Representation of strained gate-all-around junctionless tunneling nanowire filed effect transistor for analog applications*. Microelectron. Eng., 162 (16) (Aug. 2016) 12-16. Available: https://doi.org/10.1016/j.mee.2016.04.016
[17]M. Rahimian. *Controlling Ambipolar Current in a Junctionless Tunneling FET Emphasizing on Depletion Region Extension*. J Opt Nanostructures., 8 (1) (Jan. 2023) 13-31. Available: https://doi.org/10.30495/jopn.2023.31255.1274
[18]Sh. Sahay and M. J. Kumar, *Controlling the Drain Side Tunneling Width to Reduce Ambipolar Current in Tunnel FETs Using Heterodielectric BOX*. IEEE Trans. Electron Devices, 62 (11) (Nov. 2015) 3882–3886. Available: https://doi.org/10.1109/TED.2015.2478955
[19]D. B. Abdi and M. J. Kumar, *Controlling Ambipolar Current in Tunneling FETs Using Overlapping Gate-on-Drain*. IEEE J. Electron Devices Soc, 2 (6) (Nov. 2014) 187–190. Available: https://doi.org/10.1109/JEDS.2014.2327626
[20]M. Aslam, G. Korram, D. Sharma, Sh. Yadav, N. Sharma, *Enhancement of the DC performance of a PNPN hetero-dielectric BOX tunnel field-effect transistor for low-power applications*. J. Comput. Electron, 19 (Dec. 2019) 271–276. Available: https://doi.org/10.1007/s10825-019-01427-y
[21]S. Kumar, B. Raj, B. Raj, *Dual-Material Gate-Drain Overlapped DG-TFET Device for Low Leakage Current Design*. Silicon, 13 (Jun. 2020) 1599–1607. Available: https://doi.org/10.1007/s12633-020-00547-6
[22]S. Zafar, M. A. Raushan, Sh. Ahmad, M. J. Siddiqui, *Reducing off-state leakage current in dopingless transistor employing dual metal drain*. Semicond. Sci. Technol, 35 (1) (Dec. 2019). Available: https://doi.org/10.1088/1361-6641/ab542b
[23]N. Damrongplasit, S. H. Kim, and T. J. K. Liu, *Study of Random Dopant Fluctuation Induced Variability in the Raised-Ge-Source TFET*. IEEE Electron Device Lett, 34 (2) (Feb. 2013) 184-186. Available: https://doi.org/10.1109/LED.2012.2235404
[24]N. Damrongplasit, Ch. Shin, S. H. Kim, R. A. Vega and T. J. K. Liu, *Study of Random Dopant Fluctuation Effects in Germanium-Source Tunnel FETs*. IEEE Trans. Electron Devices, 58 (10) (Oct. 2011) 3541–3548. Available: https://doi.org/10.1109/TED.2011.2161990

[25]B. Ghosh and M. W. Akram, *Junctionless Tunnel Field Effect Transistor*. IEEE Electron Device Lett, 34 (5) (May. 2013) 584–586. Available: https://doi.org/10.1109/LED.2013.2253752
[26]M. J. Kumar and S. Janardhanan, *Doping-Less Tunnel Field Effect Transistor: Design and Investigation.* IEEE Trans. Electron Devices, 60 (10) (Oct. 2013) 3285–3290. Available: https://doi.org/10.1109/TED.2013.2276888
[27]J. P. Colinge, C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A. M. Kelleher, B. McCarthy, and R. Murphy, *Nanowire transistors without junctions*. Nature Nanotechnol, 5 (3) (Mar. 2010) 225–229. Available: https://doi.org/10.1038/nnano.2010.15
[28]E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, *Theory of the Junctionless Nanowire FET*. IEEE Trans. Electron Devices, 58 (9) (Sep. 2011) 2903–2910. Available: https://doi.org/10.1109/TED.2011.2159608
[29]C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J. P. Colinge, *Junctionless multigate field-effect transistor*. Appl. Phys. Lett. 94 (5) (Jan. 2009) 53511-53513. Available: https://doi.org/10.1063/1.3079411
[30]M. Bolokian, Ali. A. Orouji, A. Abbasi, M. Houshmand. *Pyramid P^+ area in SOI junction-less MOSFET for logic applications: DC investigation*. Appl. Nanosci., (Feb. 2023). Available: https://doi.org/10.1007/s13204-023-02808-3
[31]M. Bolokian, Ali. A. Orouji, A. Abbasi, D. Madadi. *Realization of Double-Gate Junctionless Field Effect Transistor Depletion Region for 6 nm Regime with an Efficient Layer*. Phys. Status Solidi., 219 (21) (Nov. 2022) 2200214. Available: https://doi.org/10.1002/pssa.202200214
[32]M. Bavir, A. Abbasi, Ali. A. Orouji. *Performance Enhancement of Asymmetrical Double Gate Junctionless CMOS Inverter With 3-nm Critical Feature Size Using Charge Sheet*. IEEE J. Electron Devices Soc., 10 (Apr. 2022) 334-340. Available: https://doi.org/10.1109/JEDS.2022.3166708
[33]
ATLAS Device Simulation Software, Silvaco, Santa Clara, CA, USA, 2019. Available: https://silvaco.com/
[34]J.-P. Colinge, J. C. Alderman, W. Xiong, and C. R. Cleavelin, *Quantum–mechanical effects in trigate SOI MOSFETs.* IEEE Trans. Electron Devices, 53 (5) (May. 2006) 1131–1136. Available: https://doi.org/10.1109/TED.2006.871872