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Research Paper

A Robust Single Layer QCA Decoder Using a Novel Fault Tolerant Three Input Majority Gate

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Abstract Quantum-dot Cellular Automata (QCA) is an emerging technology and one of the suitable alternatives to conventional CMOS technology. Designing efficient basic logic circuits like decoders is an open research topic in this emerging technology. As reliability is also the most important issue in QCA technology circuit design due to its susceptibility to faults occurring during chemical fabrication, we design an efficient coplanar robust 2-to-4 decoder, employing a novel fault-tolerant three-input majority gate. Our proposed majority gate is designed with 11 simple QCA cells. The area and energy consumptions of the proposed majority gate is 0.01 μm^2 and 1.49×2^{-2} MeV, respectively. The presented majority gate has also 71% and 100% tolerance against single-cell omission and extra-cell deposition defects, respectively, and it has a proper tolerance against cell displacement and misalignment defects. The novel robust 2-to-4 decoder is also designed using the proposed majority gate. The simulation results show that the presented decoder is more efficient in comparison to previous designs.

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1. INTRODUCTION

CMOS is one of the most popular technologies for designing integrated circuits. The number of transistors in a dense integrated circuit doubles every 18 months due to the Moore's law [1]. As a result, the transistor dimensions become halved. On the other hand, as the transistor shrinks, it reaches the physical limitation. This issue causes some serious disturbances in digital circuit operations. Researchers have been trying a lot to find a suitable alternative to CMOS. Spintronics [2] and quantum-dot cellular automata (QCA) [3-6] are the technologies that have been introduced as two appropriate replacements for CMOS. Considering the area, latency, and power consumption parameters of QCA technology, it can be the best alternative to CMOS [7-11, 45, 47].

QCA technology was introduced by Lent et al. in 1993 [12]. There is no electrical current in this technology and information is transformed through the Coulomb interactions of electrons in quantum cells. One of the challenges in designing QCA circuits is the defects that may occur during the chemical synthesis and deposition phases [14].

The most important possible defects that reduce the efficiency of the QCA circuits are cell omission, cellular displacement, cell misalignment, and extra cells deposition [13-16]. Therefore, QCA researchers have been looking for different ways of designing fault-tolerant circuits.

Decoders are known computational circuits which are widely used in different digital circuit designs. We propose a fault-tolerant majority gate in order to design a robust decoder circuit based on it. The majority gate is the most important basic gate in QCA technology and all QCA circuits can be designed and implemented using the majority gates and inverters.

In this study, we first propose a fault-tolerant three-input majority gate with 11 simple QCA cells. Then the functionality of the introduced majority gate is verified via physical proof. The proposed majority gate is then investigated against cell omission, extra cell deposition, and cell displacement defects. Then the energy consumption of the proposed majority gate is calculated and compared with the similar types of majority gates. Afterward, a fault-tolerant 2-to-4 decoder is introduced using the proposed majority gate and finally, we conclude the study.

The remainder of the paper is structured as follows. We review the basic concepts in QCA technology in Section 2. The proposed fault-tolerant three-input majority gate, its functionality verification, and reliability analysis are studied in Section 3. Section 4 introduces a robust 2-to-4 decoder based on the proposed majority gate. Finally, we conclude in Section 5.

2. BASIC CONCEPTS IN QCA TECHNOLOGY

A QCA cell has a square shape that contains four quantum dots located in its vertices. A pair of electrons move freely between the quantum dots inside the cell. Generally, there are six possible states to place an electron pair in four holes, but not all of them are stable. In fact, due to the Coulumbic repulsion between the electrons, they are always placed in two square diameters of a QCA cell which are illustrated in Figure 1. These two configurations are the -1 and +1 polarizations which are defined as the binary values of 0 and 1, respectively [17, 40].

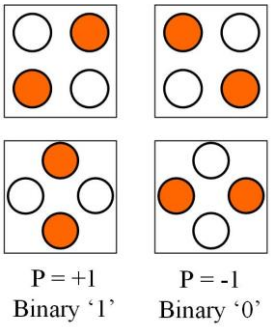

Fig. 1. The two stable states of quantum cells.

QCA cells can be placed next to each other to form different circuits. A QCA wire is created by putting the cells in a linear array form. Figure 2 shows two different types of QCA wires. As they are shown the direct and rotated QCA wires consist of simple and rotated cells, respectively [41].

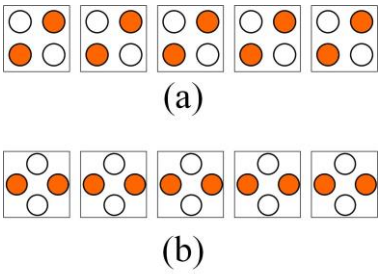

Fig. 2. QCA wires. a) direct mode, b) rotated mode.

In QCA technology, the majority gates and inverters are the two main logic gates which are widely employed to implement almost all types of logic circuits. Generally, there are two different designs for inverter which are used in QCA

circuits (Figure 3). Figure 3.b illustrates a reliable inverter that transmits the input to the output in two different ways.

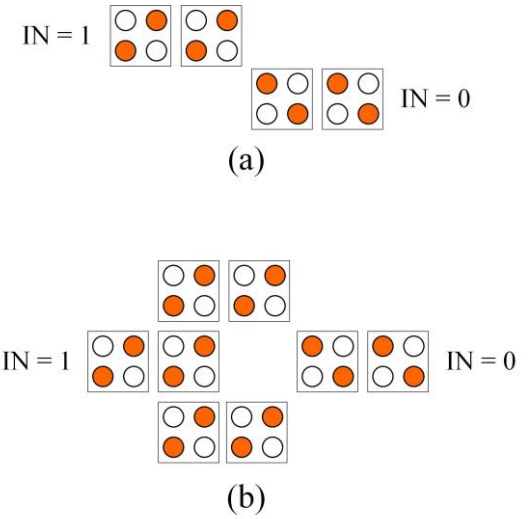

Fig. 3. The QCA inverter designs: a) the simple structure, b) the robust structure.

Figure 4 shows two different designs for a three-input majority gate. The output of this gate is calculated based on Eq.1. This gate consists of five QCA cells including three input cells, one output cell, and a decision-maker which is located in the middle of the gate. If at least two inputs out of all the three inputs become one, the output would be one; otherwise, the output would be zero [39].

$$\mathbf{MV3(X,Y,Z) = (X \wedge Y) \vee (X \wedge Z) \vee (Y \wedge Z)} \quad (1)$$

The QCA circuits need a clocking system to work properly. The clocking system is responsible to supply the main circuit power and controlling the data propagation in quantum cells. The clocking system also facilitates electrons movement in the cell and does not let them tunnel between the quantum dots. Each QCA cell may have one of these following four clock phases: switch, hold, release or relax. A cell in the switch phase starts its calculations. In the hold phase, electrons are stored and positioned within a quantum dot based on the polarity of adjacent cells. In the release phase, the electrons begin to leave their place of residence, and in the relax phase, they completely leave the place of residence and can easily circulate inside the cell. QCA designs have four clock

signals, each of which is 90 degrees different from the phase of the next and previous clocks. For example, when clock 1 is in the switch phase, clock 2 is in the relax phase, clock 3 is in the release phase, and finally, clock 4 is in the hold phase. Figure 5 shows these four clock signals.

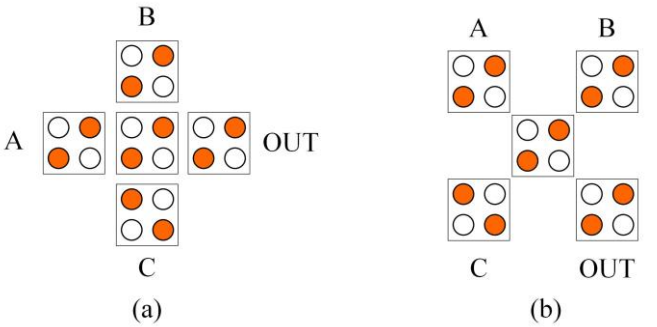

Fig. 4. Three input majority gate designs: a) the original majority gate, b) the rotated majority gate.

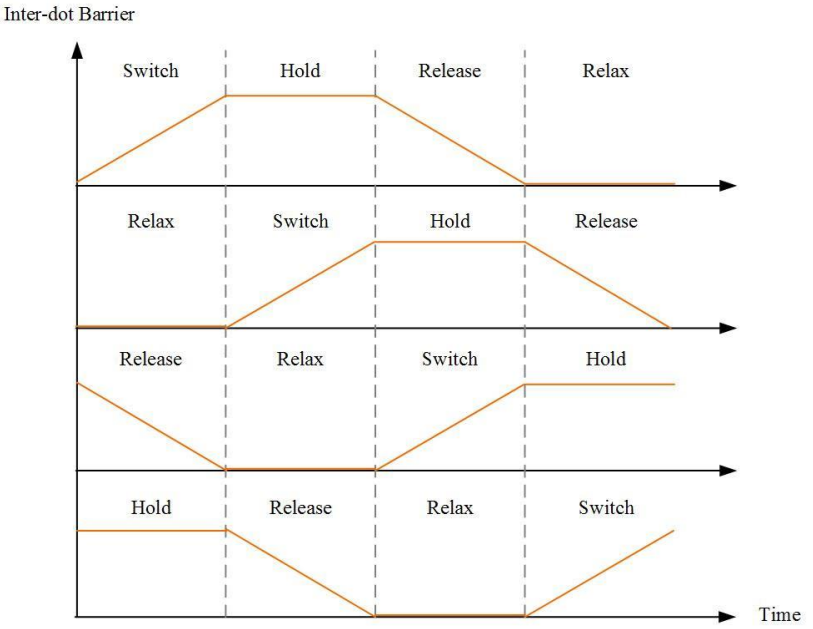

Fig. 5. Four states of clocks in QCA.

There are three types of wire crossing in QCA designs: multilayer, coplanar, and clock-based coplanar. The QCA wires in multilayer wire crossing are in different layers. Since the implementation of this type of wire crossing is practically impossible, coplanar and clock-based coplanar wire crossing structures have been proposed. Figure 6.a illustrates the coplanar wire crossing. As it is shown one of the two crossing wires is based on simple QCA cells and the other is based on rotated QCA cells. On the other hand, both crossing wires in clock-based coplanar wire crossing are based on simple QCA cells but with different clock phases (Figure 6.b). In this type of wire crossing, one of the wires must be designed in switch or release clock phases and the other must be in the hold or relax clock phases [42].

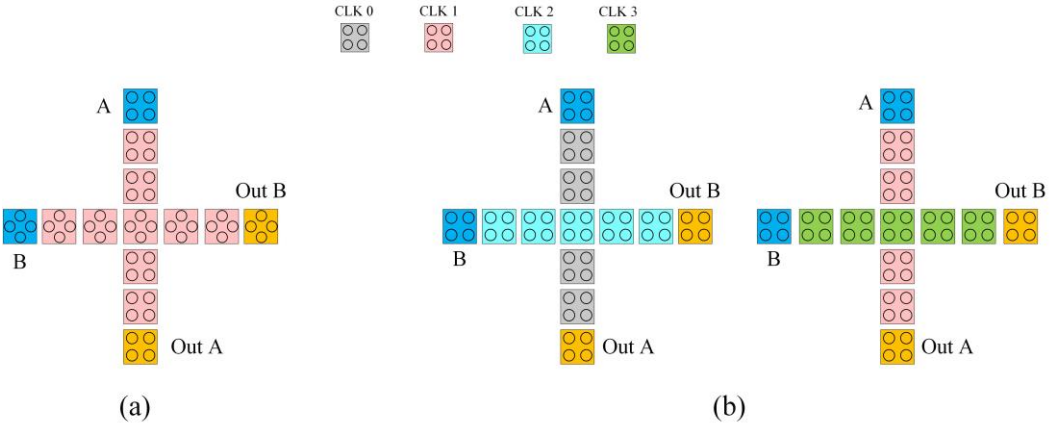

Fig. 6. Wire crossing in QCA: a) coplanar, b) coplanar clocking based

One of the most important issues in QCA technology is designing robust circuits against faults that may occur during the synthesis and chemical deposition steps. Common defects in QCA technology are divided into four categories: cell omission, cell displacement, cell misalignment, and extra cell deposition [18-20]. Cell omission defect occurs when a cell is missing compared to fault-free design (Figure 7.a). Cell displacement defect occurs when a cell is displaced from its original location (Figure 7.b). Cell misalignment defect occurs when the balance of the cells is disturbed (Figure 7.c). Finally, an extra cell deposition defect occurs when an additional cell is placed in the main structure (Figure 7.d).

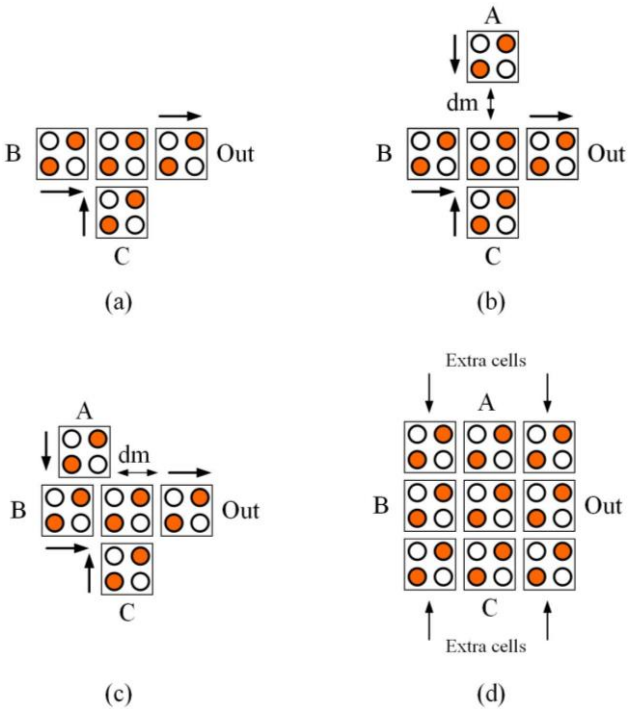

Fig. 7. Different kinds of defects: a) cell omission, b) cell displacement, c) cell misalignment, d) extra cell deposition.

3. THE PROPOSED THREE INPUT MAJORITY GATE

The three-input majority gate is one of the most important and basic gates in QCA technology since all types of digital circuits can be implemented using a combination of the majority and inverter gates. The area and energy-efficient robust circuits can be designed using fault-tolerant three-input majority gates with optimal area and energy consumptions. In this section, we first propose a fault-tolerant three-input majority gate and verify its functionality using QCA Designer 2.0.3 [21] simulator and physical proof (Kink energy). The proposed gate is then examined in terms of tolerance against cell omission, extra cell deposition, and cell displacement. After that, we compare our proposed gate with the previous majority gates.

The proposed three-input majority gate has 11 simple QCA cells and its area is 0.01 μm^2. The energy consumption of the proposed gate is also 1.49×e-002 MeV which is calculated by the QCA Designer-E simulator [30].

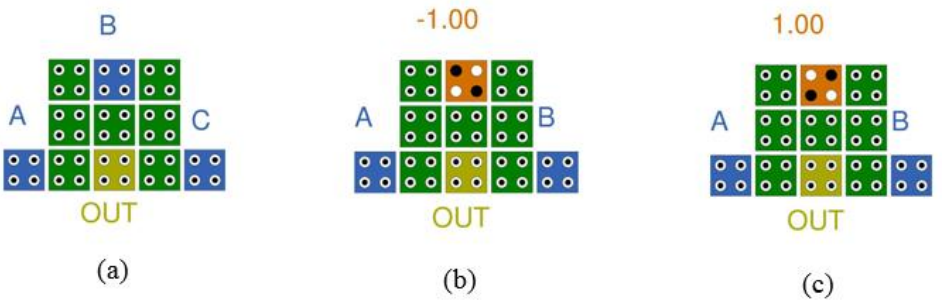

Fig. 8. a) The proposed fault tolerant three input majority gate, b) the proposed AND gate, c) the proposed OR gate**.**

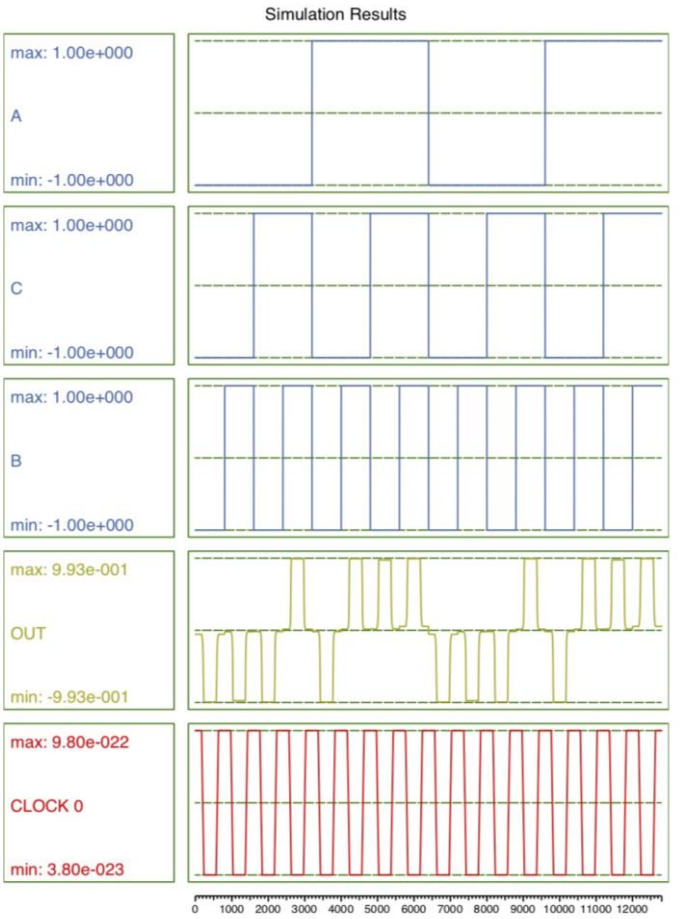

Fig. 9. The simulation results of the proposed majority gate.

Figure 8.a illustrates the proposed majority gate. As it can be seen, the output is generated during one clock phase. The simulation results of our proposed majority gate that is obtained from QCA Designer 2.0.3 are also shown in Figure 9. Two-input AND logic gates and OR logic gates can also be produced based on the proposed majority gate (Figure 8.b,c).

A. Performance evaluation using Kink energy

In this subsection we want to evaluate the proposed three-input majority gate using Kink energy. Since the majority gate has three inputs so it would have eight different modes which results in large number of calculations. In the following, we only consider the gate accuracy for the input mode (A, B, C) = (1, 0, 1).It is assumed that the quantum cells dimensions are 18 nm * 18 nm and the distance between two adjacent cells is 2 nm. The following formula is the one that calculate the energy between the electrons (Kink energy) [22, 23]:

$$\mathbf{U = \frac{kq_1q_2}{r}(J)} \tag{2}$$

In the mentioned formula, U represents the Kink energy, k is the Coulomb constant, q1 and q2 are the energy of the electrons, and r is the distance between the two electrons. By placing k and q, the resulting Kink energy is measured using the following formula:

$$\mathbf{U = \frac{9\times10^{9}\times1.6\times10^{-38}}{r} = \frac{23.04\times10^{-29}}{r}} \tag{3}$$

Table 1: The Kink energy between electrons e_1 to e_4 with electrons e_x and e_y in fig. 10.a and fig. 10.b

Figure 10.a		**Figure 10.b**	
Electron x	**Electron y**	**Electron x**	**Electron y**
$Ue_1 = 1.15\times10^{-20}$	$Ue_1 = 1.27\times10^{-20}$	$Ue_1 = 11.52\times10^{-20}$	$Ue_1 = 0.86\times10^{-20}$
$Ue_2 = 0.55\times10^{-20}$	$Ue_2 = 1.15\times10^{-20}$	$Ue_2 = 0.86\times10^{-20}$	$Ue_2 = 0.61\times10^{-20}$
$Ue_3 = 1.15\times10^{-20}$	$Ue_3 = 0.55\times10^{-20}$	$Ue_3 = 0.61\times10^{-20}$	$Ue_3 = 0.86\times10^{-20}$
$Ue_4 = 1.27\times10^{-20}$	$Ue_4 = 1.15\times10^{-20}$	$Ue_4 = 0.86\times10^{-20}$	$Ue_4 = 11.52\times10^{-20}$
$U_T = 8.24\times10^{-20}$		$U_T = 27.7\times10^{-20}$	

There are two possible arrangements of electrons by applying the input vector (A, B, C) = (1, 0, 1) to the proposed gate at a radius of less than 20 nm which are shown in Figure 10. We want to find the state in which the electrons are

more stable. First, the Kink energy of the electrons e_1 to e_4 by the electrons e_x and e_y are calculated using the Eq3 for the two states a and b in Figure 10. Table 1 shows the calculation results. As it is shown as the total Kink energy related to Figure 10.a is less than Figure 10.b, the output cell in Figure 10.a is more stable than Figure 10.b which confirms the correct direction of the output cell.

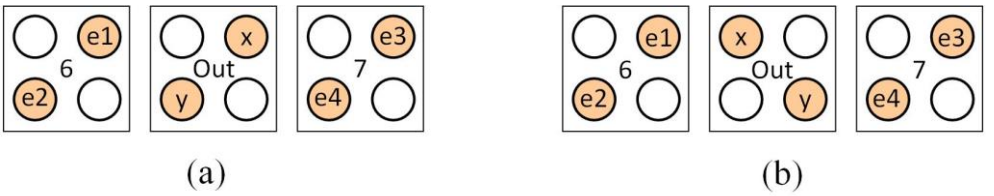

Fig. 10. a) Binary '1' output and b) binary '0' output.

B. Fault tolerance analysis through simulation

In this subsection, the circuit tolerance against possible defects such as single-cell omission, double cell omission, cell misalignment, and extra cell deposition is examined using QCA Designer 2.0.3 simulator.

One of the most likely defects in QCA technology is cell omission. Cell omission defect happens when one cell or more are missing compared to the fault-free design. Table 2 And Table 3 show the circuit output in all possible cases of single-cell and double-cell omission defects. According to these tables, if a single cell is deleted the output would be correct in five cases out of all possible seven cases and if two cells are removed, the output of six cases out of all 21 possible cases would be correct. So, if a single cell or two cells are omitted from the proposed majority gate the output would be 71% (= 5/7) and 29% (= 6/21) correct, respectively.

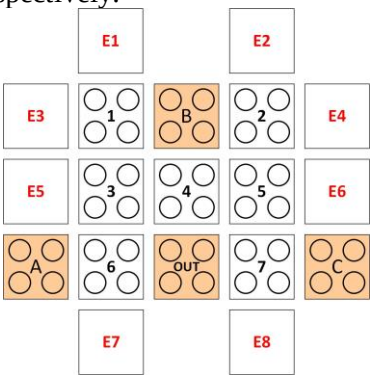

Fig. 11. Extra cells around the proposed majority gate.

In order to check the extra cell deposition defect, we place simple QCA cells all around the proposed majority gate as it is shown in Figure 11. The proposed gate output results after placing extra cells are in Table 4. According to this table, the output of the proposed gate is correct in all cases. Therefore, the tolerance of the proposed gate against additional cell deposition defects is 100%. In the following, an attempt has been made to investigate the effect of misalignment and displacement defects on the proposed gate. Table 5 shows the permitted displacement of all cells. As the results are shown, the proposed gate has a high tolerance against these defects.

Table 2 : The output of the proposed gate when single cell omission ocurred

Omitted cell	Output	Omitted cell	Output
1	Correct	5	Correct
2	Correct	6	Incorrect
3	Correct	7	Incorrect
4	Correct	**Correct rate = 71%**	

Table 3: The output of the proposed gate when double cell omission ocurred

Omitted cells	Output	Omitted cells	Output
1,2	Correct	3,4	Incorrect
1,3	Correct	3,5	Correct
1,4	Incorrect	3,6	Incorrect
1,5	Correct	3,7	Incorrect
1,6	Incorrect	4,5	Incorrect
1,7	Incorrect	4,6	Incorrect
2,3	Correct	4,7	Incorrect
2,4	Incorrect	5,6	Incorrect
2,5	Correct	5,7	Incorrect
2,6	Incorrect	6,7	Incorrect
2,7	Incorrect	**Correct rate = 29%**	

C. The proposed majority gate comparing to previous works

There are a large number of fault-tolerant three-input majority gates which have already been proposed. In this subsection, we compare our proposed majority gate with a group of best introduced majority gates. Table 6 summarizes the key characteristics of our proposed gate in comparison to the best related works.

Table 4: The proposed gate output when extra cell deposition defect occurred

Position	Output
E1	Correct
E2	Correct
E3	Correct
E4	Correct
E5	Correct
E6	Correct
E7	Correct
E8	Correct
Correct rate = 100%	

Table 5: The permissible range of cells displacement in the proposed majority gate

Cell	North (nm)	South (nm)	West (nm)	East (nm)
A	≤ 3	≤ 3	≤ 1	-
B	≤ 9	-	-	-
C	≤3	≤3	-	≤1
OUT	-	≤6	-	-
1	∞	-	∞	-
2	∞	-	-	∞
3	-	-	∞	-
5	-	-	-	∞
6	-	≤4	-	-
7	-	≤4	-	-

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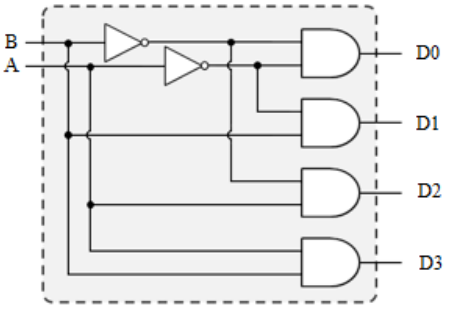
Table 6: Key characteristics of best robust QCA majority gates

Majority Gate	Cell Type	#Cell Count	Area (um^2)	Latency (clock cycles)	Total Energy (meV)	Average Energy (meV)	Tolerance Against Faults (%)			
							Single Cell Omission	Double Cell Omission	Extra Cell Deposition	Cell Displacement
[24]	rotated	13	0.01	0.25	4.87 × e-003	4.43 × e-004	88	39.5	100	0.1 - ∞
[25]	rotated	10	0.01	0.25	6.83 × e-004	6.21 × e-005	100	80	90	5 - ∞
[26]	simple	25	0.02	0.25	1.57 × e-002	1.42 × e-003	80	36	undefined	undefined
[27]	simple	37	0.05	0.25	9.32 × e-003	8.48 × e-004	82	66	50	3 - 14
[28]	simple	36	0.05	0.25	2.31 × e-002	2.1 × e-003	93.8	66	undefined	undefined
[29]	simple	20	0.03	0.5	1.96 × e-002	1.78 × e-003	87	60	100	5.2 - 500
[43]	simple	27	0.02	0.25	1.8 × e-002	1.64 × e-003	100	85	100	4 - ∞
[44]-first structure	simple	13	0.01	0.25	1.76 × e-002	1.6 × e-003	88	41	100	1.5 - ∞
[44]-second structure	simple	18	0.02	0.25	1.52 × e-002	1.38 × e-003	91	62	100	3 - ∞
proposed	Simple	11	0.01	0.25	1.49 × e-002	1.35 × e-003	71	29	100	3 - ∞

As it is shown in Table 6 the majority gates proposed in [26-29, 43, 44] were designed using only simple QCA cells but [24, 25] have presented some other majority gates which are based on both simple and rotated QCA cells. As mentioned before, the rotated QCA cells decrease the robustness of QCA designs since they are more susceptible to faults during the fabrication process. Therefore, our proposed gate is more reliable than [24, 25] works.
Comparing our proposed majority gate to those previous works which only employed simple QCA cells, it has lower cell count, area, and energy consumptions and in most cases with an average better tolerance against common QCA faults.

4. THE PROPOSED DECODER

A decoder is a combinational logic circuit that converts n coded inputs to 2n unique outputs. Decoders are widely employed in many applications and play an important role in many electronic circuit designs including lookup tables and random-access memories [31-33]. Optical decoders are also employed widely in optical logic circuits [45, 48]. Therefore, it is very important to design and implement a fault-tolerant decoder that is optimal in terms of energy consumption and area. Figure 12 shows the truth table and digital circuit design of a 2-to-4 decoder.



A	B	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Fig. 12. Digital circuit design and truth table of a 2-to-4 decoder

In the proposed decoder, four majority gates are used as Eq.4 order to make the outputs:

$$\begin{aligned} \mathbf{D0} &= \mathbf{MV(0, A', B')} \\ \mathbf{D1} &= \mathbf{MV(0, A', B)} \\ \mathbf{D2} &= \mathbf{MV(0, A, B')} \\ \mathbf{D3} &= \mathbf{MV(0, A, B)} \end{aligned} \tag{4}$$

Figure 13 illustrates a 2-to-4 decoder circuit design based on the proposed majority gate. As it is shown the relevant circuit has two inputs named A and B and produces four outputs which are D0, D1, D2, and D3. The proposed decoder is simulated and verified with QCA Designer 2.0.3 simulator. The layout and simulation results of the proposed decoder are shown in Figure 13 and Figure 14, respectively.

Each majority gate of the proposed circuit needs a clock phase to operate properly and the decoder output is ready after five clocks. The introduced single-layer decoder circuit has 137 cells which is more area efficient in comparison to the other proposed coplanar decoders. The simulation results show that only one of the decoder outputs has a value of one in each clock and the rest of the outputs are zero which is proof of the functional correctness of the proposed decoder.

Table 7. Characteristics analysis of the 2 to 4 decoders

Decoder circuits	Crossover type	Number of majority gates	Cell count	Area (um^2)	Fault tolerant
[34]	coplanar	8	270	0.38	-
[35]	coplanar	8	296	0.43	-
[36]	coplanar	6	212	0.25	-
[37]	coplanar	4	193	0.22	-
First design [38]	coplanar	4	110	0.13	-
Second design [38]	coplanar	4	159	0.18	-
[31]	multilayer	4	100	0.09	-
First design [46]	coplanar	6	56	0.05	-
Second design [46]	Multilayer	6	62	0.05	-
Proposed	coplanar	4	137	0.15	☑

Table 7 compares the presented decoder to already introduced decoders. This comparison is performed in terms of crossover type, the number of majority gates, the number of cells, occupied area, and fault tolerance. As it is shown, works that are introduced in [34-37] consume more cell count and area in comparison to our proposed decoder.

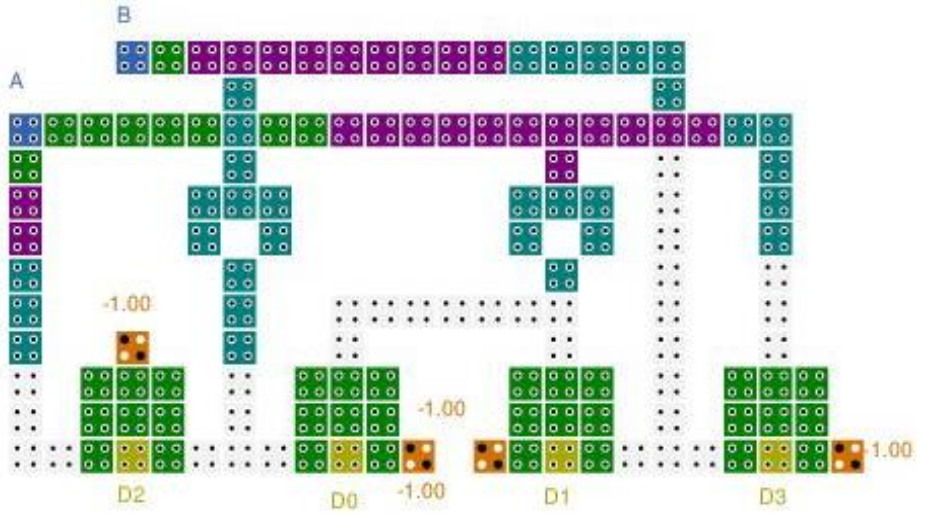


Fig. 13. The QCA layout of the proposed 2-to-4 decoder

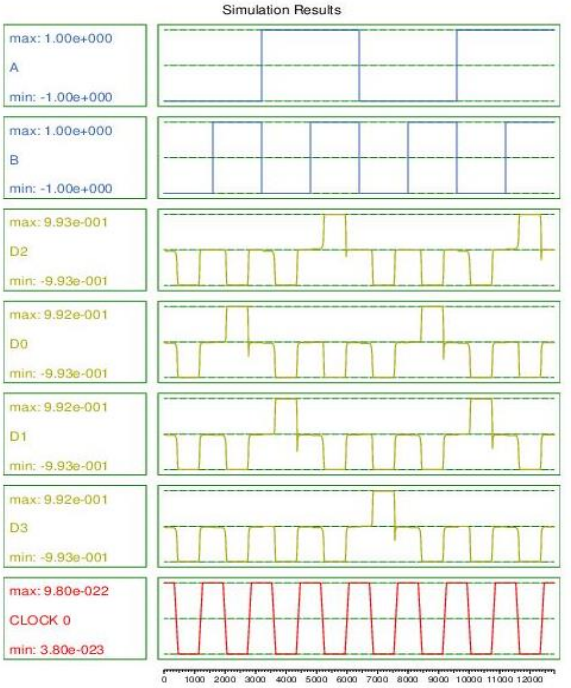


Fig. 14. The simulation results of the proposed 2-to-4 decoder

There are two different designs that were proposed in each [38] and [46] work. While the second design of [38] consumes more area, the first design of [38] and both designs of [46] are area efficient comparing to our work. But none of the first and second designs in [38] and [46] are fault-tolerant. The presented decoders in [31] and the second design in [46] are multilayer designs which increase the fabrication overheads. In fact, our proposed decoder is the only fault-tolerant coplanar design which is area efficient in comparison to most of the previous works.

5. CONCLUSION

One of the most important and suitable alternatives to CMOS is the QCA technology due to its high density, low power, and high-speed characteristics. Fault tolerant circuit design is the most important issue in QCA technology. In this paper, we have proposed a coplanar robust 2-to-4 decoder based on a novel fault-tolerant three-input majority gate using the QCA technology. The proposed majority gate has 71% and 100% tolerance against single-cell omission and extra-cell deposition defects, respectively with a suitable tolerance against cell displacement and misalignment defects. We have finally designed a coplanar area and energy-efficient robust 2-to-4 decoder using the presented majority gate.

CONFLICT OF INTEREST

The authors state that publication of this manuscript does not involve any conflicts of interest.

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