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Device and Circuit Performance Simulation of a New Nano-Scaled Side Contacted Field Effect Diode Structure

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Abstract: A new side-contacted field effect diode (S-FED) structure has been introduced as a modified S-FED, which is composed of a diode and planar double gate MOSFET. In this paper, drain current of modified and conventional S-FEDs were investigated in on-state and off-state. For the conventional S-FED, the potential barrier height between the source and the channel is observed to become larger and the flow of injected electrons is reduced. Thus, the drain current decreases in on-state. While in off-state, the potential barrier height and width become smaller in conventional S-FED and so the drain current is greater than that of modified structure. Mixed mode simulations were used to determine the performance of the proposed logic gates. We compared the operation of modified S-FED with that of conventional S-FED. Simulated power delay product (PDP) of the modified S-FED-based NOR, NAND, XOR gates were found to be about 416fJ, 408fJ and 336fJ, respectively, compared with 906fJ, 810fJ and 705fJ achievable with conventional S-FED logic gates.

Keywords: Logic Gates, Off-State, On-State, Propagation Delay, Static Power Dissipation, Power Delay Product.

1. INTRODUCTION

As MOSFET scaling continues down to the sub-50 nm scale, some new structures are likely to replace conventional bulk devices [1-4]. To extend the scalability of CMOS technology in sub nanometer regime, short channel effects (SCEs) such as large drain induced barrier lowering (DIBL), increased leakage current, poor sub-threshold swing (SS) and threshold voltage roll-off are the major challenges [5-7]. Researchers have been working on different structures through these years and have presented devices with improved performances. One of these devices is field effect diode (FED) which has been developed in recent years due to the better electrostatic control of the charges and partly

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because its fabrication procedure is similar to CMOS processing[8-9]. A FED is similar to a conventional MOS transistor with the exception of using two gates over the channel region and oppositely doped source and drain. FED device, as compared to SOI-MOSFET with similar dimensions, provides superior advantages in terms of subthreshold slope, threshold voltage, on-state current, off-state current and intrinsic gate delay [10-12].

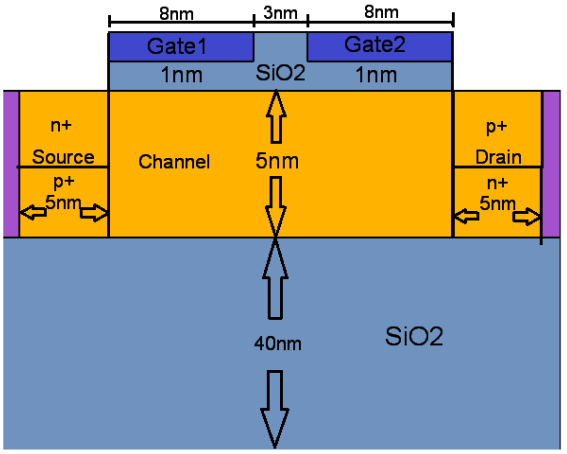
Applying biases to $gate_1$ and $gate_2$ simultaneously and field line density between drain and source regions due to drain-source voltage, controls the barrier height at source-channel and drain-channel junctions. However for channel lengths in nanometer regime, field line density originating from drain-source voltage becomes dominant, thus the device does not turn off [13-14].

Although the fabrication of FEDs is similar to the standard CMOS process, extra steps are inevitable to form reservoirs and source/drain regions. The source/drain regions can be introduced over the reservoirs using ion implantation. However, due to the demand for very shallow source/drain regions, this method may not be practically feasible. To make the fabrication of these devices more feasible, side-contact field effect diode has been proposed [8]. Side contacts are created by utilizing trench technology. Creating side contacts to the source and drain areas can be performed by reactive ion etching and using an oxide layer as an etch stop. In this structure, source and drain contacts can be epitaxially grown [9]. The rest of the fabrication steps are similar to those of the standard CMOS fabrication steps.

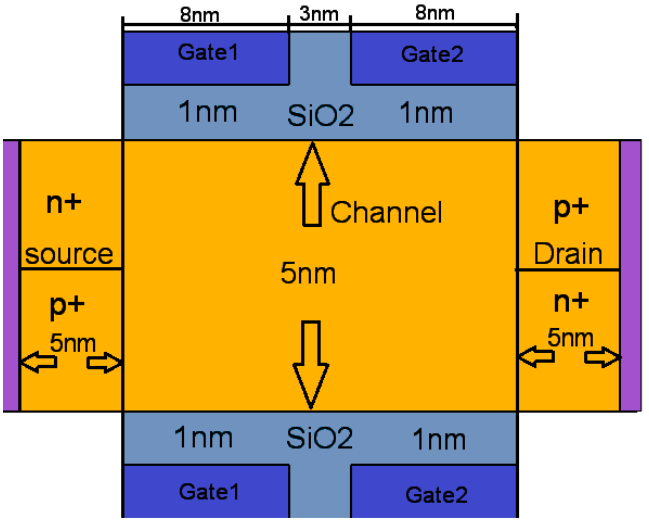
In this paper, the operation of the new modified side-contacted field effect diode (S-FED) structure is compared with that of the conventional S-FED. Also, we explore the possibility of designing nanoscaled logic gates with a reduced propagation delay and static power dissipation. The main goal of this study is to design high-performance logic gates, such as NOR, NAND and XOR, based on the nanoscaled modified S-FED. The logic gates parameters, including propagation delay time (t_p), static power dissipation (P_{diss}), and power delay product (PDP), are evaluated and compared with their corresponding of conventional S-FED products.

2. DEVICE STRUCTURE AND SIMULATION METHOD

Fig. 1 shows the proposed modified S-FED as well as the conventional structure. In this study, the structures have a body length of 5 nm and a gate oxide thickness of 1nm. The channel of devices is intrinsic silicon, the source and drain regions are highly doped Silicon (10^{20} cm^{-3}), and those are in the same lengths ($L_{S,D}$ = 5nm). The spacer length between the gate edges is 3nm and the gate lengths are 8nm with the workfunction of 4.7eV.



(a)



(b)

Fig. 1. The schematic view of (a) conventional S-FED and (b) proposed modified S-FED structures.

In the nanometer regime, the wave-like behavior of electron becomes significant, and the tunneling current should be considered [15]. The effects due to confinement of carriers associated with variations of local potential on the scale of the electron wave functions (i.e. Quantum effects) can be modeled using density gradient [16-17].

For the solution of the density gradient corrected drift diffusion approximation, we use a modified Gummel approach [18] where the Poisson equation (1) and density gradient equation (2), for a given electron Fermi-level distribution, are solved self-consistently for the electrostatic potential and the quantum-corrected electron density [19]:

$$\nabla.(\varepsilon\nabla\psi) = -q(p - n + N_D^+ - N_A^-) \tag{1}$$

$$\frac{2b_n^*}{S}\left(\frac{1}{m}\nabla^2 S\right) = \phi_n - \psi + \frac{K_B T}{q}\ln(S^2) \tag{2}$$

Where $S = \sqrt{n/n_i}$, $b_n^* = \hbar/4qr$, ϕ_n is quasi Fermi level, ψ is the electrostatic potential, ε is the local permittivity, K_B is Boltzmann's constant, T is lattice temperature and m is carrier effective mass.

The effective quantum-corrected potential is calculated from [19]:

$$\psi_{eff} = \psi + \frac{2b_n^*}{S}\left(\frac{1}{m}\nabla^2 S\right) = \phi_n + \frac{K_B T}{q}\ln(S^2) \tag{3}$$

and is then used as the driving potential for the current continuity equation:

$$\nabla.J_n = 0 \tag{4}$$

Where:

$$J_n = -qn\mu_n\nabla\psi_{eff} + qD_n\nabla n \tag{5}$$

which is solved using a standard Sharfetter-Gummel discretization based on the effective quantum-corrected potential. The set of equations are solved using 2D Silvaco ATLAS simulator [20]. High doping concentrations band gap narrowing (BGN) [21] and Auger recombination [22] models are included in the simulations. Because of presence of high impurity atom and also consideration of an interface trap (or defect) effect, Shockley-Read -Hall (SRH) [23-24] model is also included. In the Simulations, the concentration dependent mobility model for low field mobility related to doping density and the field-dependent mobility model for high field velocity saturation depending on the parallel electric field in the direction of current flow are also considered [20].

The equations 1, 2 and 4 are solved self consistently until convergence. Dirichlet boundary condition is used for the source and drain contacts.

3. RESULTS AND DISCUSSIONS

Fig. 2 represents the drain current of conventional and modified S-FEDs in the on-state. The applied biases to the gate1 and gate$_2$ contacts are V_{G1}=0.6V, V_{G2}=0.8V, respectively. Applying bias to gate$_1$ and gate$_2$ cannot modulate the barrier height at source/channel interface and drain/channel interface, respectively. Hence electrons injection from the source into the channel, under gate$_1$ are increased and holes injection from the drain into the channel, under gate$_2$ are also increased.

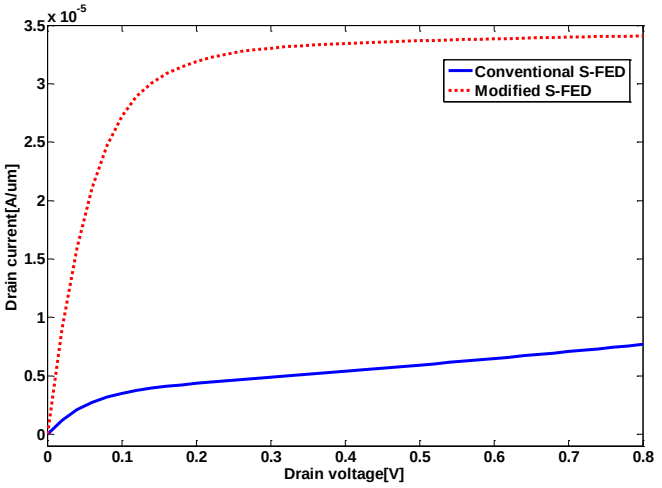


Fig. 2. Drain current versus drain voltage of conventional and modified S-FEDs in on-state (V_{G1} = 0.6V, V_{G2} =0.8V)

As shown in Fig. 3, a thermal barrier is against the electron at source/channel interface. The energy of source electrons which are equal or greater than peak potential of the thermal barrier, overcome the barrier by thermionic emission and contribute to the current flow. For the conventional S-FED, the potential barrier height between the source and the channel is observed to become larger and the flow of injected electrons is observed to reduce. Thus, the drain current decreases. On the other hand, the source-to drain tunnelling current in the modified S-FED is greater due to a smaller barrier width which is the main contribution to the transmission until the total electron energy is below the top of the barrier.

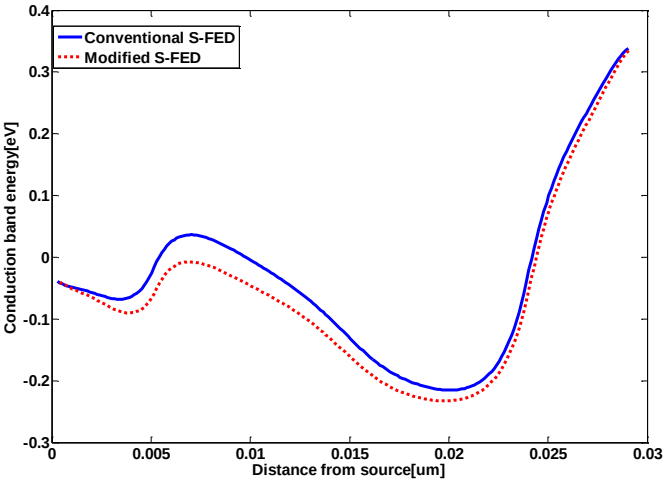


Fig. 3. Conduction band energy of conventional and modified S-FEDs in on-state (V_{G1} =0.6V, V_{G2} =0.8V, V_D=0.8V).

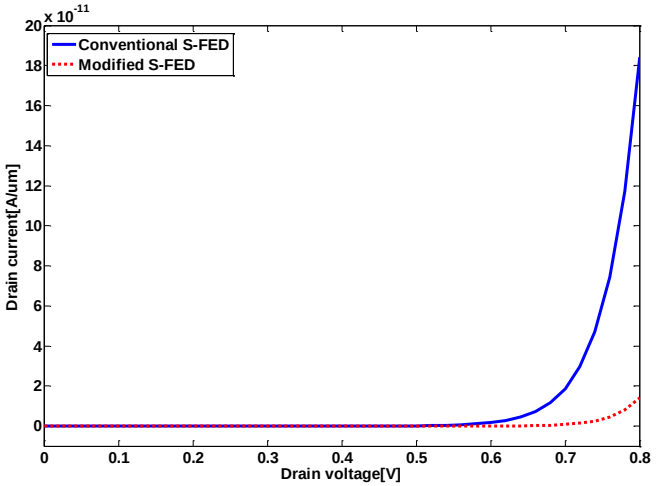


Fig. 4. Drain current versus drain voltage of conventional and modified S-FEDs in off-state (V_{G1}=-0.6V, V_{G2} =0.8V).

Fig. 4 shows the drain current versus drain voltage of conventional and modified S-FEDs in the off-state. In the S-FED structures with the applied biases V_{G1}=-0.6V, V_{G2}=0.8V, p^+ and n^+ reservoirs in the source and the drain regions cause hole injection into the channel under $gate_1$, and electron injection into the channel under $gate_2$, respectively. So an n^+pnp^+ structure forms and the device turns off. The applied bias to the $gate_1$ creates a large thermal barrier

against the electron at the source/channel interface; hence, the injected electron density from the source into the channel reduces.

As it can be seen in Fig. 5, the potential barrier and potential width in conventional S-FED is smaller than modified structure. So the drain current of conventional S-FED is greater than that of modified structure in off-state.

Fig. 6 shows drain current versus gate$_1$ voltage (I_D-V_{G1}) at V_{G2}=0.8V, V_D =0.8V. From this figure, on-state and off-state currents are achieved 78.4µA and 183pA, respectively, for conventional S-FED. Those are 192µA and 15.6pA for the modified S-FED. On-state and off-state currents are obtained at V_{G1}= 0.6V and V_{G1}=-0.6V, respectively, when V_D=0.8V and V_{G2}=0.8V. It can be concluded from the results that I_{ON}/I_{OFF} ratio in modified S-FED (I_{ON}/I_{OFF}=12.3×10^6) is larger than that of conventional S-FED (I_{ON}/I_{OFF}=4.3×10^5). Therefore, the proposed structure is a good candidate for digital applications.

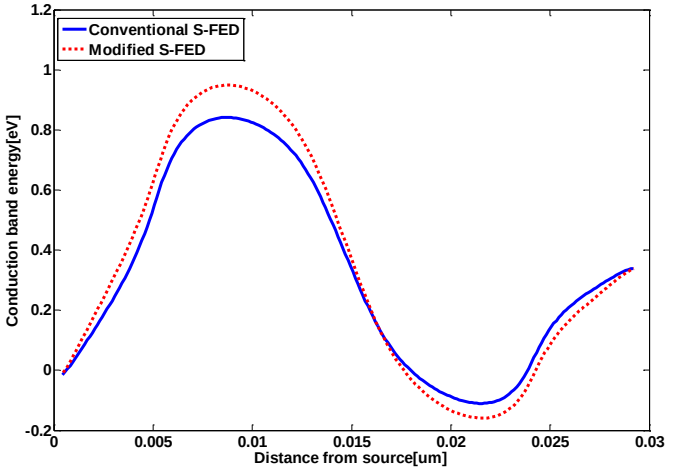


Fig. 5. Conduction band energy of conventional and modified S-FEDs in off-state (V_{G1}=-0.6V, V_{G2} =0.8V, V_D=0.8V).

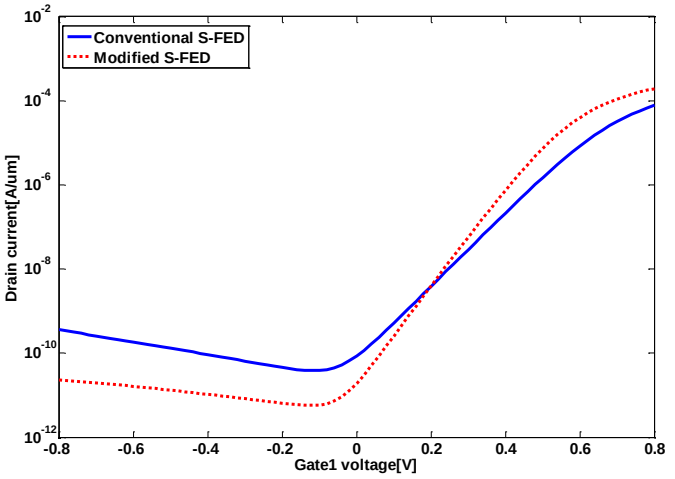
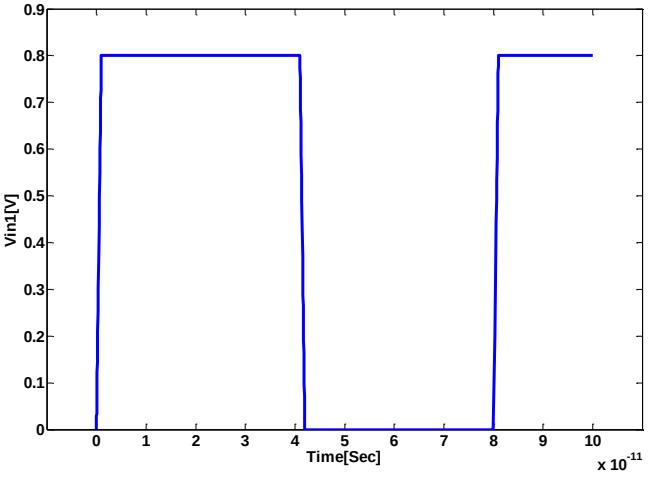
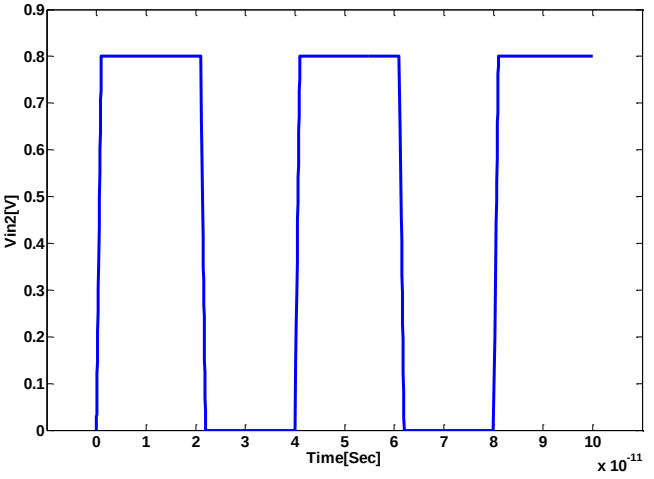


Fig. 6. Drain current versus gate$_1$ voltage of conventional and modified S-FEDs at V_{G2}=0.8V, V_D =0.8V.



(a)

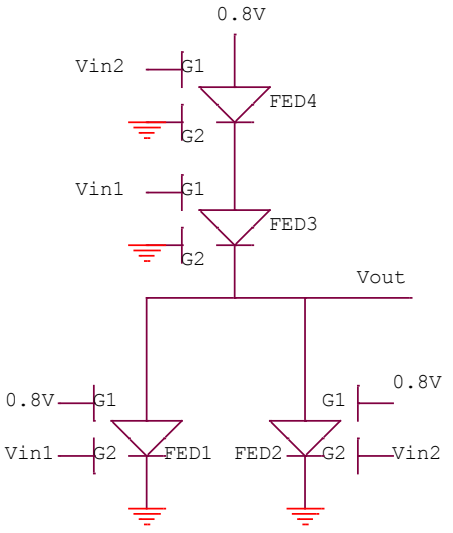


(b)

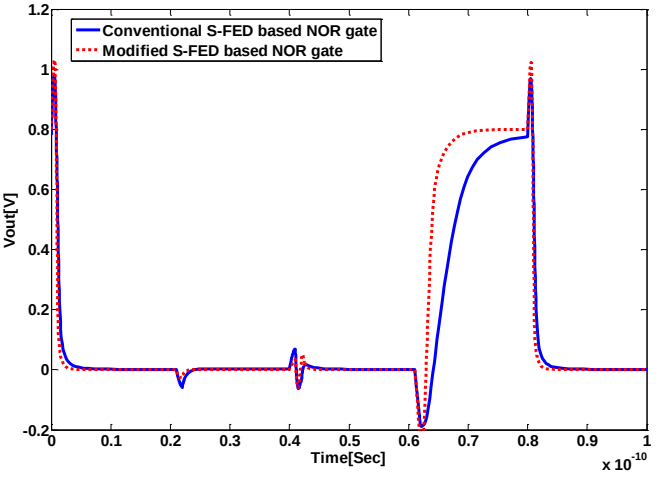
Fig. 7. Inputs of the presented structures (a) Input1: the pulse width and period are 40ps and 80ps, respectively. (b)Input2: The pulse width and period are 20ps and 40ps, respectively.

In this section, fundamental logic gates, including NOR, NAND, and XOR are designed as the building blocks in other logic gate bodies. Mixed-mode simulations are performed to design and characterize the logic gate parameters. Since there are two inputs to evaluate the performance of the logic gates, one is a square wave with the pulse width, period of 40ps, 80ps respectively, and the other one is a square wave with the pulse width, period of 20ps, 40ps, respectively, with the rise and fall times of 1ps, which are shown in Fig. 7.

Fig. 8(a) shows the circuit of NOR gate and Fig. 8(b) demonstrates the output waveform of this logic gate while the square wave is applied to the circuit input. The propagation delay time of modified S-FED based NOR gate and conventional S-FED based NOR gate are 8.5ps and 26ps, respectively. The propagation delay (t_p) is the average of the t_{PLH} and t_{PHL} : $tp = (t_{PLH} + t_{PHL})/2$. The t_{PLH} defines the response time of the gate for a low to- high output transition while t_{PHL} refers to a high-to low transition. The t_{PLH} and the t_{PHL} of the modified FED NOR gate have been found to be about 2.6ps and 0.6ps, respectively, compared with 8.3ps and 1ps achievable with the conventional FED NOR gate.



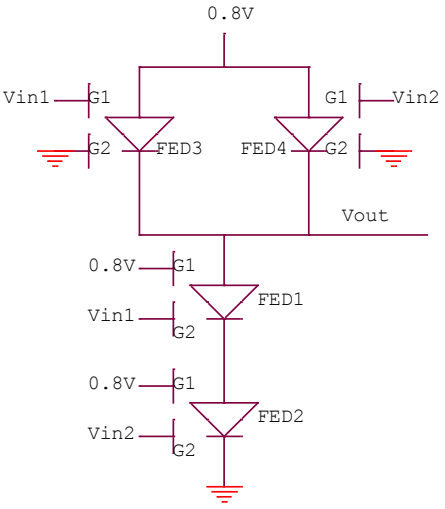
(a)



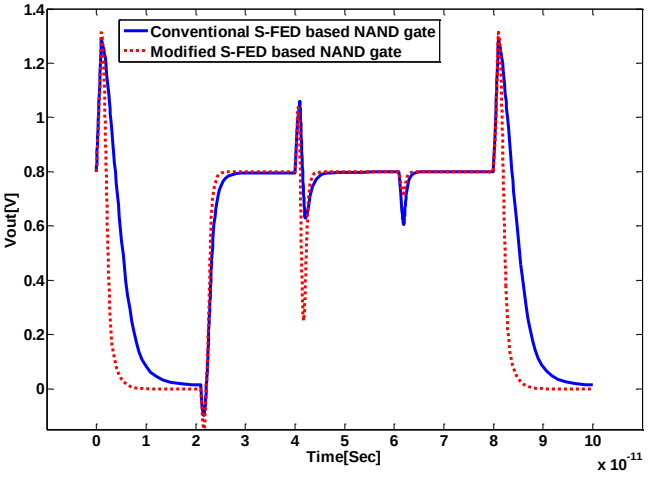
(b)

Fig. 8. (a) S-FED based NOR gate. (b) Output waveform.

The two-input NAND gate (Fig. 9(a)), is composed of pull up and pull down networks. FED_3 and FED_4 are parallel in pull up network, and FED_1 and FED_2 are serial in pull down network. As either FED_3 or FED_4 is turned ON, the output becomes "1". Also, since both FED_1 and FED_2 are turned ON, the output becomes "0". In Fig. 9(b), it can be seen that propagation delay time of modified S-FED based NAND gate and conventional S-FED based NAND gate are 1.7ps and 4.5ps, respectively.



(a)



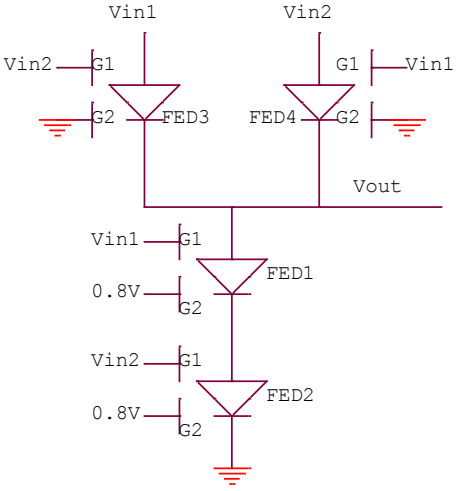
(b)

Fig. 9. (a) S-FED-based NAND gate. (b) Output waveform.

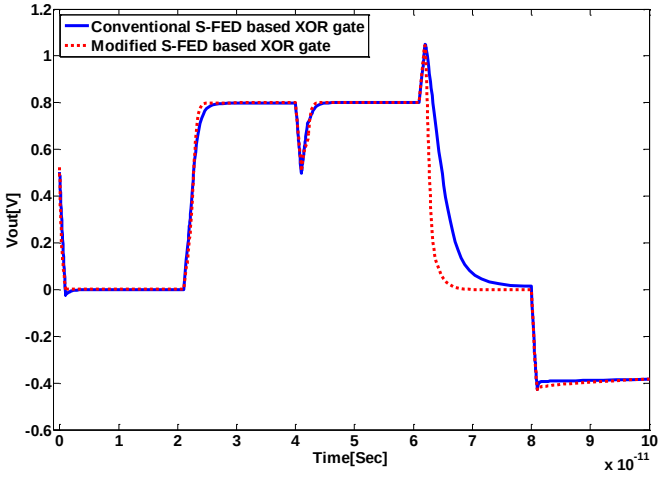
Fig. 10(a) indicates the internal circuit of XOR gate. Fig. 10(b) compares the transient responses of the XOR gate in terms of the propagation delay. The propagation delay of the XOR gate based on modified S-FED is 1.5ps and it is 4.2ps for the other structure.

A comparison between the parameters of interest, i.e., propagation delay, power dissipation, and PDP of the logic gates based on presented structures are shown in table 1 and table 2. As it can be apparent from the tables, power dissipation in conventional S-FED based logic gates is less than that of

corresponding modified S-FED based ones. In the interaction between speed and power dissipation, the PDP asserts that the modified S-FED gates have a significant advantage over the conventional S-FED counterparts.



(a)



(b)

Fig. 10. (a) S-FED-based XOR gate. (b) Output waveform.

Table 1. Characteristics of modified S-FED-based logic gates.

	NOR	NAND	XOR
Power Dissipation [nW]	260	240	224
Propagation Delay [ps]	1.6	1.7	1.5
Power Delay Product[fJ]	416	408	336

Table 2. Characteristics of conventional S-FED-based logic gates.

	NOR	NAND	XOR
Power Dissipation [nW]	195	180	168
Propagation Delay [ps]	4.65	4.5	4.2
Power Delay Product[fJ]	906	810	705

4. CONCLUSION

In this paper, the electrical characteristics of new modified S-FED have been investigated, and the results have been compared with those for the conventional S-FED. It has been shown that the modified S-FED had higher on-state current and lower off-state current. The potential barrier and potential width of conventional S-FED in off-state is smaller than modified structure which yields higher off-state current. Higher on-state current in modified structure is because of low potential barrier and narrow potential width.

These devices were used in NOR, NAND and XOR logic gates. The results show a reduction up to 60% in propagation delay and improvement up to 40% in PDP in logic gates based on modified S-FED. The analysis presented here decisively confirms that the application of the modified S-FED in the switching circuits will meet the requirements in designing nanoscaled devices with enhanced speed.

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