Effects of the Channel Length on the Nanoscale Field Effect Diode Performance

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Abstract: Field Effect Diode (FED)s are interesting device in providing the higher ON-state current and lower OFF–state current in comparison with SOI-MOSFET structures with similar dimensions. The impact of channel length and band-to-band tunneling (BTBT) on the OFF-state current of the side contacted FED (S-FED) has been investigated in this paper. To find the lowest effective channel length, this device is simulated with 75, 55 and 35 nm channel length and the results obtained are presented in this article. Our numerical results show that the I_{ON}/I_{OFF} ratio can be varied from 10^4 to 10^0 for S-FED as the channel lengths decrease. We demonstrate that for channel lengths shorter than 35 nm by considering the Band-to-Band tunneling model, the S-FED device does not turn off.

1. INTRODUCTION

As the scaling of Cmos transistor extends to the nano-scale regime, the performance of the device degrades mainly because of short-channel effects that arise due to weakened gate control [1-3]. Hence, in recent years, new devices have been proposed on a nanoscale. One of these devices is the Field Effect Diode (FED), whose physical structure is depicted in Fig. 1 The structure of FED is similar to that of the conventional MOSFET, with the exception of oppositely doped source and drain regions and also the configuration of the gates. This device was first proposed in 1996 [4].

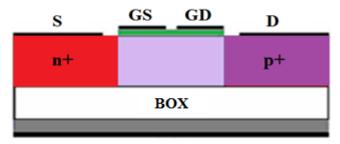* Corresponding author. E-mail: **arashrezaei92@yahoo.com**

Fig. 1. Schematic of the FED structure

The FED has a higher current than the MOSFET, and a lower leakage current. Therefore, the ION / IOFF ratio, which is one of the most important parameters in digital applications, is more in this device than field-effect transistors with similar dimensions [5, 6]. Field effects diodes have many applications such as ESD protectors [7, 8] and memory cells [9, 10], and can also be used to design integrated circuits [11,12]. As the channel length is scaled below 100 nm, the off-current of regular FEDs increases. To overcome this problem, modified FED (M-FED) (Fig. 2(a)) and side-contacted FED (S-FED) (Fig. 2(b)) structures have been recently proposed [13, 14].In this structure, there are regions in the source and drain areas called reservoir. These introduced regions assist nanoscale FEDs to be turned OFF. The reason the reservoirs are used in nanosized FEDs is that, when the device is off, the carriers that enter from drain and source into the channel are injected into opposite channel sides before annihilation.
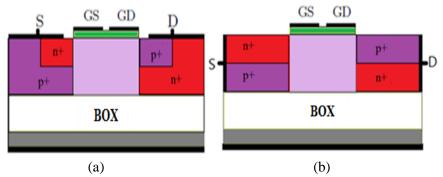

(a)   (b)

Fig. 2. Schematic cross-section of (a) M-FED and (b) S-FED

When channel length decreases in these devices, the tunneling current in the channel is increased and the performance of the field effect diode is disrupted. In this paper, the effect of the channel length on the electrical characteristics and Energy Levels of S-FED is investigated and also compared.

2. DEVICE STRUCTURE

A FED is a structure with two gates over its channel called GS and GD (see Fig. 1) and oppositely doped source and drain regions. The gate contacts of FEDs can be biased such that either a p-n or n-p channel replaces the lightly doped or intrinsic region between the source and drain areas. Based on the gate, source, and drain voltages, the source/channel/drain areas act as n+-n-p-p+ and n-+p-n-p+ structures, respectively. Fig. 1 shows a regular FED based on a SOI structure, where the source and the drain have n-type and p-type doping, respectively. This FED will be in the ON-state if positive and negative voltages are applied to GS and GD, respectively. By just reversing the gate-voltage polarities, the device will be turned off. In the OFF-state, the device has a structure similar to a silicon-controlled rectifier (n-p-n-p). However, as the channel length shrinks below 100 nm, regular FEDs cannot
be turned off [15]. To suppress this problem, M-FEDs have been proposed [15]. In this structure, oppositely doped regions called reservoirs are introduced to the source and drain areas
of regular FEDs (see Fig. 2(a)), where they assist the gate contacts to accumulate more holes and electrons under GS and GD, respectively, and induce a larger surface potential. In other words, in the OFF-state, the excess minority carrier injection takes place across the forward-biased n+-p (source side) and n-p+ (drain side) junctions, causing an increase in the electron and hole concentrations in the p-region (under GS) and the n-region (under GD), respectively. This increase in the electron and hole concentrations obstructs the formation of a reverse-biased p-n junction in the channel. Therefore, to achieve a proper OFF-state current, excess electrons and holes under GS and GD should be reduced. The reservoirs connect the p-region under GS to the source and the n-region under GD. As a result, the forward bias of the n+-p and n-p+ junctions decreases, and the carrier injection into the channel is reduced. In a forward-biased FED, the drain voltage and the neighboring gate have opposite polarities; therefore, pinchoff does not occur in FEDs, and they do not suffer from hot-electron effects, unlike short-channel FETs [4, 16].
To make the fabrication of these devices more feasible, we propose an S-FED. As shown in Fig. 2(b), side contacts are created by utilizing trench technology. Creating side contacts to the source and drain areas can be performed by reactive ion etching and using an oxide layer as an etch stop.
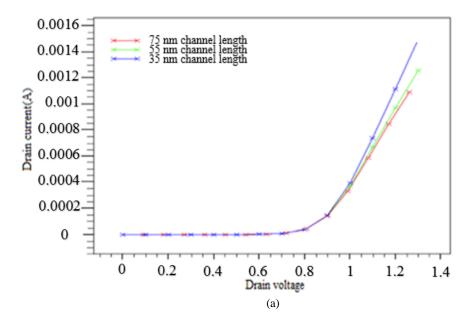
2. RESULTS AND DISCUSSION

In this section, the results of the simulation performed by the ATLAS simulator are examined [17]. We have solved the poisson and continuity equations to obtain the electrical characteristics of the FED, including I-V characteristics and carrier concentrations under each gate.

The FED operation can be explained in terms of a pin diode in which the potential in its intrinsic region is controlled by two gates over the channel. In the side-contacted FED (Fig. 2(b)), the source region is n-type with a donor density 1×10^{21} cm^{-3}, drain doping is p-type with 1×10^{21} cm^{-3} density, and the so-called intrinsic channel is actually doped with donor type impurities to 1×10^{14} cm^{-3}. The gate oxide thickness of 1 nm and a device width are 1 um. The depths of reservoirs and source/drain regions are 50 and 25 nm, respectively. These values and other structural parameters are those employed in [13, 14].

The BTBT model and Shockley–Read–Hall (SRH) model are especially needed for accurate estimation of the leakage currents. The mobility models which account for the lattice scattering, impurity scattering, conmob, field-dependent mobility, carrier–carrier scattering and impurity clustering effects at high concentration are employed. For the accuracy of the ON-current, mobility degradation due to the high transverse electric field is considered.

The output characteristics of S-FED structures as a function of the Channel Length are compared in Fig. 3 in the (a) on and (b) off state. As seen in this figure, by decreasing the length of the channel, the on and off current will be increases. In the other words, as Channel Length decreases, The tunnel flow in the channel increases is due to the closeness of the source and drain area.
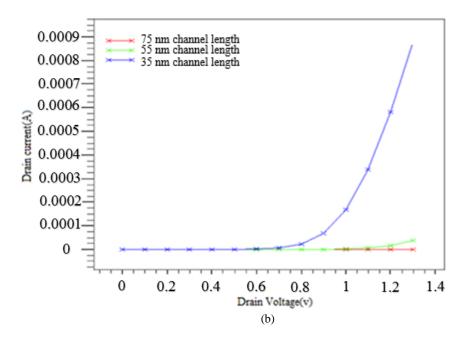

(a)

(b)

Fig. 3. Output characteristics of the S-FED as a function of the channel length in the (a) ON and (b) OFF state

As a result, for the channel lengths shorter than 35 nm, S-FED cannot be turned off. However, S-FED device suffers from an increase in I_{OFF} if channel length is scaled.

Table I shows a comparison between the S-FED structure with similar dimensions for channel length of 35, 55 and 75 nm, taking into account the tunneling phenomenon.
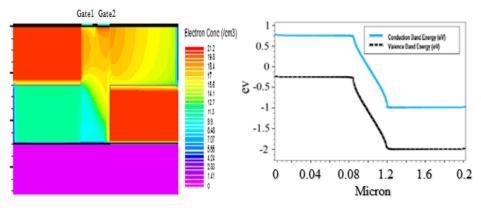
TABLE I

Comparison of simulation results of S-FED structure for channel length 35, 55 and 75 nm, Vd =1.3v, Vg =1v and considering the tunneling phenomenon
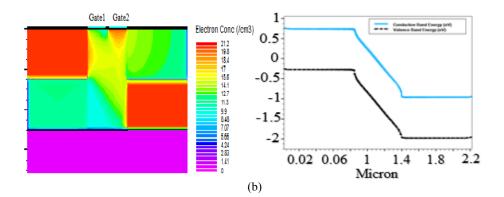
Device	Channel length	I_{ON}	I_{OFF}	I_{ON}/I_{OFF}
S-FED	75 nm	1.05 mA	90.8 nA	$1.15×10^4$
S-FED	55 nm	1.25 mA	39 uA	32.05
S-FED	35 nm	1.5 mA	0.87 mA	1.72

Fig. 4 illustrates the electron density and band diagram at a depth equal to 27 nm at the S-FED device in the OFF-state for 35, 55 and 75 nm channel length. Upon scaling electron direct tunneling from source to drain plays a major role in the OFF-state current. It appears that in the S-FED device physics reported in [14] no BTBT has been taken into account.
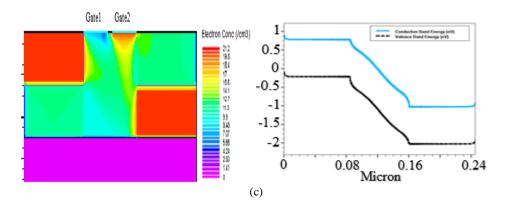

(a)

(b)

(c)

Fig. 4. Electron density and band diagram at a depth equal to 27 nm when the BTBT model is included in (a) the 35 nm channel length S-FED structure and (b) the 55 nm channel length S-FED structure (c) the 75 nm channel length S-FED structure.

Fig. 5 compares the band diagram at a depth equal to 27 nm when the BTBT model is included for various channel lengths.by decreasing the channel length, the electron direct tunneling from source to drain is increases.
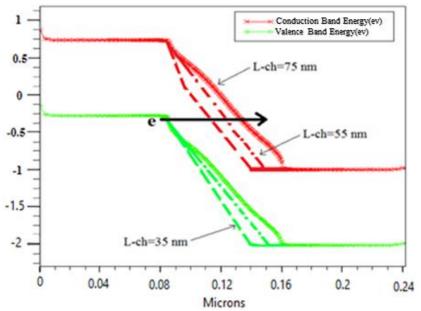

Fig. 5. Energy band diagram taken horizontally across the S-FED at distance 27 nm from the surface when the BTBT model is included

S-FED cannot be turned off for channel lengths equal to 35 nm and the shorter. As a result, OFF-state current is increased noticeably for the 35 nm channel length in comparison with that 55 and 75 nm channel length of the S-FED. Figure.6 shows the changes in energy levels at 2 nm below the gate in off state. As expected, by decreasing channel length, the potential dam is reduced.
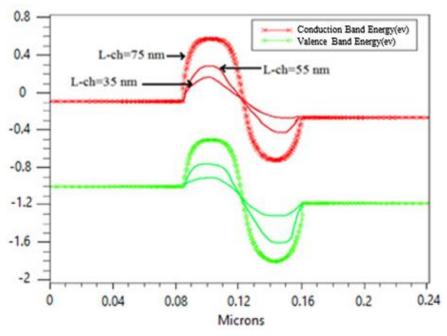

Fig. 6. Energy band diagram taken horizontally across the S-FED a distance 2 nm from the surface when the BTBT model is included

Figure. 7 compares the I_{ON}/I_{OFF} ratio as a function of channel length for S-FED. Fig.7 illustrates that by decreasing the channel length and considering the tunneling phenomenon, the I_{ON}/I_{OFF} ratio decreases.
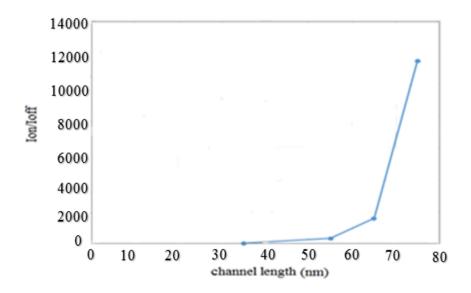
Fig. 7. I_{ON}/I_{OFF} ratio as a function of channel length for the S-FED

5. CONCLUSION

In this paper, the role of the channel length and band-to-band tunneling (BTBT) on the performance of S-FED is investigated. Simulation results in this paper show that the band diagram of the S-FED device for less than 35 nm channel length is similar to the tunneling diode. Hence electron tunneling from the valence band into the conduction band is formed. As a result, additional electron hole pairs are generated and contribute to the OFF-state current. Therefore, BTBT increases the OFF-state current of the S-FED device. The characteristic of the voltage-current and energy levels of this structure was studied for 75 nm, 55 nm and 35 nm channel length. Our studies indicate that by decreases the channel length, the I_{ON}/I_{OFF} ratio can be varied from 10^4 to 10^0 for S-FED. Therefore that for channel lengths shorter than 35 nm by considering the Band-to-Band tunneling model, the S-FED device does not turn off.

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