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Design of a Sample & Hold Circuit Using a Two-Stage Class-AB operational transconductance amplifier

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Abstract

This paper introduces dc-gain enhancement circuit for CLASS AB Operational Trans conductance Amplifier (OTA). In this OTA, active loads and recycling folded cascade technique are employed to increase the DC-gain of the OTA by about 17dB without affecting the unity-gain bandwidth (UGBW), stability, power dissipation and output voltage swing of the conventional two-stage OTA. Using the nonlinear current mirror (NLCM) in the second stage the current of the output stage is increased. Therefore, the slew rate (SR) is improved. The proposed OTA is utilized in a flip-around sample-and-hold amplifier (SHA). The output spectrum of the SHA shows the total harmonic distortion of 0.0023%. The post-layout and Monte Carlo simulation results show that the proposed OTA has better performance than the state-of- the-art designs. The efficiently of the proposed OTA is evaluated by several simulations in 0.18µm, CMOS process whit the 1.8V supply voltage.

1. Introduction

Operational trans- conductance amplifier (OTA) are an essential component in the modern mixed-signal systems [1–3]. High-gain and high-speed OTA can be used in the various applications such as high-resolution analogue-to-digital converters and digital-to-analogue converters, bandgap voltage references and sample-and-hold amplifiers (SHAs) [4–6]. Designing a OTA that combines both high DC gain and high slew rate (SR) has proven to be a difficult task, especially in low-voltage circuits. Bulk-driven methods can also be used for gain enhancement in low-voltage processes [7–14]. The major disadvantage of a bulk- driven MOS device in CMOS technologies is that bulk-source trans-conductance is smaller than the gate-source trans- conductance and may not be enough in some applications [15]. In addition, this method has some problems such as degradation of the phase margin of the amplifier compared with the conventional amplifier due to non-dominant poles

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effect which is caused by the added current mirrors [16]. In [17, 18], a method based on positive feedback has been introduced to increase the DC gain of the op-amp by about 18.5 dB. However, in this technique chip area has been increased drastically. In other methods [19, 20], DC-gain enhancement is obtained with the cost of UGBW decreasing. In [21], a folded cascode op-amp has been proposed which improves DC gain using positive feedback technique. However, this method is sensitive towards process variation. Combined method using the bulk-driven and positive-feedback techniques is proposed in [3]. An OTA with bulk-driven input stage is proposed in which bulk trans-conductance is improved using the positive-feedback. But, some specifications such as input referred noise may not be desirable. To dominate the deficiency of the class-A OTAs, the class-AB OTA can be helpful [12]. Several techniques for class-AB OTAs have been reported in the literatures [7-21]. Class-AB OTAs suggested in [7] have high values for current efficiency (CE) factors. This improvement in CE is obtained by increasing the maximum value of the signalcurrent both in the input and output branches. However, these methods suffer from low open loop gain. A technique to achieve class AB operation is suggested with the cost of increasing the power consumption and silicon area of the circuit [8]. Some class-AB techniques have been applied to the recycling folded cascode (RFC) OTA [9-10]. But, the OTAs need additional local common-mode feedback loops at the active load of the differential pair which should be implement by passive or active matched resistors. In another method [11], adaptive biasing circuit (ABC) for classic fully differential circuits have been introduced using dynamically control the bias current of the amplifier However, circuit area and power dissipation have been increased due to auxiliary blocks. In [12], a class-AB OTA based on single-stage topology with non-linear current amplifiers has been introduced. But, some target specifications such as DC-gain and SR have not been improved significantly. Some low-current OTAs have been suggested in [13-19]. But, technology or temperature sensitivity in the proposed class-AB OTAs are the main drawback of these techniques. In this paper, a new two-stage class-AB OTA is proposed. The trans-conductance enhancement of the first stage is achieved via the simultaneous use of the active loads and the RFC technique. Therefore, the DC-gain of the OTA is increased. Enhancement of the SR is obtained using the nonlinear current mirror (NLCM). The rest of the paper is organized as follows. In Section 2, the proposed OTA is introduced. The performance evaluations of the OTA and comparison results are given in Section 3. Finally, Section 4 concludes the paper.

2. Proposed OTA

The conventional two-stage class-AB OTA is shown in Figure 1 [22]. Figure 2 demonstrates the circuit configuration of the proposed class-AB OTA. In this Figure, v_o and v_{out} indicate the output voltages of the first and second stages, respectively. In Figure 2, a flipped voltage follower (FVF) [23-24] including the transistors $(M_{1a}, M_{1b}, M_{2a}, M_{2b}, M_{3a}, M_{3b})$ are utilized as an ABC. When a large differential input signal is applied to the OTA, the FVF can deliver more current than the quiescent current. Therefore, it operates in class-AB and this characteristic can be useful for low-power applications. The RFC block is also shown in Figure 2. Input signals are applied to the split transistor sets (M_{4a}, M_{4b}) and (M_{4c}, M_{4d}) which have the same aspect ratio. M_{24a}:M_{24b} and M_{25a}:M_{25b} with a ratio of k:1 are used as current mirrors. To improve matching, M_{23a}:M_{23b} are employed to maintain the drain potentials of M_{24a}:M_{24b} and M_{25a}:M_{25b} equal [20]. The Source of (M_{4a}, M_{4b}) is connected to the drain of M_{3b} and to the gate of M_{10}. similarly, Source of (M_{4c}, M_{4d}) is connected to the drain of M_{3a} and to the gate of M_9. Therefore, the class-AB operation can be obtained for the active load transistors M_9 and M_{10} related to the common-gate transistors M_5 and M_6.

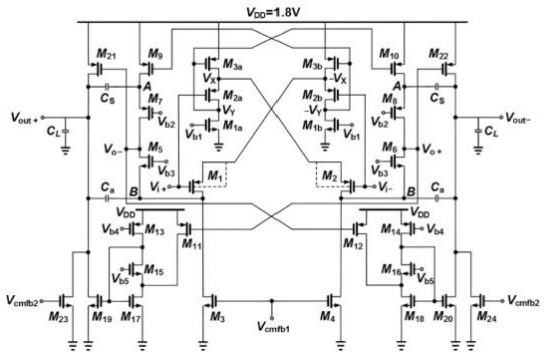


Fig. 1: The conventional two-stage class AB OTA [22].

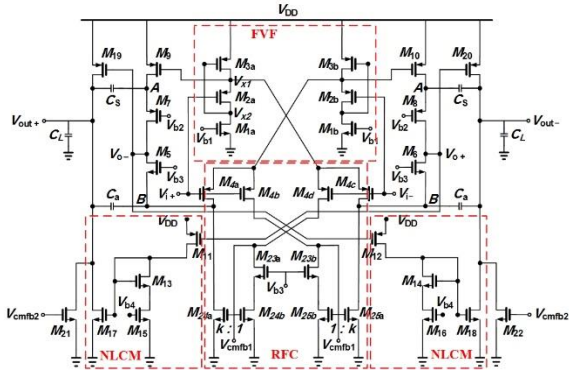


Fig. 2: The proposed class-AB OTA.

In this circuit, the gate of M_9 and M_{10} are connected to the input stage using the FVF. It is illustrated in Figure 3 that gate-source voltage of M_9 is $V_{X1} = V_i / 2$. Therefore, the trans-conductance of the input stage is obtained as follows:

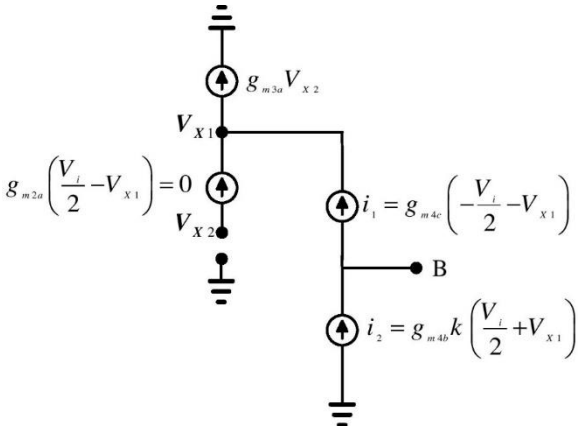


Fig. 3: calculating trans-conductance of the input stage with Small-signal model

The Solar cogeneration system with several desalinat As can be seen from e (1), the input trans-conductance is higher than the methods proposed in [20, 22, 23]. For a better explanation, the input stage trans-conductance of the proposed OTA and existing OTAs are summarized in Table 1.

Table 1:. Comparison of the input stage trans-conductance of the proposed OTA and the existing OTAs .

Method	Input Stage Trans-conductance
[20]	$g_{m4a}(1+k)$
[22]	$g_{m1,2}+g_{m9,10}$
[23]	$g_{m1,2}+g_{m9,10}$
The Proposed OTA	$g_{m4a}(1+k)+g_{m9,10}$

The NLCMs have been used for the output active loads including transistor sets $(M_{11},M_{13},M_{15},M_{17})$ and $(M_{12},M_{14},M_{16},M_{18})$. To active the NLCMs, the gates of M_{11} and M_{12} are connected to the first stage outputs V_{o+} and V_{o-}, respectively. The transistors M_{15} and M_{16} are biased near the triode region so that their drain-source voltages are a bit higher than $V_{DS,sat}$ [12]. In following, it shows that for a large V_{id} the output current increases proportional to v_{id}^4, that would enhance the SR of the OTA.

2-1. DC-gain

The DC-gain of the proposed OTA can be calculated as follows:

$$A_d = A_1 \times A_2 \tag{2}$$

$$A_1 = g_{meff1} R_{out1} \tag{3}$$

where

$$R_{out1} = g_{m7} r_{ds7} r_{ds9} \| \left(g_{m5} r_{ds5} \left(r_{ds4a} \| r_{ds24a} \right) \right) \tag{4}$$

A_2 is the DC-gain of the second stage as follows:

$$A_2 = g_{m19} R_{out2} \tag{5}$$

$$R_{out2} = r_{ds17} \| r_{ds19} \| r_{ds21} \tag{6}$$

In the above equations, R_{out1} and R_{out2} represent the output resistance of the first and second stages, respectively. The drain-source resistor of the relevant transistor is shown by r_{ds} .

2.2. Common-mode gain

Analysis of the common-mode (CM) gain is performed for the proposed OTA. It should be noted that decreasing the RFC output current, $g_{m4a}(\mathrm{k}-1)$ in the common-mode compared to $g_{m4a}(\mathrm{k}+1)$ in the differential-mode, leads to a reduction in the common-mode gain (See Figure 4). The common-mode gain can be calculated as follows:

$$A_{CM}=\frac{(g_{m4a}(\mathrm{k}-1)+g_{m9,10})R_{out1}}{1+2(g_{m4a}(\mathrm{k}-1)+g_{m9,10})r_{ds3a}}\times g_{m19}R_{out2} \tag{7}$$

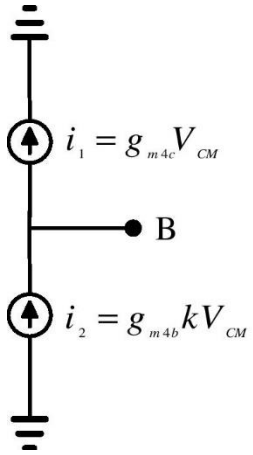


Fig. 4: RFC output current in the common-mode.

2.3. Power supply rejection ratio

Power supply rejection ratio (PSRR) analysis is performed for the proposed OTA to evaluate the effect of power supply voltage variations on the output nodes. The voltage source Vdd(ac) indicates the power supply variations. The PSRR is calculated as below:

$$PSRR=\frac{V_{out}/V_{id}}{V_{out}/V_{dd}(ac)}=\frac{A_d}{V_{out}/V_{dd}(ac)} \tag{8}$$

$$=\frac{-A_d}{\left(g_{m3a}(\mathrm{k}-1)/2+g_{m9}\right)R_{out1}g_{m19}R_{out2}}$$

2.4. Input-referred noise

The input-referred noise of transistors can be calculated as below

$$\overline{V_{ni,\mathrm{M}4c}^2}=\left(\frac{g_{m4c}}{g_{meff1}}\right)^2\times\overline{V_{n,4c}^2} \tag{9}$$

$$\overline{V_{ni,\mathrm{M}25a}^2}=\left(\frac{g_{m25a}}{g_{meff1}}\right)^2\times\overline{V_{n,25a}^2} \tag{10}$$

$$\overline{V_{ni,\mathrm{M}25b}^2}=\left(\frac{g_{m25b}}{g_{meff1}}\right)^2 k^2\times\overline{V_{n,25b}^2} \tag{11}$$

$$\overline{V_{ni,\mathrm{M}9}^2}=\left(\frac{g_{m9}}{g_{meff1}}\right)^2\times\overline{V_{n,9}^2} \tag{12}$$

By substituting $\overline{V_{ni,Mi}^2}=\frac{4kT\gamma}{g_{mi}}$ in the above equations, the OTA total input-referred noise voltage per unit bandwidth is given as follows:

$$\overline{V_{ni,\mathrm{pro}}^2}=\frac{8kT\gamma}{g_{meff1}^2}\left[g_{m4b}(1+k^2)+(g_{m25a}+g_{m25b}\mathrm{k}^2)+g_{m9}\right] \tag{13}$$

Therefore, increasing g_{meff1} can significantly reduce the total input-referred noise voltage of the proposed OTA.

2.5. Input offset

The mismatch between MOS transistors can be defined as a function of device areas, distances, and orientations [25]. It has been demonstrated that the difference of an electrical parameter P between two rectangular devices is modeled by the following equation

$$\sigma^2(\Delta P)=\frac{A_P^2}{WL}+S_P^2D_x^2 \tag{14}$$

where Ap is the area proportionality constant for P, W and L represent the width and length of the transistor, and SP is the variation of P under the device spacing Dx. The input offset variance of the proposed OTA is ca

$$\sigma^2(V_{OS})=\frac{2}{g_{meff1}^2}\left[\frac{g_{m4b}^2(1+k^2)A_{VTP}^2}{W_{4b}L_{4b}}+\frac{g_{m25a}^2A_{VTN}^2}{W_{25a}L_{25a}}+\frac{g_{m25b}^2k^2A_{VTN}^2}{W_{25b}L_{25b}}+\frac{g_{m9}^2A_{VTP}^2}{W_9L_9}\right] \tag{15}$$

In the above equations, A_{VTP} and A_{VTN} are the area proportionality constant for threshold voltage of PMOS and NMOS, respectively.

2.6. Output current of NLCM

Here, an equation for the drain current of M_{18} in terms of V_{id} is presented. It should be noted that the transistors M_{16} and M_{18} should be biased in the vicinity of the triode and saturation region, respectively. As a result, the current through M_{18} is given by

$$I_{18}=\frac{\beta_{18}}{2}\left(\frac{\sqrt{2I_{12}}}{\beta_{14}}+\frac{2I_{12}}{\lambda_{16}\beta_{16}\left(V_{b4}-V_{th}\right)^2}-\frac{1}{\lambda_{16}}\right)^2 \quad (17)$$

where $\beta_{18}=\mu_n C_{ox}(\mathrm{W/L})_{18}$, λ is the modulation parameter and V_{th} represents the threshold voltage. The current through M_{12} is given by

$$I_{12}=\frac{\beta_{12}}{2}(V_{GS12}-V_{th})^2=\frac{\beta_{12}}{2}(V_{DD}-V_{o-}-V_{th})^2 \quad (18)$$

The voltage V_{o-} of this node can be obtained as below

$$V_{o-}=g_{meff1}\frac{V_{id}}{2}R_{out1}+V_{CMO1} \quad (19)$$

where V_{CMO1} is the first stage common-mode output voltage. Substituting (18) in (19), the drain current of M_{12} is obtained

$$I_{12}=\frac{\beta_{12}}{2}(V_{DD}-g_{meff}\frac{V_{id}}{2}R_{out1}-V_{CMO1}-V_{th})^2 \quad (20)$$

Finally, using (19), (20) the current through M_{20} is calculated:

$$I_{18}=\frac{\beta_{18}}{2}\left(\frac{\sqrt{2(\frac{\beta_{12}}{2}(V_{DD}-g_{meff}\frac{V_{id}}{2}R_{out1}-V_{CMO1}-V_{th})^2)}}{\frac{\beta_{14}}{2(\frac{\beta_{12}}{2}(V_{DD}-g_{meff}\frac{V_{id}}{2}R_{out1}-V_{CMO1}-V_{th})^2)}}+\frac{2(\frac{\beta_{12}}{2}(V_{DD}-g_{meff}\frac{V_{id}}{2}R_{out1}-V_{CMO1}-V_{th})^2)}{\lambda_{16}\beta_{16}\left(V_{b4}-V_{th}\right)^2}-\frac{1}{\lambda_{16}}\right)^2 \quad (21)$$

From (21), it is obvious that for a large V_{id} the output current increases proportional to V_{id}^4 .

$$FOM_S=\frac{UGBW.C_L}{I_T} \quad (22)$$

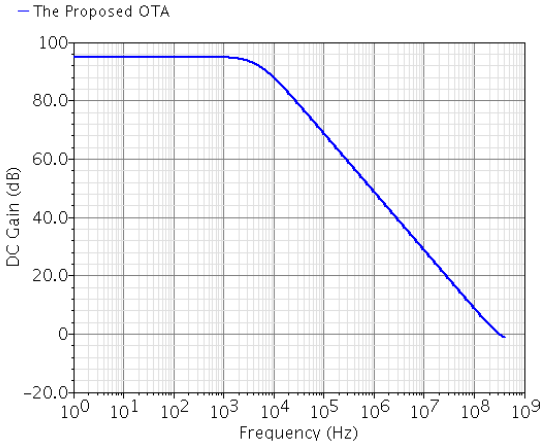
$$FOM_L=\frac{\mathrm{SR}.C_L}{I_T} \quad (23)$$

3. Simulation Results

To verify the performance of the proposed two-stage class-AB OTA several simulations are performed in a 0.18 μm CMOS process with 1.8V supply voltage using Cadence software. The specifications of the elements and bias voltages of the proposed OTA are reported in Table 2. The frequency responses of the proposed OTA are shown in Figure 5. According to the simulation results, The DC-gain of the OTA is 95 dB. UGBW and phase margin of the proposed OTA is 340 MHz and 64^o , respectively. For the slew rate calculation, a square wave, 1 Vpp at 5 MHz was applied to the OTA and the result is given in Figure 6. The common-mode rejection ratio (CMRR) and PSRR of the proposed OTA are shown in Figure 7. Table 3 shows the OTA specifications in the three processes and temperature corners. As seen from the results, the OTA presents high DC-gain. Also, the proposed OTA is stable in the three processes and temperature corners. Furthermore, the proposed OTA- is employed in an 80 MS/s flip-around SHA (Fig. 8a).The SHA samples from a sinusoidal input signal with the input frequency of 2 MHz and amplitude of Ain,diff = 0.4 Vpp. The fast Fourier transform (FFT) of the SHA output is shown in Fig. 8b using 256 points. Accordingly, the calculated total harmonic distortion (THD) is about 0.0023%. Monte Carlo (MC) simulations are done by considering both process and mismatch variations. Figure 9 demonstrates the MC histograms of the proposed OTA using 1000-run simulations. The vertical axis represents the histogram count. The horizontal axis in Figures a to d represents the DC-gain, input offset, phase margin and UGBW, respectively. The results are also summarized in Table 4. As can be seen from the results, under the process and mismatch variations the OTA specifications are not degraded significantly. The physical layout of the proposed OTA is shown in Figure 10. The layout area is 131µm×142µm .The proposed OTA simulation results are compared with the existing methods in Table 5. The results indicate that the proposed OTA has the highest DC-gain compared to the other techniques. It has the lowest input-referred noise due to the improved input stage trans-conductance. To compare the other performance parameters, the traditional couple of figures of merits in (22), (23) which for a given load indicate a trade-off between speed performance and total bias current (I_T) are utilized [26-27]. As can be seen from Table 5, the proposed OTA has proper values for both of FOMs and FOM_L

Tables 3: Specifications of the proposed OTA.

Parameter	Value	Parameter	Value
$(W/L)_{1a,1b}$	1×10µm/0.18µm	$(W/L)_{23a,23b}$	1×15µm/0.18µm
$(W/L)_{2a,2b}$	1×25µm/0.18µm	$(W/L)_{24a,25a}$	1×45µm/0.18µm
$(W/L)_{3a,3b}$	2×25µm/0.18µm	$(W/L)_{24b,25b}$	1×15µm/0.18µm
$(W/L)_{4a,4b,4c,4d}$	1×12.5µm/0.18µm	C_a, C_s	2.1 pF
$(W/L)_{5,6}$	1×15µm/0.18µm	C_L	10 pF
$(W/L)_{7,8}$	1×30µm/0.18µm	V_{b1}	0.63V
$(W/L)_{9,10}$	1×30µm/0.18µm	V_{b2}	0.77V
$(W/L)_{11,12}$	2×15µm/0.36µm	V_{b3}	1.15V
$(W/L)_{13,14,15,16,17,18}$	2×10µm/0.36µm	V_{b4}	0.77V
$(W/L)_{19,20}$	2×40µm/0.36µm	V_{CMO1}	1.15V
$(W/L)_{21,22}$	2×10µm/0.36µm	V_{CMO2}	0.9V



(a)

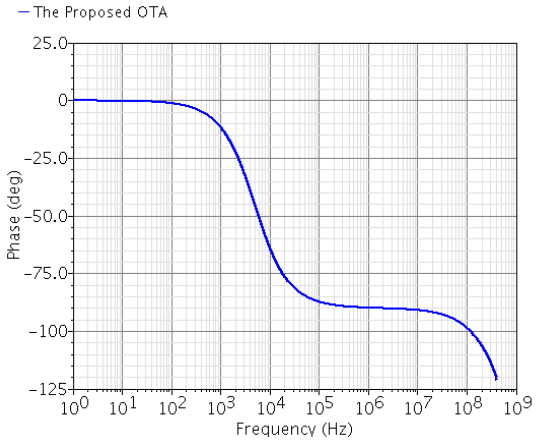


Fig 5. Frequency responses for both OTAs: (a) magnitude and (b) phase

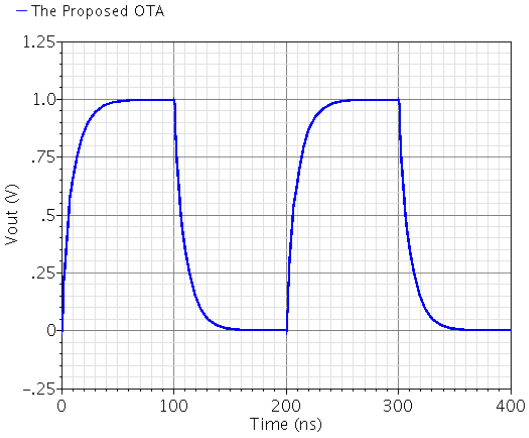


Fig. 6 Large signal step responses of the OTA

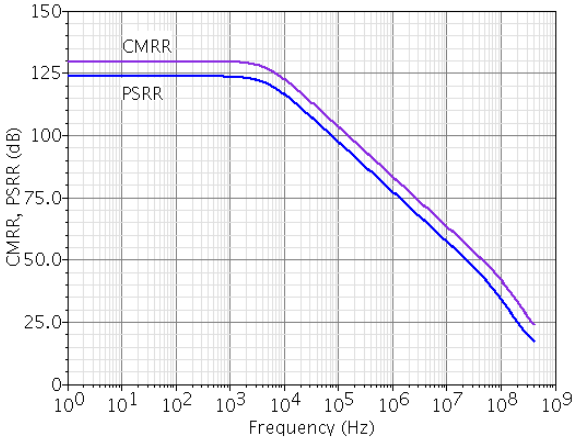
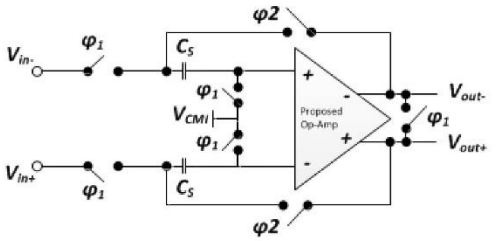


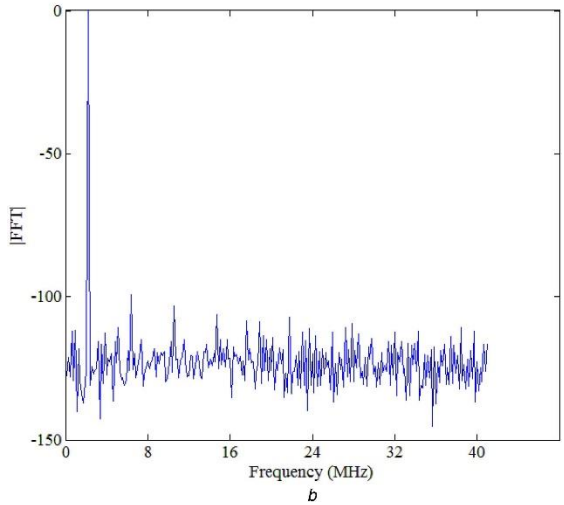
Fig. 7 CMRR and PSRR of the OTA.

Table 3. Specifications of the proposed OTA

Specification	Proposed OTA		
	TT(27° C)	FF(-40° C)	SS(90° C)
Technology	0.18µm	0.18µm	0.18µm
DC-Gain (dB)	95	88	96
Input-Referred Noise@100kHz $(\mu V/\sqrt{Hz})$	0.21	0.19	0.30
Differential output Swing (peak to peak) (V)	2.8	2.8	2.8
Phase Margin ($^{\circ}$)	64	63	67
Power Dissipation (mW)	3	4.1	2.3
Slew Rate $(V/\mu s)$	172	252	102
UGBW (MHz)	340	450	230
C_L (pF)	10	10	10

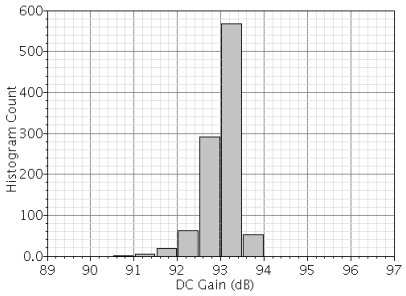


a

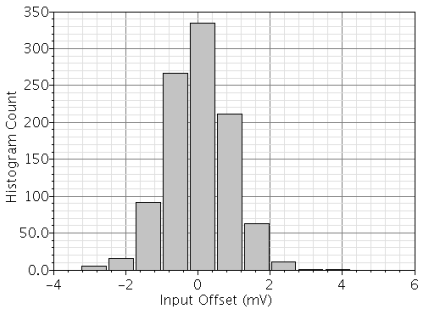


b

Fig. 8 Flip-around and FFT of the SHA output (a) Flip-around sample-and-hold, (b) FFT plot of the output of the sample-and-hold



(a)



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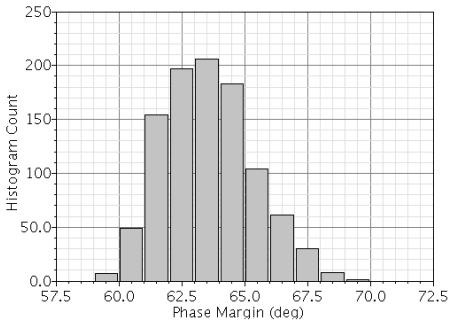
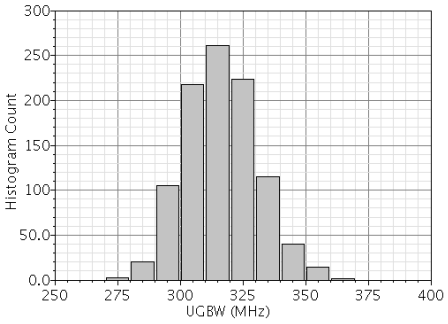


(c)



(d)

Fig. 9. Histogram of MC Simulation. (a) Dc Gain, (b) Input Offset, (c) Phase Margin, (d) UGBW

Table 4. The MC Analysis of the Proposed OTA.

Specification	Mean Value	Standard Deviation
DC Gain (dB)	93.5	3.9
Input Offset (mV)	0.02	0.8
Phase Margin ($^\circ$)	63.6	1.8
UGBW (MHz)	326.5	10.2

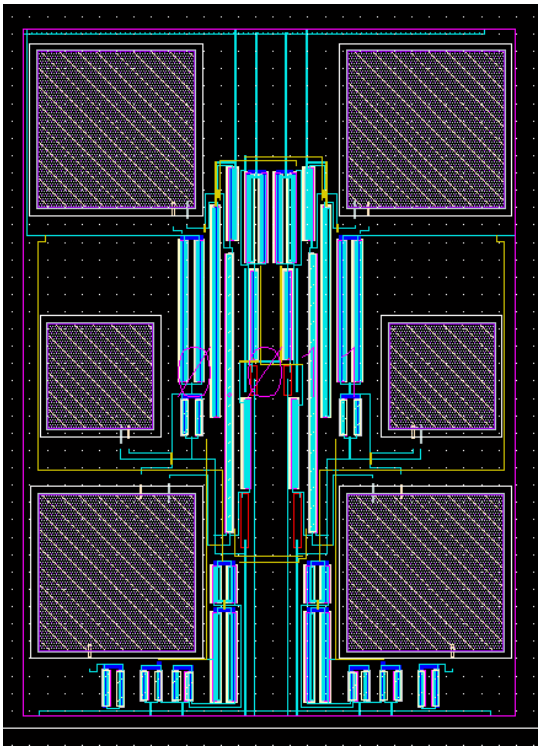


Fig 10. Physical layout of the proposed OTA

	This[b] work	[12]	[14]	[17]	[23][b]
Technology	0.18µm	0.5µm	0.5µm	0.18µm	0.18µm
Supply Voltage (V)	1.8	1	1	1.8	1.8
DC-Gain (dB)	93.5	30	76.8	72	93
Input-Referred Noise@100 kHz $(\mu v/\sqrt{Hz})$	0.23	144	0.023	144	0.31
Differential Output Swing (peak to peak) (V)	2.8	--	--	--	2.8
Phase Margin ($^\circ$)	64	90	75.1	50	65
Power Dissipation (mW)	3	0.08	0.1	11.9	3
Slew Rate $(V/\mu s)$	169	0.35	25.3	74.1	494
UGBW (MHz)	334	0.2	3.4	86.5	216
Loading Capacitance (pF)	10	80	70	200	1
Operating Mode[a]	SI	SI	SI	SI	SI
$FOM_S = \frac{MHz.pF}{mA}$	2000	200	1190	2613	135
$FOM_L = \frac{V.pF}{\mu s.mA}$	1012	350	8855	2239	309

4. Conclusion

In this paper, a new two-stage class-AB OTA in a 0.18 µm CMOS process with a 1.8 V supply voltage has been presented. The proposed OTA was based on the simultaneous application of class-AB operation in both of the stages. Using active loads and also RFC structure, the first stage trans-conductance has been increased. The NLCM in the output stage has been employed to enhance the SR of the OTA. To evaluate the effectiveness of the proposed method, several simulations have been performed. The results indicated the better performance of the proposed OTA in terms of DC-gain, UGBW, and SR compared to the

existing methods. The OTA has been employed in an 80 MS/s SHA. The results showed that the THD was about 0.0023%.

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Data availability

The specifications of the elements and bias voltages of the proposed OTA are reported in Table.

Parameter	Value	Parameter	Value
$(W/L)_{1a,1b}$	1×10μm/0.18μm	$(W/L)_{23a,23b}$	1×15μm/0.18μm
$(W/L)_{2a,2b}$	1×25μm/0.18μm	$(W/L)_{24a,25a}$	1×45μm/0.18μm
$(W/L)_{3a,3b}$	2×25μm/0.18μm	$(W/L)_{24b,25b}$	1×15μm/0.18μm
$(W/L)_{4a,4b,4c,4d}$	1×12.5μm/0.18μm	C_a, C_s	2.1 pF
$(W/L)_{5,6}$	1×15μm/0.18μm	C_L	10 pF
$(W/L)_{7,8}$	1×30μm/0.18μm	V_{b1}	$0.63V$
$(W/L)_{9,10}$	1×30μm/0.18μm	V_{b2}	$0.77V$
$(W/L)_{11,12}$	2×15μm/0.36μm	V_{b3}	$1.15V$
$(W/L)_{13,14,15,16,17,18}$	2×10μm/0.36μm	V_{b4}	$0.77V$
$(W/L)_{19,20}$	2×40μm/0.36μm	V_{CMO1}	$1.15V$
$(W/L)_{21,22}$	2×10μm/0.36μm	V_{CMO2}	$0.9V$