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Research Article

Design and Implementation of a 16-bit Multi-Mode Delta-Sigma Digital-to-Analog Converter with Time-Interleaved Structure, Multi-Channel, and Compensation of Non-Idealities Based on FPGA

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Abstract

In this research, a 16-bit multi-mode second-order Delta-Sigma Modulator-Digital-to-Analog Converter (DSM-DAC) with a time-interleaved (TI) structure operating at a center frequency of 4 GHz and a bandwidth of 20 MHz has been implemented using VHDL on an FPGA platform. The proposed architecture utilizes a single clock frequency for generating RF signals. The second-order DSM is reconfigurable, offering three filter modes: LP, BP at Fs/4, and HP for signal synthesis. Since the coefficients remain simple for all modes, multiplication operations can be achieved using a shifter block. To investigate the effect of duty-cycle-error (DCE) and its compensation, various error values are applied to the modulator and compensation is performed. A novel solution is proposed to overcome the DCE by adjusting the filter and unilaterally narrowing the signal passband without adding extra hardware complexity. This approach significantly enhances the SNDR and SFDR of the DSM output, even for the BP mode. Another challenge is the mismatch error in DAC cells. This error is simulated and compensated using two methods: DWA and SDEM. Simulation results in ISE demonstrate that the SNDR values for LP, BP, and HP modes are 106.10, 105.65, and 104.95 dB, respectively.

Keywords: Delta-sigma modulator, Duty-cycle-error, Error-feedback, FPGA, Mismatch, Time-interleaved.

Highlights

- A 16-bit multi-mode digital-to-analog converter with a time-interleaved structure at a frequency of 4 GHz.
- Only one clock frequency is used to generate the radio frequency signal.
- There are simple coefficients for all cases, the multiplication operation can be performed using a shifter block.
- Two dominant errors in TI-DSM-DACs (mismatch and duty-cycle-error (DCE)) have been compensated
- A new method is proposed to remove the effect of signal image in BP mode, instead of using complex circuits.

Citation: [in Persian].