A new topology for quasi-Z-source inverter

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Abstract

In this paper, a new circuit is proposed for step-up Z-source inverter based on QZSI (quasi-Z-source inverter). The proposed topology inherits all advantages of the conventional topology. The proposed topology in comparison with conventional topology reduces the ST (Shoot-through) duty cycle by over 25% at the same voltage boost factor. Theoretical analysis of the proposed qZSI in the ST and non-ST operating modes is described. Then in order to show the performance of the proposed ZSI, the simulation results on PSCAD software are used.

Keywords: Z-source inverter; quasi-Z-source inverter; Shoot-through

1. Introduction

The Z-source converter employs a unique impedance network to couple the converter main circuit to the power source. The Z-source converter overcomes the limitations of the conventional voltage source and current source converters and provides a new power conversion concept. In [1], the step-up dc/dc converter family with a cascaded qZS-network has been presented. Presented circuit in [1], could be derived by adding of one diode, one inductor, and two capacitors to the conventional qZSI and inherits all advantages of the conventional topology such as boost and buck conversion in a single stage, continuous input current, and improved reliability. Moreover, as compared to the conventional qZSI, reduces the ST duty cycle by over 30% at the same voltage boost factor. Due to the decreased ST duty cycle, the values of inductors and capacitors of the presented qZSI in [1] could also be decreased. On the other hand, for the same component ratings and voltage and current stresses, this circuit will ensure a higher voltage boost factor than with conventional topologies. The presented qZSI in [1] can be applied to almost all dc/ac, ac/dc, ac/ac and dc/dc power conversion schemes. To further decrease the ST duty cycle at the same voltage boost factor, the number of stages of the qZS-network could be increased.

In [2], the main circuit of the Z-source inverter or three-phase Z-type inverter has been presented. This inverter has two different operating modes including ST state and non-ST state. In [2], the main circuit of the Z-source inverter and the operation principle have been described in detail. Simple boost control method is used for controlling qZSI [3].

To improve the performance of the conventional ZSIs, in [4] several topologies have been developed. These inverters are similar to the Z-source inverters presented in previous works, but have several advantages, including in some combination, lower component count and simplified control strategies. The qZSI topologies, like the ZSIs, are well suited for systems which require a large range of gain, or a large gain, such as motor controllers and renewable energy applications.

1. Proposed topology

In this paper a new topology for step-up Z-source inverter is proposed based on qZI. This cascaded structure inherits all advantages of the conventional topology. The proposed topology in

comparison with conventional topology reduces the ST (Shoot-through) duty cycle by over 25% at the same voltage boost factor. According to the Fig. 1, the proposed circuit is derived by the adding of one diode, one inductor and two capacitors to the presented qZSI in [1]. The inverter at the output of ZSI can be single-phase or three-phase. In Fig. 1, the single-phase inverter is used. The proposed topology in comparison with the presented circuit in [1], reduces the ST duty cycle by over 25% at the same voltage boost factor. Due to the decreased ST duty cycle, the values of inductors and capacitors of the proposed topology could also be decreased. On the other hand, for the same component ratings and voltage and current stresses, the proposed topology can generate a higher voltage boost factor than the conventional topologies.

In order to analyze the proposed structure in ST and non-ST modes it is supposed that all of the circuit elements such as diodes, capacitors and inductors are ideal.

One of the SPWM control methods for Z-source inverters, is simple boost control method. Fig. 2 shows the modulation, the driver signals for the four switches, and the ST signals of simple boost control method. If we use two right lines V_p and V_n in conventional SPWM control method, simple boost control method is obtained. In this method, two straight lines (V_p and V_n) are employed to realize the ST duty ratio (D_{ST}) [3]. The first one (V_p) is equal to the peak value of the sinusoidal reference voltages while the other one (V_n) is the negative of the first one. Whenever the triangular carrier signal is higher than the positive straight line or lower than the negative straight line, the inverter will operate in ST. Otherwise it works as a conventional PWM inverter [11].

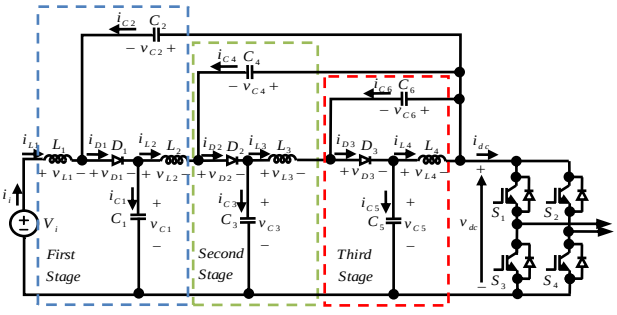
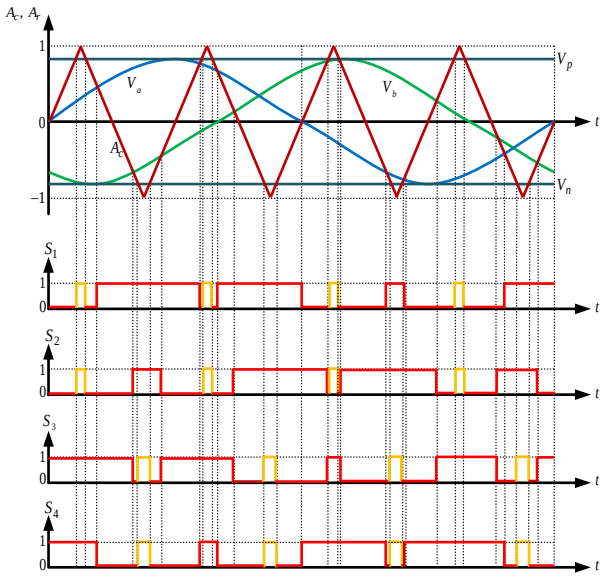


Fig. 1. Proposed quasi Z-source inverter figure



Generation of PSM signals with shoot-through states during zero states

2. Circuit analysis of the proposed qZSI

The equivalent circuits of proposed topology during non-ST and ST modes are shown in Fig. 3. With this explanation that, in non-ST state the inverter bridge seen by dc side is equal to a current source and diodes conducts and the voltage V_{dc} increases stepwise from zero to its maximum ($V_{dc,\max}$). But in the ST state, the inverter bridge seen by dc side is equal to short circuit and diodes do not conduct and the inverter bridge input voltage ($V_{dc}=0$) and energy stored in capacitors is transferred to the inductors.

By applying KVL to circuit for Fig. 3(a) we have:

$$v_{L1}=V_i-V_{C1} \quad (1)$$

$$v_{L2}=V_{C1}-V_{C3}=V_{C4}-V_{C2} \quad (2)$$

$$v_{L3}=V_{C3}-V_{C5}=V_{C6}-V_{C4} \quad (3)$$

$$v_{L4}=V_{C5}-v_{dc}=-V_{C6} \quad (4)$$

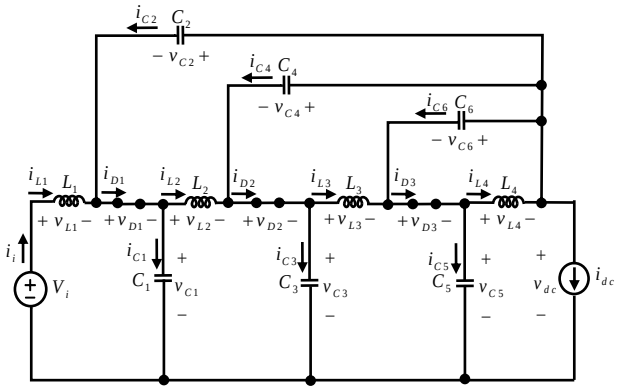
By applying KVL to circuit for Fig. 3(b) we have:

$$v_{L1}=V_i+V_{C2} \quad (5)$$

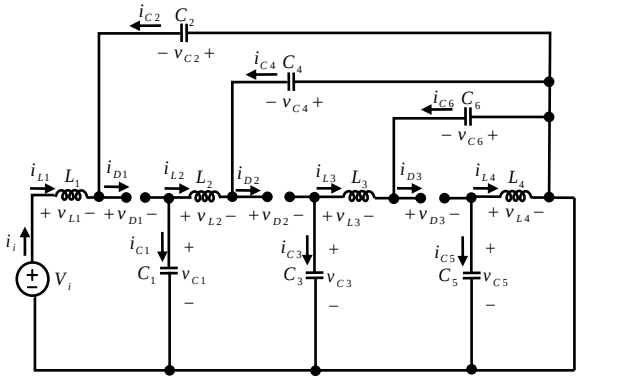
$$v_{L2}=V_{C1}+V_{C4} \quad (6)$$

$$v_{L3}=V_{C3}+V_{C6} \quad (7)$$

$$v_{L4}=V_{C5} \quad (8)$$



(a)



(b)

Fig. 2. Equivalent schemes of the proposed qZSI **(a)** non-ST state **(b)** ST state

In steady state, the average value of voltage across inductors equal to zero. In other words:

$$\int_0^{T_s} v_{L1}\,dt = D_{ST}(V_i + V_{C2}) + (1-D_{ST})(V_i - V_{C1}) = 0 \quad (9)$$

$$\int_0^{T_s} v_{L2}\,dt = D_{ST}(V_{C1} + V_{C4}) + (1-D_{ST})(V_{C4} - V_{C2}) = 0 \quad (10)$$

$$\int_0^{T_s} v_{L3}\,dt = D_{ST}(V_{C3} + V_{C6}) + (1-D_{ST})(V_{C6} - V_{C4}) = 0 \quad (11)$$

$$\int_0^{T_s} v_{L4}\,dt = D_{ST}(V_{C5}) + (1-D_{ST})(-V_{C6}) = 0 \quad (12)$$

Simplifying (9) and (12) and considering (1) to (4), we obtain as below:

$$V_{C1} = \frac{1-3D_{ST}}{1-4D_{ST}} V_i \quad (13)$$

$$V_{C2} = \frac{3D_{ST}}{1-4D_{ST}} V_i \quad (14)$$

$$V_{C3} = \frac{1-2D_{ST}}{1-4D_{ST}} V_i \quad (15)$$

$$V_{C4} = \frac{2D_{ST}}{1-4D_{ST}} V_i \quad (16)$$

$$V_{C5} = \frac{1-D_{ST}}{1-4D_{ST}} V_i \quad (17)$$

$$V_{C6} = \frac{D_{ST}}{1-4D_{ST}} V_i \quad (18)$$

Considering (4), (17) and (18), the maximum amount of dc-link voltage ($v_{dc,\max}$) is obtained as below:

$$v_{dc,\max} = \frac{1}{1-4D_{ST}} V_i \quad (19)$$

Voltage across the inductors at ST and non-ST states can be obtained considering the equations of voltage across the capacitors. It is approved that voltage across the inductors at non-ST and ST states are the same. Thus we have:

$$v_{L1} = v_{L2} = v_{L3} = v_{L4} = v_L = L\frac{\Delta i}{\Delta T_s} \quad (20)$$

Considering (5) to (8), we have:

$$v_L = V_{C5} = \frac{1-D_{ST}}{1-4D_{ST}} V_i \quad (21)$$

Supposing current ripple and constituting of Δi and ΔT_s (ST period) from (22) and (23) in above equation, the amount of v_L is obtained as (24).

$$\Delta i = 0.2 I_L \quad (22)$$

$$\Delta T_s = T_s D_{ST} \quad (23)$$

$$v_L = L\frac{0.2 I_L}{T_s D_{ST}} = V_{C5} \quad (24)$$

Finally constituting of I_L from (25) in above, the amount of inductances of proposed qZSI is calculated as (26):

$$I_L = \frac{P}{V_i} \quad (25)$$

$$L = \frac{D_{ST} V_i^{\,2}}{0.2 P f_s}\left(\frac{1-D_{ST}}{1-4D_{ST}}\right) \quad (26)$$

P is the rated power and f_s is the frequency of qZSI.

By applying KCL for Fig. 2(a), the following equation can be obtained:

$$i_{C1} = I_{L1} + i_{C2} - I_{L2} \quad (27)$$

$$I_{L1} = i_{C1} + i_{C3} + i_{C5} + i_{dc} \quad (28)$$

$$i_{C3} = I_{L2} + i_{C4} - I_{L3} \quad (29)$$

$$I_{L3} = i_{C2} + i_{C4} + i_{C5} + i_{dc} \quad (30)$$

$$i_{C5} = I_{L3} - I_{L4} + i_{C6} \quad (31)$$

By applying KCL for Fig. 2(b), we have:

$$i_{C1} = -I_{L2} = -I_{L4} \quad (32)$$

$$i_{C2} = -I_{L1} \quad (33)$$

$$i_{C3} = -I_{L3} = -i_{C6} \quad (34)$$

$$i_{C4} = -I_{L2} = -i_{C5} \quad (35)$$

In the steady state, the average value of current through capacitors is zero. Neglecting the ripple of flowing current in inductor, we have:

$$\int_0^{T_s} i_{C1}\,dt = D_{ST}(-I_L) + (1-D_{ST})(I_L - I_L + i_{C2}) = 0 \quad (36)$$

$$\int_0^{T_s} i_{C2}\,dt = D_{ST}(-I_L) + (1-D_{ST})(I_L - I_L + i_{C1}) = 0 \quad (37)$$

$$\int_0^{T_s} i_{C3}\,dt = D_{ST}(-I_L) + (1-D_{ST})(I_L - I_L + i_{C4}) = 0 \quad (38)$$

$$\int_0^{T_s} i_{C4}\,dt = D_{ST}(-I_L) + (1-D_{ST})(I_L - I_L + i_{C3}) = 0 \quad (39)$$

$$\int_0^{T_s} i_{C5}\,dt = D_{ST}(I_L) + (1-D_{ST})(I_L - I_L + i_{C6}) = 0 \quad (40)$$

$$\int_0^{T_s} i_{C6}\,dt = D_{ST}(I_L) + (1-D_{ST})(I_L - I_L + i_{C5}) = 0 \quad (41)$$

Considering (32)-(41), for ST state the following equation for capacitors current is obtained:

$$i_{C1} = i_{C2} = i_{C3} = i_{C4} = i_{C5} = i_{C6} = i_C \quad (42)$$

According to (27) to (31), for non-ST state the following equations are obtained:

$$i_{C1} = i_{C2} \quad (43)$$

$$i_{C3} = i_{C4} \quad (44)$$

$$i_{C5} = i_{C6} \quad (45)$$

In order to obtain the values of capacitance C_1, C_2, C_3, C_4, C_5 and C_6 according to (46) and substituting ΔT_s from equation (23), we have:

$$i_C = C\frac{\Delta V_C}{\Delta T_s} \quad (46)$$

$$i_C = \frac{2P}{0.03V_i} = C\frac{v_{dc,\max}}{T_s D_{ST}} \quad (47)$$

Finally according to (42), for ST state and substituting $v_{dc,\max}$ from (19) the following result is obtained:

$$C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C = \frac{2PD_{ST}}{0.03V_i v_{dc,\max} f_s} = \frac{P}{0.015V_i^2 f_s} D_{ST}(1-4D_{ST}) \quad (48)$$

According to (19), the voltage gain is declared as below:

$$B = \frac{v_{dc,\max}}{V_i} = \frac{1}{1-4D_{ST}} \quad (49)$$

Considering the above equation, we can show the duty cycle of ST state is:

$$D_{ST} = \frac{B-1}{4B} \quad (50)$$

The duty cycle for presented topology in [1] is given by:

$$D_{ST} = \frac{B-1}{3B} \quad (51)$$

For same voltage gain for presented topology in [1] and proposed topology, we have:

$$\frac{\frac{B-1}{4B}}{\frac{B-1}{3B}} = \frac{3}{4} \quad (52)$$

Considering the above equation, it is seen that duty cycle of ST state for proposed qZSI is about 0.25 less than the duty cycle of ST state for presented qZSI in [1].

In order to calculate the values of inductors of proposed structure, note that the values of inductances in presented qZSI in [1] is obtained as below:

$$L = \frac{D_{ST}V_i^2}{0.2Pf_s}\left(\frac{1-D_{ST}}{1-3D_{ST}}\right) \quad (53)$$

Considering (26) related to inductors of proposed structure is divided to (53) related to inductors of presented qZSI in [1]. Then substitute of values related to proposed structure duty cycle and values of duty cycle related to presented qZSI in [1], we obtain:

$$\frac{\frac{D_{ST}V_i^2}{0.2Pf_s}\left(\frac{1-D_{ST}}{1-4D_{ST}}\right)}{\frac{D_{ST}V_i^2}{0.2Pf_s}\left(\frac{1-D_{ST}}{1-3D_{ST}}\right)} = 0.784 \quad (54)$$

Note that in above equation, input voltage, rated power and operating frequency is considered the same for each two structures. It is obviously known that in proposed qZSI the value of inductors will be 21.6% less than presented qZSI in [1].

In order to calculate the values of capacitors in proposed structure, note that the values of capacitances in presented qZSI in [1] is obtained as below:

$$C = \frac{P}{0.015V_i^2 f_s} D_{ST}(1-3D_{ST}) \quad (55)$$

Considering (48) related to capacitors of proposed structure is divided to (55) related to

capacitors of presented qZSI in [1]. Then substitute of values related to proposed structure duty cycle and values of duty cycle related to presented qZSI in [1], we obtain:

$$\frac{\frac{P}{0.015V_i{}^2 f_s}D_{ST}(1-4D_{ST})}{\frac{P}{0.015V_i{}^2 f_s}D_{ST}(1-3D_{ST})}=0.75 \quad (56)$$

Note that in above equation, input voltage, rated power and operating frequency is considered the same for each two structures. It is obviously known that in proposed qZSI the value of capacitors will be 25% less than presented qZSI in [1].

The waveforms of voltage and current for proposed qZSI is shown in Fig. 4 for $D_{ST}=0.125$.

It is to be noted that in Fig. 4, A_c is the carrier wave, A_r is the reference sinusoidal wave, positive straight line (V_p) is equal to maximum of reference sinusoidal wave and negative straight line (V_n) is equal to minimum of reference sinusoidal wave. Also T_{ST} and T_{non-ST} are switching period of ST state and non-ST state at a complete switching cycle respectively.In Fig. 5, ST state duty cycle is shown as a function of the voltage boost factor for presented one stage and two stage qZSI also for proposed qZSI.

The ST duty cycle of the proposed qZSI and positive input voltage should never exceed one-fourth of the switching period, while in the conventional topologies, it is, in theory, possible to use the ST duty cycle values up to one-half (for single-stage) and one-third (for two-stage). Practically, it is not advisable to operate at high ST duty cycle values because it will cause high power losses in the components, which could seriously reduce the converters efficiency.

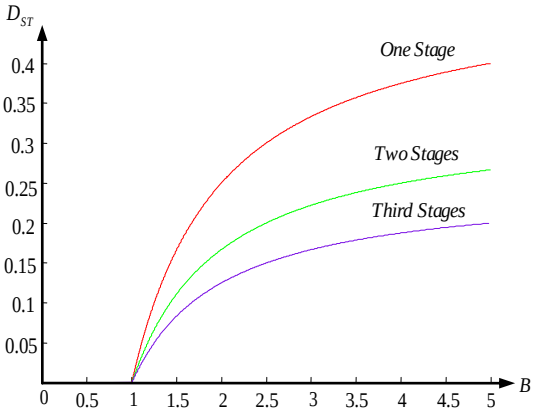


Fig. 3. Shoot-through duty cycle as a function of the voltage boost factor for different types of qZS-networks

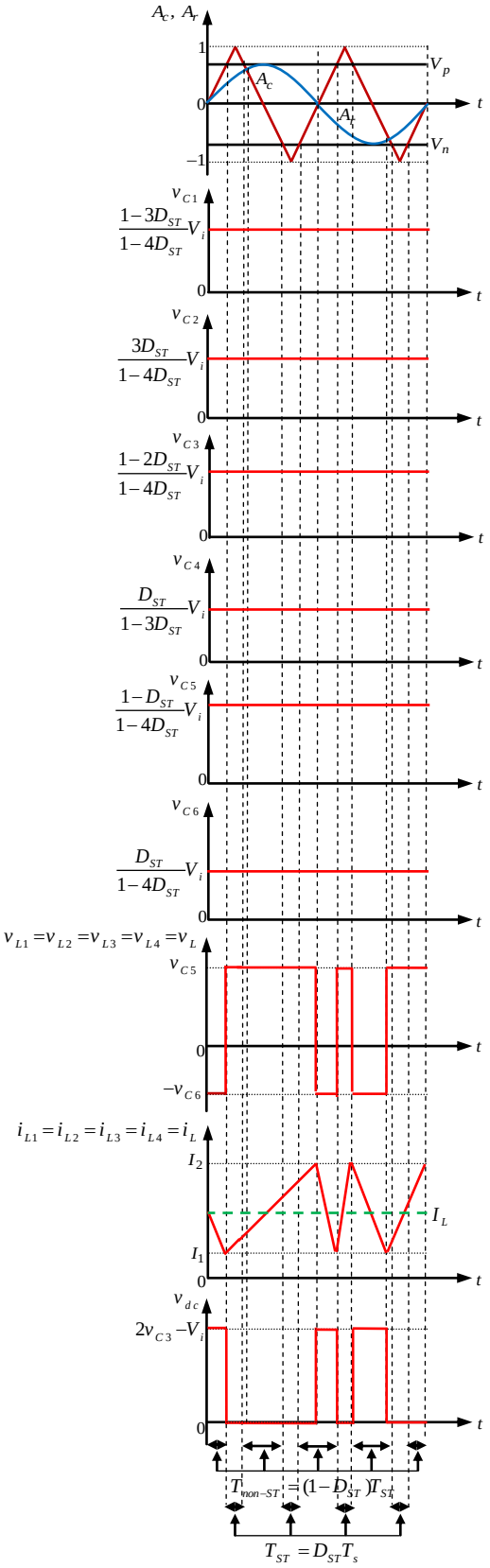


Fig. 4. Voltage and current waveforms of proposed qZSI for $D_{ST}=0.125$

3. Experimental verification

In contrast to the presented solution in [1], the proposed qZSI, provides a reduction of 25% in the ST duty cycle at the same input voltage boost factor. Despite the increase number of passive components and their summarized values, rated values of the inductors and capacitors of the proposed qZSI could also be reduced in comparison with the presented qZSI in [1]. For example, despite the 25% capacitance reduction, the summarized capacitance value ($C_1+C_2+C_3+C_4+C_5+C_6$) required for the proposed qZSI is 12.5% higher than that of the presented qZSI in [1]. The summarized value of the required inductance ($L_1+L_2+L_3+L_4$) will also be 4.53% higher. From here, the feasibility of the proposed qZSI emerges.

Considering losses in the components of the qZS-network (voltage drops in diodes, transistors and inductors), $88V$ was set as the desired dc-link voltage, which means that the twofold boost of the input voltage was required. Moreover, it was stated during the experiments that the proposed qZSI ensures continuous input current in the ST operating mode.

According to equations obtained for voltage across the inductors and capacitors, theoretical results are discussed also proposed values for inductance and capacitance are calculated to compare with results of simulation. Then in order to show the performance of proposed qZSI, the results of simulation are presented by PSCAD software.

Assuming $V_i = 44V$ and $D_{ST} = 0.125$ in (13) to (19) we obtain the values of voltage across the C_1, C_2, C_3, C_4, C_5, C_6 and maximum dc-link voltage ($v_{dc,\max}$) as shown in table 2. Also the values of voltage across the inductors at non-ST state are obtained using (1) to (4) via substituting the calculated values of voltage of capacitors at a defined V_i. Then similarly the value of voltage across the inductors at ST state are obtained as shown in table 2 using V_i and voltage of capacitors in (5) to (8). In order to calculate the values of inductors in proposed structure, according to (54) and defining $37.5\mu H$ for value of inductors in two stage inverter, we obtain $29.4\mu H$ as the value of inductors for proposed qZSI. Similarly according to (56) and defining $240\mu F$ for value of capacitors of presented qZSI in [1], we obtain $180\mu F$ as the value of capacitors of proposed qZSI. The values of output load, frequency of reference wave and frequency of switching used in software are as shown in table 1.

4. Conclusion

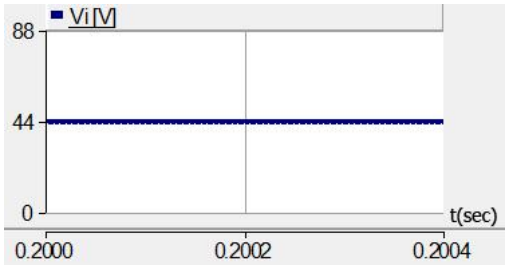
The proposed configuration inherits all advantages of the presented qZSI in [1]. Moreover, the proposed qZSI reduced the ST duty cycle by over 25% at the same voltage boost factor and component stresses as the presented qZSI in [1]. Moreover, during the experiments it is known that the proposed topology, ensures continuous input current in the ST operating mode, thus featuring the reduced stress of the input voltage source. Despite the reduced ST duty cycle, the proposed qZSI, provides the demanded twofold boost of the input voltage. The proposed topology provides a reduction of 25% in the ST duty cycle at the same input voltage boost factor. It is obviously known that in proposed qZSI the value of inductors and capacitors will be 21% and 25% less than conventional structure respectively. Despite the increase number of passive components and their summarized values, rated values of the inductors and capacitors of the proposed qZSI could also be reduced in comparison with the presented qZSI in [1]. For example, despite the 25% capacitance reduction, the summarized capacitance value required for the proposed qZSI ($C_1+C_2+C_3+C_4+C_5+C_6$) is 12.5% higher than that of the presented qZSI in [1]. The summarized value of the required inductance ($L_1+L_2+L_3+L_4$) will also be 4.53% higher.

Table.1.
Usable parameters for proposed qZSI for $D_{ST} = 0.125$

V_i	$44V$	
D_{ST}	0.125	
$C_1=C_2=C_3=C_4=C_5=C_6$	$180\mu F$	
$L_1=L_2=L_3=L_4$	$29.4\mu H$	
Output load values	$R_L = 10\Omega$	$L_L = 1mH$
Frequency reference	$50Hz$	
Frequency switching	$10kHz$	

Table.2.
Results of theoretical and simulation of the proposed qZSI

	Computational results	**Simulation results**
V_{C1}	55	54.99
V_{C2}	33	33.16
V_{C3}	66	65.8
V_{C4}	22	22.37
V_{C5}	11	11.21
V_{C6}	11	10.79
$v_{L1}=v_{L2}=v_{L3}=v_{L4}(non-ST)$	-11	-11
$v_{L1}=v_{L2}=v_{L3}=v_{L4}(ST)$	11	16.9
$v_{dc,\max}$	88	88.1



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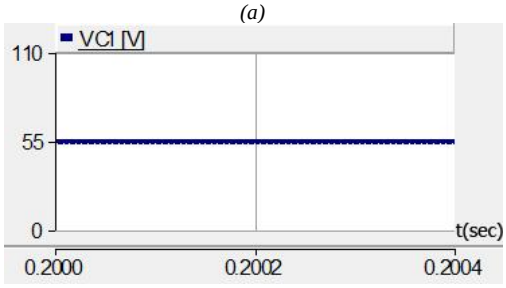

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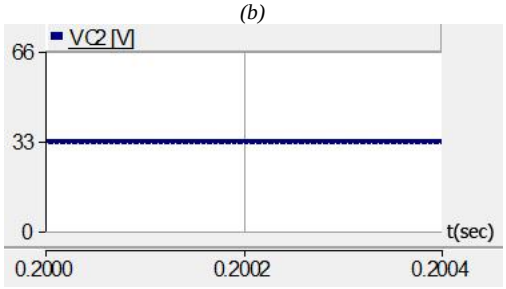

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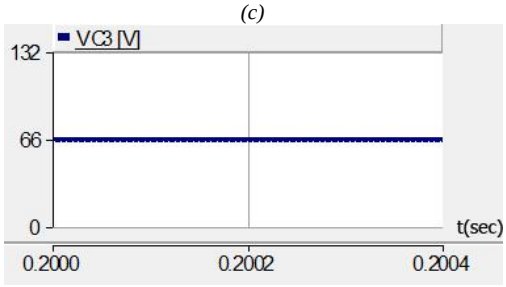

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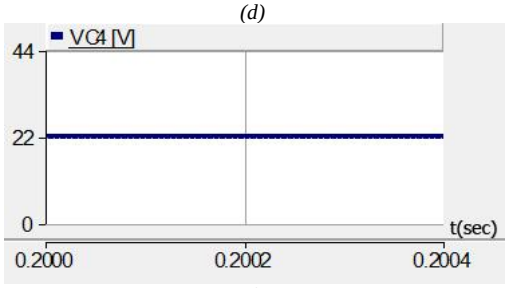

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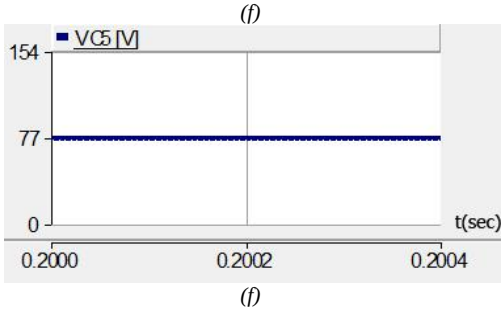

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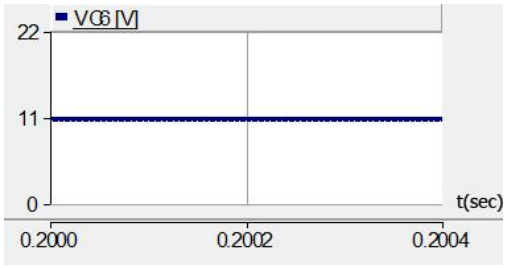

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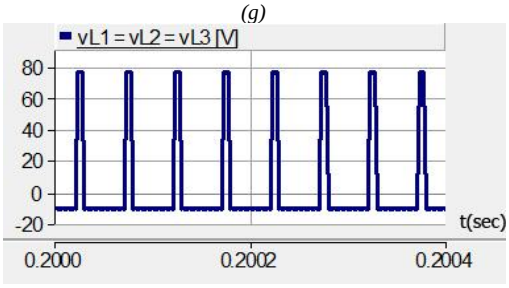

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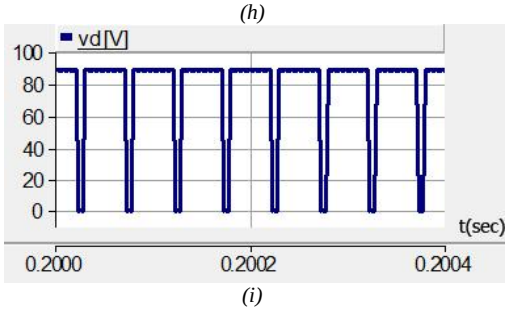

(i)

Fig. 5. Measured waveforms of the proposed qZSI for $D_{ST} = 0.125$ (a) input voltage converter (b) voltage across the capacitor C_1 (c) voltage across the capacitor C_2 (d) voltage across the capacitor C_3 (e) voltage across the capacitor C_4 (f) voltage across the capacitor C_5 (g) voltage across the capacitor C_6 (h) voltage across the inductors (i) output voltage converter

References

[1] D.Vinnikov, I. Roasto, R. Strzelecki, and M. Adamowicz, "Step-up dc/dc converters with cascaded quasi-Z-source network," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3727-3736, Oct. 2012.

[2] F.Z. Peng, "Z-Source inverter," *IEEE Trans. Ind. Appli.*, vol. 39, no. 2, pp. 504-510, March/April 2003.

[3] F. Z. Peng, M. Shen, and Z. Qian, "Maximum boost control of the Z-Source inverter," in *Proc. IEEE PESC*, pp. 255-260 ,2004.

[4] J. Anderson and F.Z. peng, "Four quasi-Z-source inverters," in *Proc. PESC*, Rhodes, vol. 15, no. 19, pp. 2743-2749, June,2008.

[5] F.Z. Peng, "Z-Source inverter for motor drives," in *Proc. PESC*, pp. 249-254,2004.

[6] F.Z. Peng, X. Yuan, X. Fang, and Z. Qian, "Z-Source inverter for adjustable speed drives," *IEEE Power Electron. Lett.*, vol. 1, no. 2, pp. 33-35, June 2003.

[7] M. Shen, J. Wang, A. Joseph, F.Z. Peng, L.M. Tolbert, and D.J. Adams, "Maximum constant boost control of the Z-Source inverter," in *Proc. IEEE IAS*, 2004.

[8] Y. Li, J Anderson, F.Z. Peng, and D. Liu, "Quasi-Z-source

inverter for photovoltaic power generation systems," in *Proc. APEC*,Washington DC, vol. 15, no. 19, pp. 918-924, 2009.

[9] J.-H. Park, H.-G. Kim, E.-C. Nho, T.-W. chun, and J. Choi, "Grid connected PV system using a quasi-Z-source inverter," in *Proc. APEC*, 2009, Washington DC, vol. 15, no. 19, pp. 925-929.

[10] D. Vinnikov, and I. Roasto, "Quasi-Z-source-based isolated dc/dc converters for distributed power generation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 192-201, Jan. 2011.

[11] B.Y. Husodo, M. Anwari, S.M. Ayob, and Taufik, "Analysis and simulations of Z-source inverter control methods," *9th IPEC, 2010 Conference proceedings*, pp. 699-704, Oct. 2010.