A Novel Technique for Low Power Consumption Based on Switch Capacitor in CMOS Circuits

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Abstract

The share of static power from the total consumed power in deep submicron circuits is rapidly rising due to short channel effects. The present paper examines the recent techniques introduced for reducing leakage power and proposes a novel technique based on switched-capacitor (SC) circuits for this purpose. The central concept consists of using two SCs on the route to PUN and PDN up to the output. Very high temperature stability and the ability to control the SC circuits using the clock frequency (f_c) are among the benefits of the proposed concept. The introduced technique was implemented on NAND, NOR, and XOR logic gates and the C17 standard circuit. Next, the proposed model was simulated in HSPICE software with 32-nm BSIM4 (level-54 parameters) CMOS technology to investigate its leakage power, delay, surface area, and PDP factors. The results indicate the excellent leakage power reduction performance of this technique compared to previously introduced techniques. Implementing the presented circuit in various corners of the process and a subsequent temperature stability analysis demonstrated the high reliability of the proposed technique.

Keywords: Leakage Power; Switch Capacitor; Low Power Design; Deep Nanometer
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1. Introduction

Today, the use of submicron technology, as well as miniaturization of technology, has made it easier for electronic circuit designers to fabricate integrated circuits on chips and access smaller, higher-speed digital circuits. Besides, a rise in computational burden and the sophistication of circuits has increased the power consumption of these chips per unit surface area, leading to an increase in chip temperature. As a result, a larger cooling capacity is needed, increasing the circuit's volume and final cost. In this respect, researchers have attempted to miniaturize the transistor and reduce the circuit's supply voltage to decrease power consumption and prevent circuit damage. Besides, with a reduction in the supply voltage, one will need to lower the threshold voltage of the transistor to achieve optimal performance. This issue has exponentially increased the subthreshold current and remarkably raised the static power consumption in recent years[1], [2] . Various approaches have been recently suggested for reducing static power consumption and enhancing circuit performance. Some of these approaches improve the pull-up network (PUN) and the pull-down network (PDN) resistance toward the output node [3]–[5].Some others are based on disconnecting the power supply from the standby transistors. Each of these groups has advantages and disadvantages [6], [7]. Although most of the proposed techniques reduce the static power of the circuit, they increase the total power consumption or power-delay product (PDP) by increasing the dynamic power or delay. For decades, dynamic power had taken up the largest share of total power consumption (i.e., 70%-90% of the power consumed in CMOS circuits). However, the advent of submicron technology in recent years has highlighted the significance of leakage power. Today, increasing its share to more than 50% of total power consumption in modern technologies has become one of the important concerns of VLSI designers [8]. The most important component of the leakage power is the subthreshold current, which

flows between the drain and the source when VGS is smaller than the threshold voltage[9], [10]. Hence, the present research utilizes SC circuits to reduce the subthreshold current and the static power. It is of note that lower power consumption is achieved at the cost of higher speed and a larger surface area. Therefore, attempts to meet these requirements simultaneously will complicate the design of low-consumption circuits. Kao et al.[11] proposed a method called dual threshold voltage to enhance the route resistance and reduce the leakage current. To this end, they tried to find non-critical routes and place high-threshold-voltage transistors in those routes. Since a non-critical route is less active than a critical route, the output of this route is prepared earlier than that of a critical route. Accordingly, one can reduce the leakage current by using transistors with higher threshold voltages in non-critical routes such that the output is ready at the same time as that of the critical routes, and the logic performance of the circuit is not compromised. The drawbacks of this technique include complexity and the probability of error in the critical and non-critical route detection algorithms. Drake et al. introduced a novel technique, called Variable threshold voltage MOSFET (VTMOS), to reduce the leakage current. This technique can be considered a type of body bias, in which the transistor bodies are set to active bias by switching between the two created voltage levels to increase the circuit speed. Also, the transistor body is set to reverse bias to increase resistance and reduce the leakage current in the standby mode. This technique requires twin well or triple well technology since it uses two different body voltage levels[12]. Mutoh et al. and Kao et al.[11] introduced the Multi-threshold CMOS (MTCMOS) method for decreasing the leakage current.

This method decreases the leakage current in the standby mode. Although this technique declines the leakage current in the circuit, it suffers from disadvantages such as data loss during trips and the difficulty in determining the transistor sizes for correct circuit performance in large designs. By introducing SKA (Sleepy keeper Approach), Hun et al.[14], applied two auxiliary transistors and sleep transistors in the PUN and PDN to decrease leakage current. In this paper, in order to reduce power consumption and power supply circuit, control signals have been used to turn transistors on and off in standby and active modes. Lorenzo et al.[15], applied the Dynamic Threshold Sleep Transistor (DTST) method to reduce power leackage. This method used two DTMOS transistors in the PUN and PDN. The connection between the gate and the body in LCT transistors prevents a good transistor status during switching, hence increasing the delay. Johanna et al.[16]introduced a hybrid method for reducing power consumption in a circuit. They applied two parallel PMOS transistors placed in series in the route from the Vdd to the PUN, an N transistor in the route of the PDN up to the ground, and a P transistor diode mode between the input and the PDN. Even though this method increased the route resistance toward the output and cut the power consumption, it increased delay and destroyed the symmetry of the circuit [15], [16]. Mistry et al. proposed the sub-clock power gating technique to reduce power consumption by lowering the voltage and the frequency. However, this technique can only be used in circuits with a relatively low clock pulse, which is considered critical] Woong Chun et al.[20] revised transistor configuration in the reference gates and examined their advantages and disadvantages to propose various algorithms for obtaining a novel transistor configuration. Overall, they demonstrated the lower power consumption of the proposed circuits compared to those in the literature. Drawbacks of this design include a need for major modifications in standard circuits. Pratap and Kumre presented a method based on configuring the transistors in series and increasing the resistance to decrease the leakage current. Although this merhod significantly reduced the leakage power and leakage current, it eliminated the symmetry of the circuit, hindering the simultaneous arrival of various inputs at the output [21], [22]. Using one transistor pass (transistors that disconnect specific routes in the circuit) at the input of the logic gates and selecting the best input to obtain the smallest leakage current was proposed by Rani et al.[23] This method reduces the leakage current and delay compared to TG by turning off the gates during stand by via the determined inputs to the transistor pass. Notably, the decrease in the power–delay product (PDP) is lower in this circuit than in others .Gong et al.[24] reduced the leakage current in nanometer-scale transistors by using the properties of transistors in series, increasing the route resistance, and determining their optimal length and width. The difficulty in determining the transistor sizes in more complex circuits is a major shortcoming of this method. An another technique, Asyaei et al.[25], [26], introduced a new technique that, moreover to reducing power consumption, increase the noise immunity of wide fan-in gates in nano-scale technologies. This technique has reduced the power consumption and leakage current by reducing the swing voltage of PDN network and using stack, respectively.

2. Proposed Design

In this paper, a new design was proposed to decrease the leakage current in digital circuits based on switch capacitance. The overall structure

of the proposed design is shown in Fig. 1, where the capacitor shift circuit is used to increase PUN and PDN resistance to reduce static power consumption.

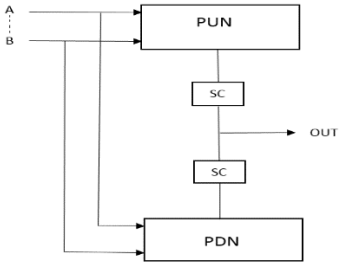

Fig. 1. Proposed circuit

According to the proposed scheme, firstly the capacitive circuit of the circuit is studied. The schematic of the SC (Switching Capacitor) circuit is generally shown in Fig. 2.

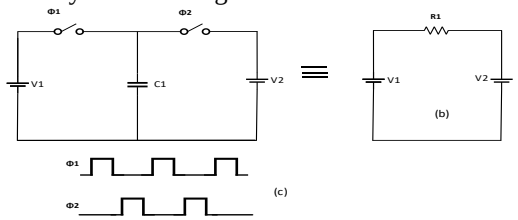

Fig. 2. a. Switch capacitance b. Relative resistance circuit c. non-overclock clock pulses

A circuit diagram of the capacitor switch is shown in Figure 2. The non-overlapping clock pulses shown in Fig. 2(c) are two logic signals with a single frequency, arranged so that they do not occur at the same time, and do not interact with each other. To ensure that the charge does not suddenly disappear, the high time should be controlled so that there is a perfect time to charge the electric charge in the circuit.By writing the conventional equations for the circuit 2-a, in terms of capacitance:

$$Q_a = C_x V_x \quad (1)$$

Now assume that Q1, Q2 are two non-overlap clock pulses, as illustrated in Fig. 2(c). In this case, the C1 capacitor is charged with V_1 , and then to V_2 at each clock period. ΔQ_1 is also the charge between the nodes V_1 and V_2 transmitted and calculated as follows:

$$\Delta Q_1 = C_1(V_1 - V_2) \quad (2)$$

Given that the load transmitted in each period of the clock cycle is repeated, and the equivalent current can be calculated from the transmitted load divided by the clock frequency rotation, thus the average current I_{avg} is equal to (expressed in amperes):

$$I_{avg} = \frac{C_1(V_1 - V_2)}{T} \quad (3)$$

In which T is the periodic clock ($f_s = \frac{1}{T}$ is the sampling frequency).

Similarly, for Figure 2(b), we can write as follows:

$$I_{avg} = \frac{(V_1 - V_2)}{R} \quad (4)$$

By comparing the two equations (3) and (4), we can see:

$$R = \frac{T}{C} = \frac{1}{fc} \quad (5)$$

Considering that the relationship (5) creates the sensory sense, so that if the clock frequency increases, the same load is transmitted at any clock but faster. Therefore, the current flow will be higher. Now, if capacitor C increases, a larger amount of load will be transmitted in each period, and as a result, the average flow will increase. As shown in Equation (5), the resistance can be controlled with the frequency of the switches, meaning that the frequency increases the switch's resistance and, by decreasing it, increases the resistance. In this research, this structure is used in digital circuits to reduce the leakage current and control it with the operating frequency of the circuit. The schematic representation of the NAND gate is displayed by placing the SC block in Fig.3.

The circuit schematic of the block SC is shown in Fig. 4.

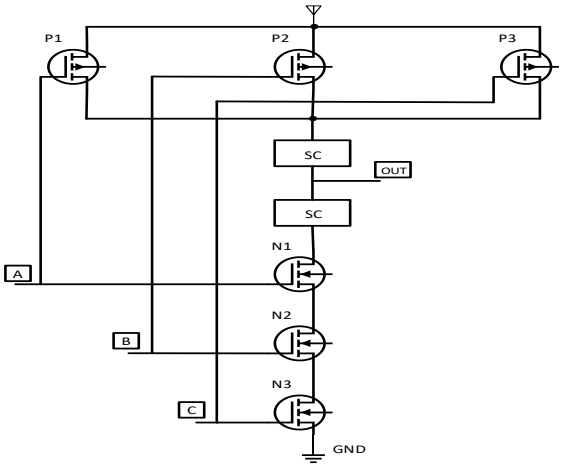

Fig. 3. NAND gate circuit for three inputs with SC added to reduce the flow below the threshold

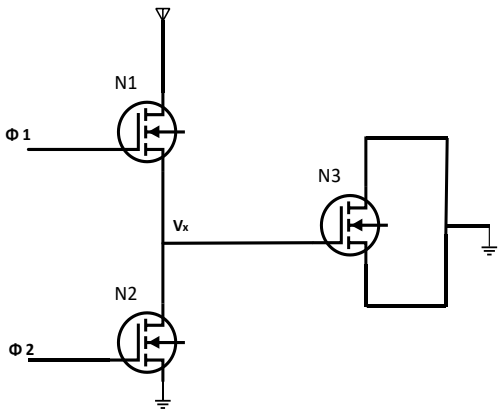

Fig. 4. Capacitor Switch SC

In the circuit shown in Fig. 4, the N3 transistor is used as a capacitor, which can be obtained by selecting its parameters to obtain the desired capacitor capacitance for adjusting the desired resistance in different circuits. Also, 1φ and 2φ of the non-overlap clock are shown in Fig.2(c). In the following, the effect of reducing the leakage current is proved by studying the proposed circuit equations. As we know, I_{ds} transistors can be represented by Equation (6).

$$I_{ds} = I_{ds0} e^{(V_{gs}-V_{to}-k_\gamma V_{sb}+\lambda_d V_{ds})/nV_T}(1- e^{-V_{ds}/V_T}) \quad (6)$$

Whereλ_d is the DIBL(Drain-Induced Barrier Lowering) factor, and k_γ is the fixed body effect and n character is dependent on the technology used [27].

If the parameter S is expressed as the sub-threshold slope and as the relation (7)

$$S = [\frac{d(log_{10} I_{ds})}{dV_{gs}}]^{-1} = nV_T \ln 10 \quad (7)$$

Therefore, the leakage current can be shown in (8).

$$I_{ds} = I_{off}\, 10^{(V_{gs}-k_\gamma V_{sb}+\lambda_d (V_{ds}-V_{dd}))/S}(1- e^{-V_{ds}/V_T}) \quad (8)$$

The current I_{off} is below the threshold in V_{gs}=V_{sb} =0 and $V_{ds} = V_{dd}$. If $V_{ds} \geq \frac{3KT}{q}$ is considered, we can write Equation (9) as follows.

$$I_{ds} = I_{off}\, 10^{(V_{gs}-k_\gamma V_{sb}+\lambda_d (V_{ds}-V_{dd})/S} \quad (9)$$

By studying the leakage current in the capacitor switching circuit shown in Fig. 4, which has the same behavior as the stack state, its effect on reducing leakage current can be observed. In terms of stability (Q_1 and Q_2 are off, $V_{b_1} = V_{b_2} = 0$), if the midpoint voltage (gate N3) is called V_x, then the transistor current is equal to:

$$I_{N1} = W_1 I_{off} 10^{\frac{-(1+\lambda_d+k_\gamma)V_x}{s}}$$
$$I_{N2} = W_2 I_{off} 10^{\frac{-\lambda_d(V_{dd}-V_x)}{s}} \quad (10)$$

By equating the flow rate at the midpoint, the voltage of this point can be obtained as follows:

$$I_{N1} = I_{N2} \Rightarrow W_1 I_{off} 10^{\frac{-(1+\lambda_d+k_\gamma)V_x}{s}} = W_2 I_{off} 10^{\frac{-\lambda_d(V_{dd}-V_x)}{s}} \Rightarrow V_x = \frac{\lambda_d V_{dd}+S\log\frac{W_1}{W_2}}{1+2\lambda_d+k_\gamma} \quad (11)$$

By placing V_x obtained from the above equation in one of the equations (10), and given that $k_\gamma \leq 1 + 2\lambda d$, the leakage flow rate can be obtained as follows.

We write the equations for relationI_{N2} as follows:

$$I_{leak} = W_2 I_{off} 10^{\frac{-\lambda_d V_{dd}}{s}} 10^{\frac{\lambda_d V_x}{s}} = W_2 I_{off} 10^{\frac{-\lambda_d V_{dd}}{s}} \left[10^{\frac{\lambda_d\left(\frac{\lambda_d V_{dd}+S\log\frac{W_1}{W_2}}{1+2\lambda_d}\right)}{s}}\right] =$$
$$W_2 I_{off} 10^{\frac{-\lambda_d V_{dd}}{s}} \left[10^{\frac{\lambda_d}{s}\left(\frac{\lambda_d V_{dd}}{1+2\lambda_d}\right)} * 10^{\frac{\lambda_d\left(S\log\frac{W_1}{W_2}\right)}{s(1+2\lambda_d)}}\right] =$$
$$W_2 I_{off} 10^{\frac{-\lambda_d V_{dd}}{s}} \left[10^{\frac{\lambda_d}{s}\left(\frac{\lambda_d V_{dd}}{1+2\lambda_d}\right)} * 10^{\alpha\,(\log\frac{W_1}{W_2})}\right] =$$
$$W_1^{\alpha} W_2^{1-\alpha} I_{off} 10^{\frac{-\lambda_d V_{dd}}{s}(1-\alpha)} \quad (12)$$

In the above equation, $\alpha = \frac{\lambda_d}{1+2\lambda_d}$ is considered. Considering the relation (12), it can be seen that, using the SC technique, the leakage current can be significantly reduced. Considering the usual value for λ_d and s, this property can reduce the leakage current by about 10 times.

In this case, the value of V_{ds} for the main gate is equal to V_{dd}, maximizing the leakage current.

The amount of leakage current passing through three transistors P is obtained as follows, which is similar to P transistors:

$$I_{sub} = I_{sub1} + I_{sub2} + I_{sub3} = 3 * I_{ds0} e^{(V_{gs}-V_{to}-k_\gamma V_{sb}+\lambda_d V_{ds})/nV_T}(1-e^{-V_{ds}/V_T}) \quad (13)$$

By measuring the leakage current, SC can be used to reduce leakage current by applying the SC technique and controlling the resistance produced by this circuit. Due to the connection of the source and the drain in the N3 transistor, the transistor is located in a strong inversion zone, which is best suited for its capacitive property. Considering the dimensions and 32nm technology, this transistor is equivalent to a capacitance of 175pf, so that the best conditions can be provided for high point of V_x in order to make the calculations more accurate, and increasing the | V_{sb} | to further reduce the flow of leakage. According to the above-mentioned circuit diagrams Fig.1 is proposed to reduce very high leakage current in digital circuits.

3. Results

The proposed circuit are simulated by using HSPICE software based on Berkeley predictive 32 nm technology model (BSIM4) with $V_{dd} = 0.8\,V$ at 27 ° C [10]. delay, Static power, area and PDP are the factors evaluated in the analysis, the results of which are presented in the following. The W / L ratio of PMOS transistors is considered as 128/32 nm, and for NMOS transistor it is considered as 64/32nm. The input pulse range may vary from 0 - 0.8 volts, in addition to the main NAND gate on the main Gates NOR, XOR, as well as C17, the analysis was done from MCNC'91 bench circuits whose circuits are shown in Fig 5. The results were also compared with those of recent methods such as DTST, LECTOR, GALEOR, DLSL, and DG. In this research, the power and delay caused by the non-overclock clock pulse source were not investigated.

A) Static power (Leakage power (W))

The static power consumption is referred to the power consumed in standby mode, so that to calculate its pulse signal, the unplugged clock will cut the input to the SC circuit and reduce the leakage current. To accurately calculate the power consumption, all the input states of the test circuits and its total as power consumption are applied as shown in Table1.Tables 2 and 3 and Figures 6 and 7, respectively show the proposed method, which can be used in different corners of NAND and NOR gates for the process. As can be seen, the proposed method has high reliability. As seen in all design corners of the process, power consumption is always much lower than other methods.

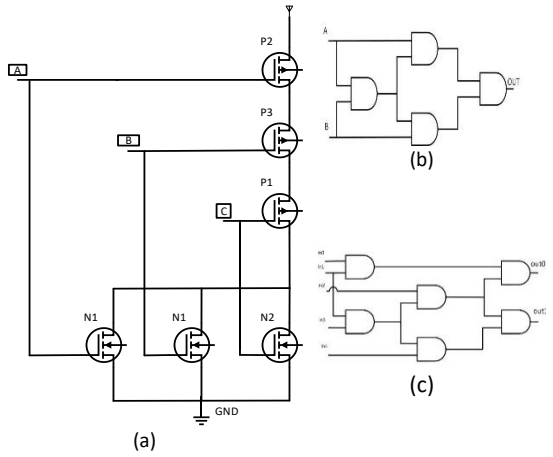

Fig. 5. Gate Circuits a. NOR b: XOR c. C17 [13]

Table.1.
Leakage power (W) in CMOS gates and benchmark Circuits

Technique	*NAND*	*NOR*	*C17*	*XOR*
Conventional	1.90E−08	1.72E−08	5.23E−04	1.81E-8
LECTOR	1.87E−08	7.31E−09	6.87E−05	1.175E-8
GALEOR	1.59E−08	6.02E−09	6.15E−05	13.4E-8
DLSL	1.10E−09	1.08E−09	4.01E−05	1.77E-10
DG	7.41E−09	1.76E−09	5.77E−05	4.8E-9
DTST	1.20E−09	1.11E−09	4.25E−05	2.618E-8
proposed	8.494E-10	8.18E-10	1.543E-05	2.56E-09

Table.2.
Leakage power of two-input NAND gate at different corners of the process (W)

Corner	*00*	*01*	*10*	*11*	*Total*
SS	21.57E-11	19.38E-11	14.24E-11	1.42E-11	5.661E-10
FS	25.41E-11	21.60E-11	15.56E-11	1.36E-11	6.393E-10
SF	66.52E-11	64.57E-11	51.90E-11	5.01E-11	18.80E-10
FF	90.27E-11	74.47E-11	66.53E-11	77.3E-11	44.35E-10
SS	2.540E-10	03.16E-10	02.56E-10	2.36E-11	8.494E-10

Table.3.
Leakage power of two-input NOR gate at different corners of the process (W)

Corner	*00*	*01*	*10*	*11*	*Total*
SS	57.59E-11	6.85E-11	11.19E-11	13.4E-11	26.16E-11
FS	37.4E-11	6.88E-11	11.21E-11	13.4E-11	27.12E-11
SF	24.01E-10	40.32E-11	58.8E-11	60.7E-11	80.152E-11
FF	43.5E-10	87.04E-11	83.36E-11	87.5E-11	176.66E-11
SS	8.17E-10	7.32E-11	14.33E-11	18.6E-11	42.56E-11

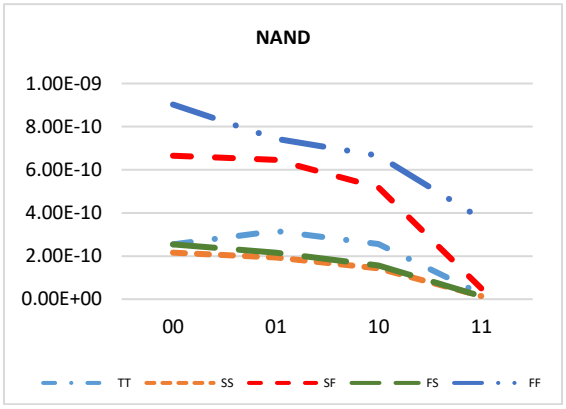

Fig. 6. Leakage power NAND gate graph at different process corners

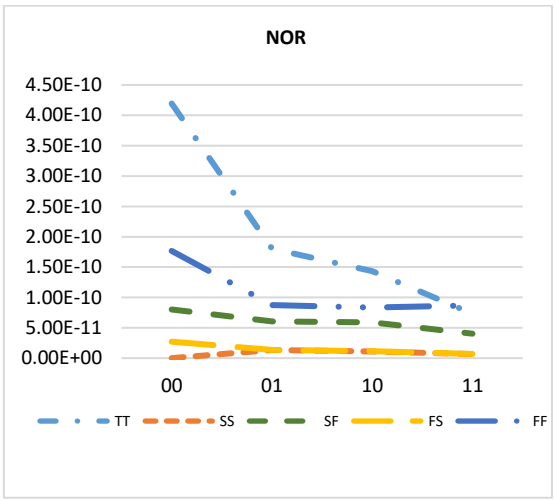

Fig. 7. Leakage power NOR gate graph at different process corners

B) Delay

As shown in Table 4, the propagation delay was calculated for random inputs in different functions as well as standard functions. The comparison of the results of different techniques with each other, and the original circuit showed that, the average delay penalty is equal to 30.01% in the proposed technique, with the optimal response to the GALEOR and DLSL techniques. It should be noted that, the delay caused by various techniques results

from the presence of transient current decreasing transistors. The output and input waveforms for the NAND, NOR and XOR Gates are shown in Figures 8 to 10, indicating very low latency of the proposed technique. In the proposed circuit, although the amount of delay increases relatively due to the use of SC transistors, but on the other hand, the proposed technique reduces the important amount of leakage current by reducing the important factor of PDP, which indicates an increase in circuit efficiency.

C) Area Comparison

An electric tool was used with 32nm technology for layout area, and area comparison was calculated. According to the results presented in Table 5, the area of the target circuits was determined using other designs, and the increase in the area of the proposed technique is attributed to the use of three transistors in the SC section.

Table.4.
propagation delay in different techniques (s)

Technique	***XOR***	***C17***	***NOR***	***NAND***	***Avg. penalty%***
Conventional	9.99E-8	6.02E-07	1.3E-11	1.6E-11	-
LECTOR	1.01E-7	8.01E-07	4.1E-11	4.0E-11	28.1
GALEOR	1.34E-7	9.03E-07	8.0E-11	8.0E-11	37
DLSL	8.43E-7	8.96E-05	2.4E-11	1.9E-11	99.2
DG	9.99E-8	7.85E-07	1.7E-11	1.8E-07	27.54
DTST	1.06E-7	6.55E-07	2.8E -10	2.3E-10	13.04
Proposed	1.00E-7	9.23E-07	6.3E-11	4.9E-11	30.01

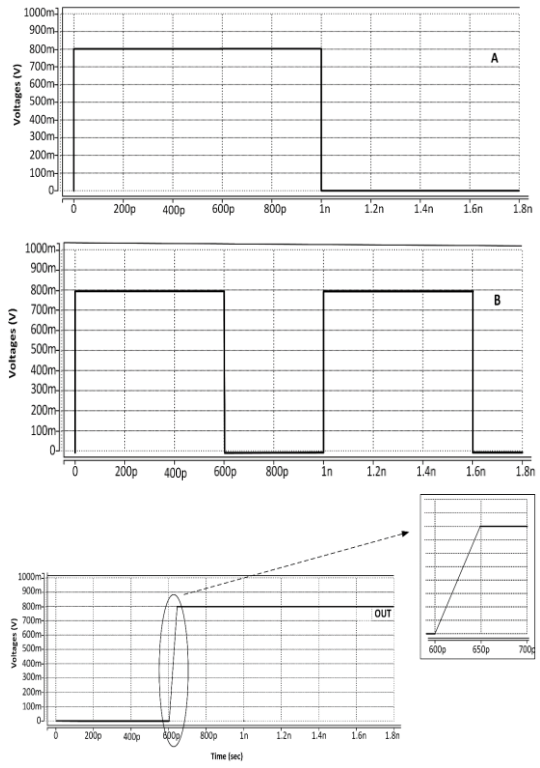

Fig. 8. Waveform output of two input NAND gate, two inputs A and B and output

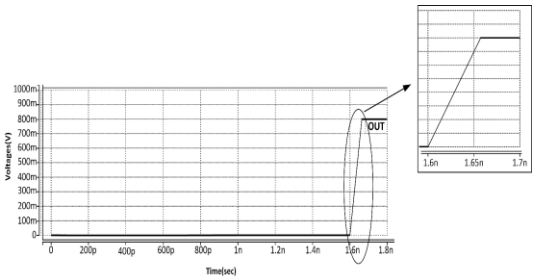

Fig. 9. Waveform output of Proposed Design for two input NOR gate

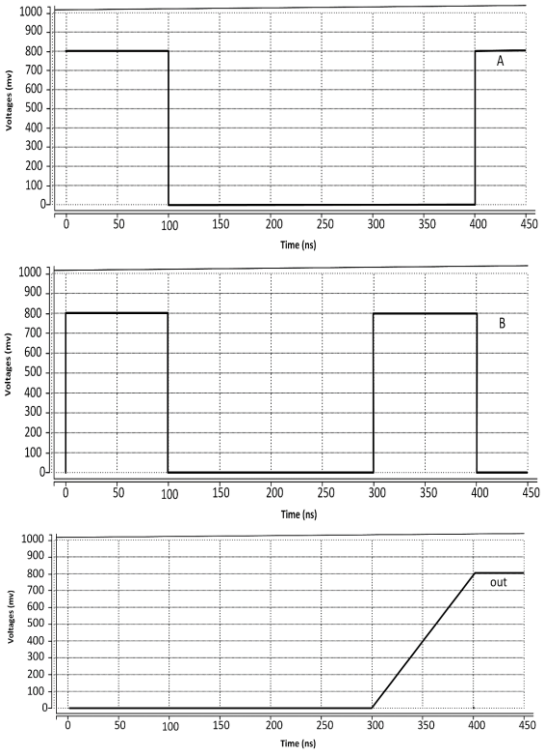

Fig. 10. Waveform output of two input XOR gate

Table.5.
Area comparison $(\mu m)^2$

Technique	***OR***	***C17***	***NOR***	***NAND***	***Avg. penalty%***
Conventional	31.5	4829	28.7	28.5	-
LECTOR	36	5610	30.6	31.5	28.1
GALEOR	35.4	5780	30.1	31.5	37
DLSL	39.1	5921	36.9	35.8	99.2
DG	38.4	5819	36.1	35.5	27.54
DTST	45.6	6125	41.3	42	13.04
Proposed	49.5	6385	45.5	47	30.01

D) Post Layout Simulation

Fig. 11 and Fig.12 illustrate the layout design and post-layout simulation of the proposed technique in two input NAND gate as depicted in figure 8 (a). As can be seen, the propagation delay in the circuit and post layout simulations is calculated as 49.8 ps and 52.1 ps, respectively. The

static power consumption in the circuit and post layout simulations is calculated as 423E-18 w and 501E-18 w, respectively. As shown in the post layout simulation, the proposed method has the highest leakage power savings, the lowest propagation delay and the lowest PDP-static rate compared to other techniques proposed so far.

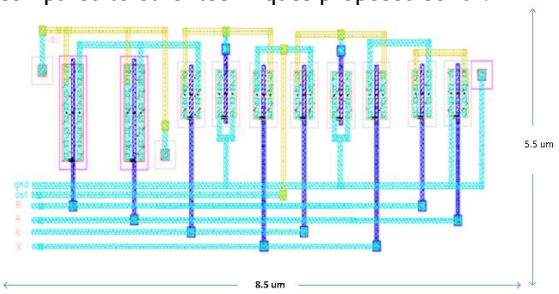

Fig. 11. Layout of proposed two-input NAND gate circuit

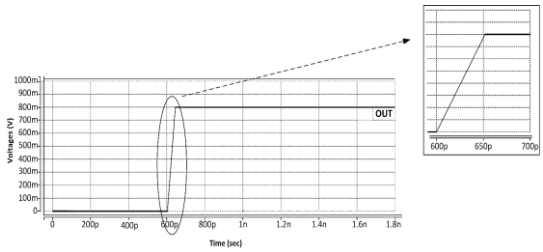

Fig. 12. Output voltage Waveform based on post layout simulation result

E) Temperature variations

Stability of the proposed technique and other method with respect to temperature variations is also studied for temperature in the range of 0 to 80 °C with 5 °C steps and is illustrated in Fig. 13. The proposed technique operates properly in different temperatures ranging from 0 to 80 °C and have better leakage in all temperatures.

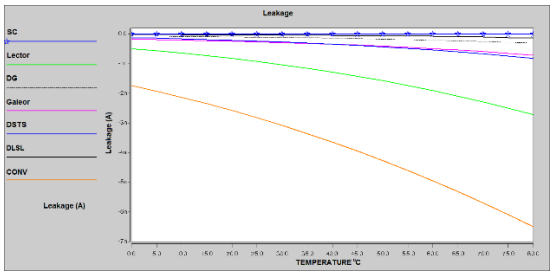

Fig. 13. Leakage current in different temperatures

F) Static Power-Delay Product (PDP)

PDP is calculated using the propagation delay and leakage power, the results of which are shown in Table 6. The amount of this factor was found to be very low in the proposed methods and other methods, and has a significant decrease of about 95.4% respect to the conventional design.

Table.6.
Static PDP (w)

Technique	*XOR*	*C17*	*NOR*	*NAND*	*Avg. P.%*	*Avg. S%*
Conventional	9.08E-16	3.15E-10	6.66E-18	4.64E-18	-	-
LECTOR	11.5E-16	5.50E-11	4.11E-18	1.06E-17	-	82.5
GALEOR	17.8E-15	5.55E-11	4.03E-18	1.28E-17	-	82.3
DLSL	14.9E-17	3.29E-09	8.80E-18	3.14E-17	90.4	-
DG	5.52E-16	3.29E-09	8.78E-19	3.04E-18	90.4	-
DTST	24.2E-16	2.78E-11	4.17E-19	3.42E-19	-	91.1
Proposed	2.56E-16	1.42E-11	5.15E-20	4.23E-20	-	95.4

4. Conclusion

In this paper, some techniques used for leakage current minimization were reviewed, and a new technique was proposed for reducing leakage current in CMOS circuits using capacitive switches, then the advantages and disadvantages of each technique were identified and were compared regarding the power, propagation delay, area, and static PDP. The results obtained using 32nm process technology and other conditions mentioned in Section 4 indicated that, the proposed technique is very successful in reducing static and PDP power compared to other techniques. The delay also decreased compared to the techniques of GALEOR and DLSL Circuit. Area was found to be more occupied due to the increase in the number of flow-reducing transistors in the proposed circuit, which is usually less important in the design of low-power electronic circuits than other metrics. The results of the NAND and NOR gate analysis at different corners of the process showed that, the proposed circuit has high reliability. It should be noted that, controlling the resistance level of SCs with frequency is also one of the strengths of the proposed scheme, which can be used cautiously in this regard.

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