Design of Multiple-Valued Interconnection Networks with Gate all Around Transistor for Smart Computer Networks

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Abstract

In junctionless nanowire transistors, drain-channel-source doping is of the same type and level. Therefore, fabricating junctionless transistors is less complicated than inversion mode transistors. However, the reduced ratio of on current to off-state current (ION/IOFF) in junctionless nanowire transistors has made their operation difficult due to the high impurity scattering in the channel. The larger ION / IOFF ratio indicates an increase in transistor switching speed. In this study, the use of gate oxide engineering is proposed to increase of ION / IOFF ratio. The proposed oxide thickness is 1.5nm, which is a buffer layer with K = 5.7 and a thickness of 0.5nm, and the oxide with a high permittivity factor with K = 29 and a thickness of 1nm. The proposed structure is called GAA-JL-FET-with-oxide buffer layer. In GAA-JL-FET-with-oxide buffer layer, the ION / IOFF ratio has been improved by about 10^6 and 10^2 times compared to the structure with K = 3.9 and K = 7.5, respectively. Due to the high switching speed, the GAA-JL-FET-with-oxide buffer layer is applied to design the multiple-valued logic (MVL) interconnection network in the voltage mode for the first time using the mixed-mode tool in Silvaco software. The results reveal improving subthreshold parameters of the simulated device significantly enhance the average power, max delay and power delay product (PDP) of the proposed interconnection networks.

Keywords: Smart Computer networks; Junctionless FET; Multiple-Valued Logic; Interconnection Network; High Speed
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1. Introduction

With the development of technology, dimensions of metal-oxide-semiconductor field-effect transistors (MOSFETs) are scaled down to the sub-micrometer regime. Scaling has led to the emergence of short-channel effects (SCEs) and decrease in device performance [1-4]. Moreover, source/channel and drain/channel junctions in nanoscale inversion mode transistors have ultra-sharp impurity density gradients [5,6]. Changing doping from source to channel and drain to channel when fabricating these transistors is very complicated and requires using the millisecond microwave thermal annealing technique [7,8]. As a result, the cost of manufacturing nanoscale inversion mode transistors increases [9,10]. The junctionless field-effect transistor (JL-FET) has been recently proposed to solve this problem [11,12], in which source-channel-drain doping is selected of the same type and level [11,12]. Thin body thickness is the key point in manufacturing JL-FETs because it causes the carriers to completely depletion the channel in the OFF state [11,12]. The advent of multi-gate transistors has provided a new path for manufacturers [13-15]. The electrical properties of junctionless transistors are improved with increasing the number of gates [16,17]. In these structures, subthreshold parameters are significantly improved due to the desirable gate control over the channel [16,17]. GAA structures have more ON and less OFF state currents. The electrostatic control of the gate over the channel is greater in GAA structures Therefore, GAA structures have more desirable

subthreshold parameters than other structures [18,19]. Parallel computing and processing have long been inspected as an interesting area of research [20]. Interconnection networks (ICNs) are an inevitable part of every parallel system [21]. Therefore, new techniques for interconnection networks are crucial. Also, interconnection networks are essential parts of the Network-on-Chip (NoC) [22]. In recent years, considerable attention has been received on NoC to solve System-on-Chip (SoC) interconnect problems like providing a flexible path toward complex fabrication topologies with abundant amounts of available bandwidth [23]. Interconnection networks as the major part of network-on-chip (NoC) have always been of interest for researchers [24]. In the current integrated circuits, an important part of the chip latency and area is associated with communication links [25]. Therefore, new devices are required to provide communication in interconnection networks for reducing power consumption, increasing speed and decreasing chip size [26,27]. Increasing the speed and reducing the power consumption are directly associated with reducing the number of links in the system [28]. Therefore, the present study aimed to design interconnection networks using GAA junctionless transistors. Based on this concept, GAA junctionless transistor with gate oxide engendering was proposed. In the proposed device, a buffer layer with K = 5.7 and a thickness of 0.5nm, and a high K-oxide with K = 29 and a thickness of 1nm. The proposed device was applied to design interconnection networks by the mixed-mode tool in Silvaco software. Multiple-valued logic was employed to design interconnection networks in the voltage mode. The simulation results revealed improving subthreshold parameters of the simulated device significantly improved the parameters of the proposed interconnection networks.

1. Device structure and simulation method

Figure 1 illustrates the junctionless nanowire transistor structure. The band offset between the source and channel was considered an important factor in the performance of the proposed structure. In the n-channel device, conduction band of the source should be higher than that of the channel. This band offset could cause electrons to be injected into the channel faster [29]. The channel length, source/drain length and body width were 7 nm, 6.5 nm and 5 nm, respectively. Moreover, thickness of the gate oxide, made of SiO2, was 1 nm. The gate was composed of p+-type polysilicon with the work function of 5.1 eV and Dirichlet boundary conditions were considered [30]. Source, drain and channel doping was of the donor type at $4\times10^{20}cm^{-3}$ and channel doping was of the donor type at $1\times10^{20}cm^{-3}$. Neumann boundary conditions were considered for source and drain contacts [31].

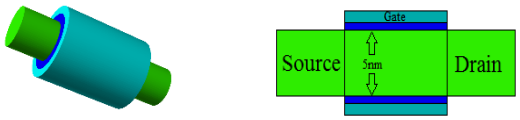


Fig. 1. (a) The structure presented in this paper and (b) the cross section of the proposed device

In order to simulate the proposed structures, the commercial tool was used. The Mode Space Non-Equilibrium Green's Function (MS_NEGF) approach is used to determine the electrical characteristics of the proposed structures. The NEGF model is coupled to the Schrödinger-Poisson equation to extract the amounts of current and electron density. In order to find the eigen energy and eigen function the Schrödinger equation first is solved in each part of the proposed structures. Then, the transfer equation is solved for electrons moving in the sub-bands.

The Poisson's relation is defined as follows [32,33]:

$$div(\varepsilon\nabla\psi)=\rho \tag{1}$$

Where ψ is the electrostatic potential, εis the local permittivity and ρ is the local space charge density. The transformation of a real space Hamiltonian, Ho, to a mode space is accomplished by taking a matrix element between m-th an n-th wave functions of k-th and l-th slices as following [33]:

$$H^{MS}mnkl=\left\langle \Psi^{k}m(y)\middle|H_{0}\middle|\Psi^{l}n(y)\right\rangle \tag{2}$$

The quantum transport equations are given as following [33]:

$$\left(E-H^{MS}mnkl-\Sigma_{S}^{R}-\Sigma_{D}^{R}\right)G^{R}=I \tag{3}$$

$$\left(E-H^{MS}mnkl-\Sigma_{S}^{R}-\Sigma_{D}^{R}\right)G^{<}=\left(\Sigma_{S}^{<}+\Sigma_{D}^{<}\right)G^{A} \tag{4}$$

where, E is an electron energy. Σ R is the source or drain self-energies, carrying information about the density of states in the contacts. Σ< is retarded less-than self-energies, carrying information about the Fermi distribution function in the contacts. GR (E) is a retarded Green's function and G< (E) is a less-than Green's function. GA (E) =GR ((E))† is an advanced Green's function. After solving equations (2-4) at each energy, the current and carrier density for the proposed structure will be obtained as following [33]:

$$n(x_i,y_j)=-\frac{i}{L_Z}\sum_{K_Z}\sum_{\sigma mn}\int G^{<}{}_{mnii}(E)\Psi^{i}m(y_i)\Psi^{*i}n(y_j)\frac{dE}{2\pi} \tag{5}$$

$$J_x(x_i,y_j)=-\frac{2e}{hL_Z\Delta_x}\sum_{K_Z}\sum_{\sigma mn}\int \Re e\left(t_{i+1ij}G^{<}{}_{mnii+1}(E)\right)^{<}\Psi^{i}m(y_i)\Psi^{*i+1}n(y_j)\frac{dE}{2\pi} \tag{6}$$

$$J_y(x_i,y_j)=-\frac{2e}{hL_Z\Delta_y}\sum_{K_Z}\sum_{\sigma mn}\int \Re e\left(t_{iij+1}G^{<}{}_{mnii}(E)\right)^{<}\Psi^{i}m(y_j)\Psi^{*i}n(y_{j+1})\frac{dE}{2\pi} \tag{7}$$

$$J=(J_x^2+j_y^2)^{1/2} \tag{8}$$

where, tijkl is an off-diagonal element of real space Hamiltonian Ho, which couples nodes (xi,yk) and (xj,yl).

2. Results and Discussion

Figure 2 depicts the conduction sub-bands of the proposed device at thermal equilibrium condition. The conduction sub-bands do not fully overlap due to the quantum effects along the nanowire diameter.

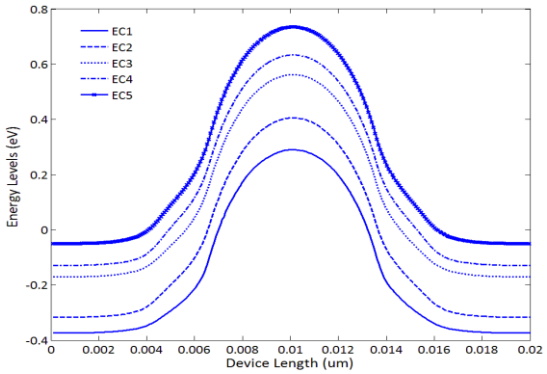


Fig. 2. The conduction sub-bands energy of the proposed device at the thermal equilibrium

Figure 3(a) shows the input characteristic of the proposed device at Vd=0.8V. As can be seen, the current of the device increases with an increasing gate voltage. In fact, as the gate voltage increases, the height of the barrier Potential against the electrons at the source / channel interface decreases. See Figure 4.b. In this case, the injection of electrons from the source into the channel increases and the current flow increases.

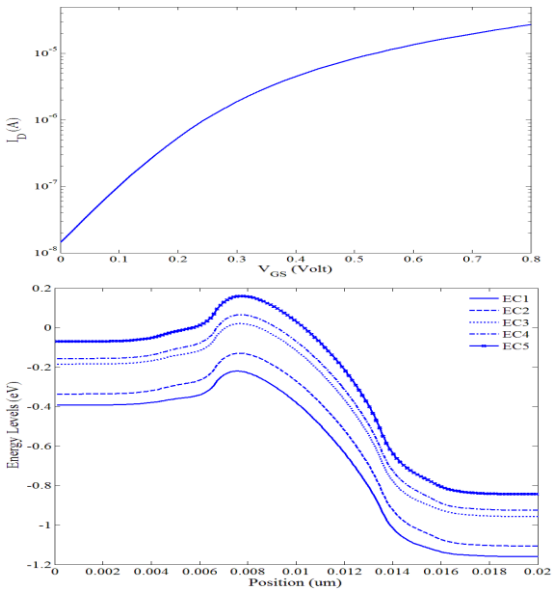


Fig. 3. The ID-VGS curve and The sub bands energy level along the device at the on state

Figure 4 compares the density of electrons along the channel at the cross-section perpendicular to the device channel in the center of the gate for the zero states (VGS = VDS = 0V) and the on state (VGS = VDS = 0.8V). Notes are as follows:

– As can be seen, in the zero states, the electron is depleted below the gate.

– As can be seen, in the on-states, the electron is moving from the center of the nanowire, as a result, the surface scattering of the electron due to the roughness of the interface is reduced.

The main current of a field effect transistor in the upper threshold region. In inversion mode transistor, an inverted layer is formed in the upper area of the threshold at the surface of the device and the movement of electrons from the inverted layer leads to a collision with the interface and reduces mobility. Whereas in the JL- device, threshold voltage is much smaller than the flat band voltage, so in the upper threshold region the electron moves farther away from the surface. As a result, the sensitivity of the device to the vertical field due to the gate voltage is reduced.

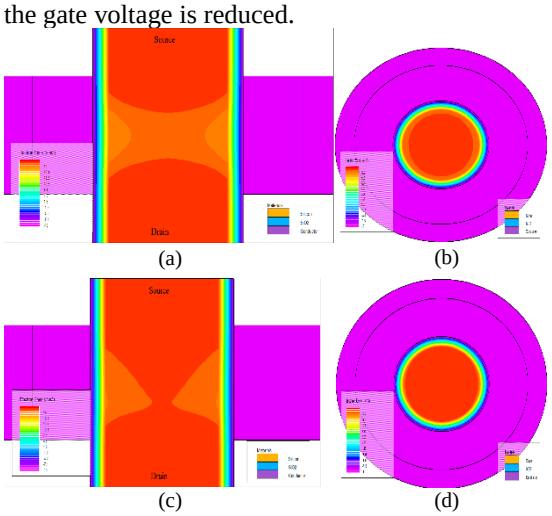


Fig. 4. Electron density (a) and direction of electron motion (b) in the direction perpendicular to the motion of the electron at zero (VGS = VDS = 0V). Electron density (c) and direction of electron motion (d) in the direction perpendicular to the motion of the electron in the on-state (VGS = VDS = 0.8V).

Figure 5 shows the first sub-band of the conduction band energy in the proposed device at the VGS = 0V, for different values of drain voltage. As can be seen, with increasing drain voltage, the height of the potential barrier in front of the electrons is reduced. As a result, the density of electrons in the channel is increased. Therefore, channel conductivity increases, then the off state current increases. This undesirable effect is called drain induced barrier lowering.

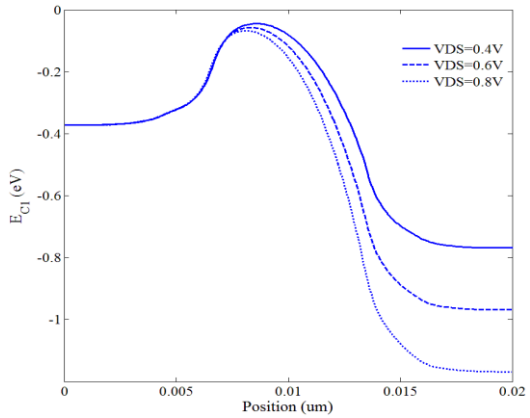


Fig. 5. The first sub-band energy along the channel for differen.00t values of VDS.

Increasing the off state current with increasing drain voltage is undesirable, because the control of the potential barrier against the electron at the source/channel interface is the responsibility of the gate and should not be affected by the drain. To eliminate this adverse effect, the electrostatic control of the gate over the channel must be increased. One way to increase the electrostatic control of the gate over the channel is to reduce the thickness of the gate oxide. If the thickness of the gate oxide decreases, oxide Defeat occurs at high field conditions, and electrons tunnel from the gate to the channel, so the off state current is increased. high-permittivity oxide can be used to increase the electrostatic control of the gate over the channel without reducing the oxide thickness. The use of oxide with a permittivity of K = 7.5, which is equivalent to Si3N4 oxide, has been proposed to improve the electrical characteristics of the device in Figure 1. Figure 6 shows the current-voltage characteristic curve of the proposed device with K = 7.5. As can be seen, the off state current is significantly reduced compared to Figure 4. a

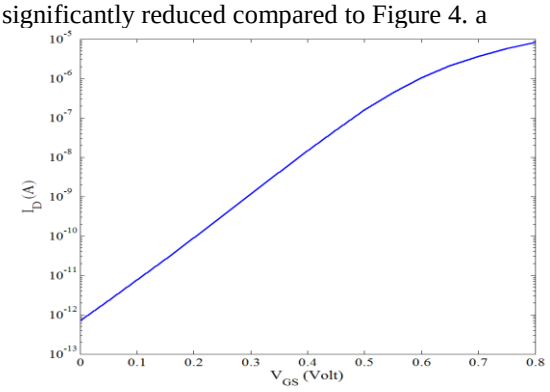


Fig. 6. ID-VGS for K = 75.

figures 7. a and 7. b, show the energy levels for Proposed device at the thermal equilibrium and on state condition respectively. As can be seen, the Potential barrier against electrons at the source/Channel interface for K = 7.5 has increased in thermal equilibrium compared to Figure 3. Therefore, the decrease of the off-state current for K = 7.5 compared to K = 3.9 can be attributed to the increase of the gate electrostatic control over the channel. Comparing Figures 7.b and 3.b, it can be seen that the potential barrier against the electron at the source / channel interface is slightly larger in the device with K = 7.5 than in the device with K = 3.9, which causes slight reduction of the on state current.

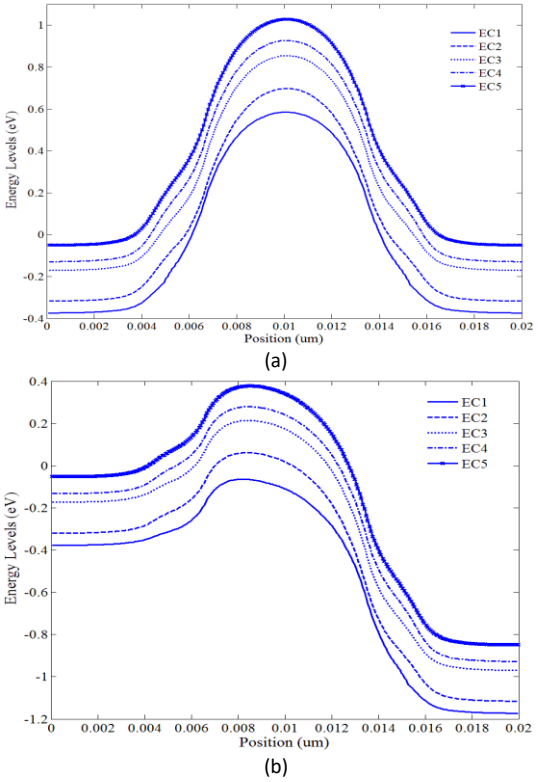


Fig. 7. Energy levels for the proposed device with K = 7.5 in (a) thermal equilibrium condition (VDS = VGS = 0V) and (b) for on state condition (VDS = VGS = 0.8V).

One of the important parameters of JL-transistor for the switching application is called the ratio of on state current to off state current, ION / IOFF. On state current, drain current at VGS = VDS = 0.8V and off state current, drain current at VGS = 0V, VDS = 0.8V are assumed. The simulation results show that for devices with K = 3.9 and K = 7.5, the ION / IOFF parameters are 1.89 × 103 and 1.167 × ×107, respectively. Therefore, the use of Si3N4 instead of SiO2 increases the ION / IOFF ratio four times. To further increase the ION / IOFF ratio, it is proposed to increase the oxide permittivity coefficient. Figure 8 shows the energy levels for the thermal equilibrium condition and the on state condition for K = 21 and K = 29.

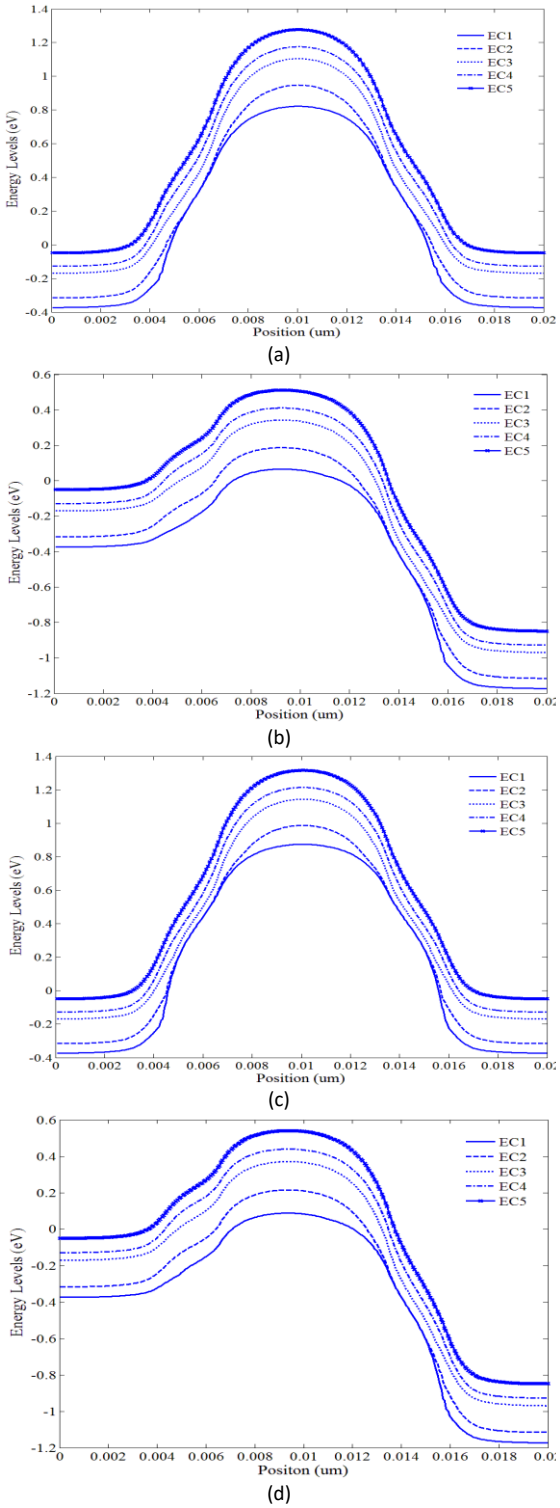


Fig. 8. Energy levels for K = 21 in (a) thermal equilibrium and (b) in the on state and for k = 29 in (c) thermal equilibrium and (d) in the on state.

As can be seen, with increasing K, the energy levels are deformed in the on and the thermal equilibrium state. Figure 9 compares the input charaterstics of the proposed devices for different values of K.

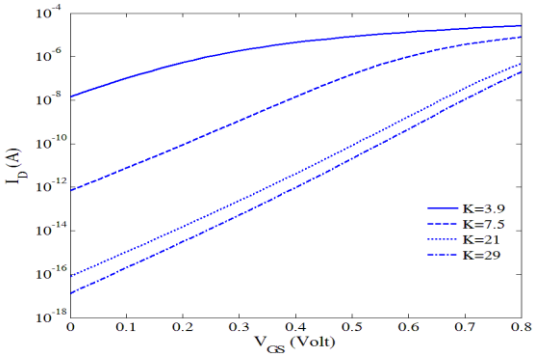


Fig. 9. ID-VGS characteristic for the proposed structure for different values of K

As can be seen, increasing K has significantly reduced the off state current as well as the on state current. The simulation results show that the density of electrons below the first band of the conduction band is much higher than in other sub bands and the current flow can be attributed to the electron transfer below the first band of the conduction band. To investigate the reduction of the off-state current by increasing K, the first sub-band of the conduction band in thermal equilibrium with VGS = VDS = 0V is shown in Figure 10. As can be seen, with increasing K, the height of the potential barrier in the channel has increased. An increase in K causes the surface potential in the channel increased and the electron to be depleted from the electron. In fact, with increasing K, the electrical coupling between the gate and the channel increases, and the off state current decreases. In addition, Figure 10 shows that with increasing K, the barrier width of the electron direct tunneling from the source to the channel increases, which in reduces the off state current. Figure 11 shows the first sub band energy for on state condition with increasing K. As can be seen, with increasing K, the height of the potential barrier against the electron at the source/ channel interface increases. Therefore, the decrease in on state current with increasing K can be attributed to the increase in the barrier potential.

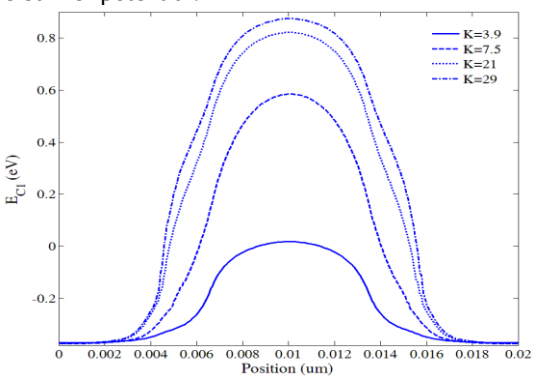


Fig. 10. The first band sub-band energy for the proposed device in thermal equilibrium and different K values.

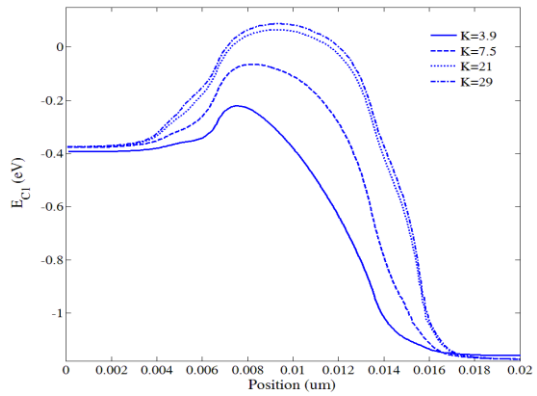


Fig. 11. The first sub-band of the conduction band for the proposed device in the on state for different values of K.

Figure 12 shows the electron density in the on state at the cross-section perpendicular to the current flow in the center of the gate for different values of K. As can be seen, the channel conduction decreases with increasing K.

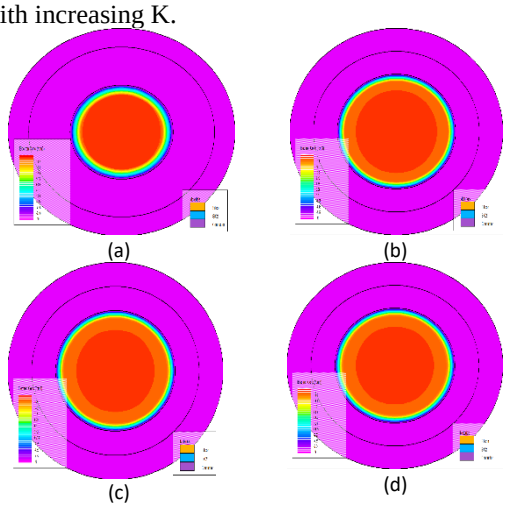
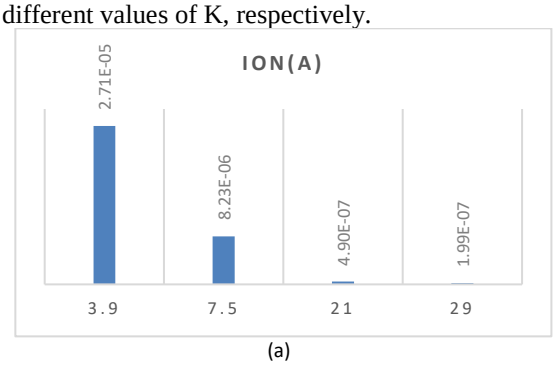


Fig. 12. Electron density in the on state at the cross section perpendicular to the current flow in the center of the gate for the values of (a) K = 3.9, (b) K = 7.5, (c) K = 21 and (d) K = 29.

Reducing the channel conduction by increasing K, on the one hand, means reducing the on state current and on the other hand means reducing the sensitivity of the electron to the gate voltage. Figures 13 (a), (b) and (c) show the on state current, off state current, and ION / IOFF ratio for different values of K, respectively.



(a)

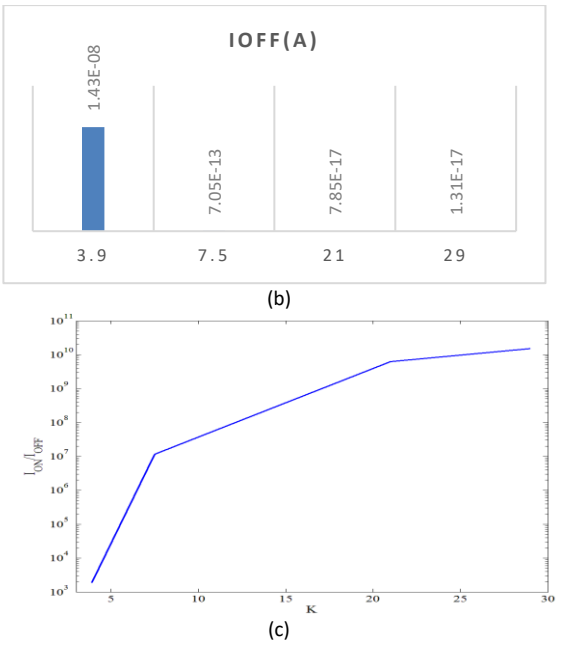


Fig. 13. Current (a) on, (b) off, and (c) On-to-off ratio for different values of K

For K = 7.5, the device has a reasonable off state current, and at the same time, compared to the device with K = 3.9, the on-state current is almost constant. As K increases, the on state current decreases dramatically, so increasing the device latency. Accordingly, K = 7.5 is recommended as the optimal value for the proposed device.

According to the contents stated by selecting K = 7.5, the proposed device has suitable electrical specifications. However, the constant network mismatch between the oxide and the silicon increases with the increasing K, which will cause an unstable oxide with an unsuitable interface. for solving this problem, a new structure has been proposed. In this structure, an oxide layer with a thickness of 0.5 nm is used as a buffer with K = 5.7. On top of the buffer layer, oxide with K = 29 is used to achieve the appropriate electrical characteristics. The proposed structure is called GAA-JL-FET-with-oxide buffer layer. Figure 14 compares the input characteristics of the Proposed device with the device with K = 7.5. In this comparison, the thickness of the oxide with K = 7.5 is equal to 1.5nm.

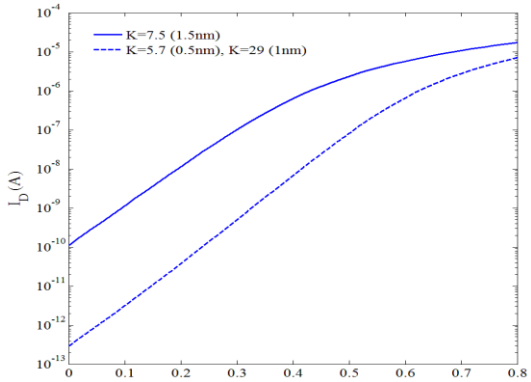


Fig. 14. Input characteristics of the GAA-JL-FET-with-oxide buffer layer

As can be seen, the off state current of the GAA-JL-FET-with-oxide buffer layer has been reduced by about 1000 times compared to the device with K = 7.5. This is due to the increased electrostatic control of the gate over the buffer layer. Figure 15 compares the conduction band energy of devices with K = 5.7, K = 29, and K = 7.5 in the on state. As can be seen, the energy band in the channel for the device with K = 5.7, K = 29 is higher than K = 7.5. Therefore, the electron density in the channel is higher for the device with K = 7.5 and slightly increases the on state current. see Figure 16.

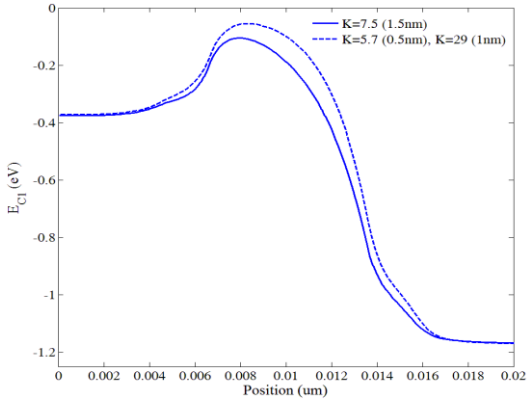


Fig. 15. The conduction band energy in the on state (VGS = VDS = 0.8V).

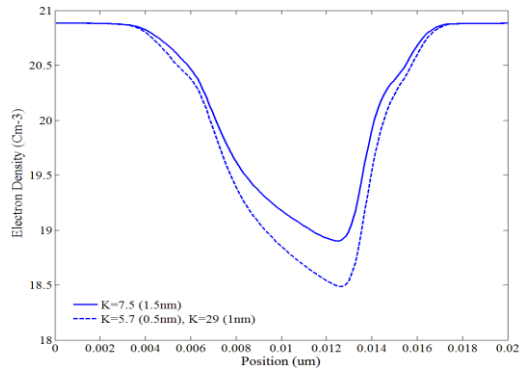


Fig. 16. Electron density along the channel for simulated structure

Due to the significant improvement of the subthreshold parameters of the GAA-JL-FET-with-oxide buffer layer, this device can be a suitable candidate for digital electronics applications.

One of the challenges for the fabrication is the growth of the gate insulator on the silicon semiconductor. Using the atomic layer deposition (ALD), the gate insulator on the silicon semiconductor can be made with acceptable quality [34,35].

3. Designing an interconnection network by the GAA-JL-FET-with-oxide buffer layer

As a major component of NoCs, ICNs have always received researchers' attention. In modern Very Large-Scale Integration (VLSI) circuits, an important part of chip delay and area occupation is due to the connecting links. Therefore, novel techniques for communication in ICNs are highly in demand to increase speed, reduce power consumption, and minimize the chip area. High speed and reduction in consumed power are directly associated with a decrease in the number of links in the system. The use of multiple-valued logic in ICNs has been proposed as a solution for reducing the number of links. This study uses voltage-mode ICNs to allow the simultaneous communication of two processing elements [36-39].

In the following section, two novel architectures are presented to design highly efficient ICNs GAA-JL-FET-with-oxide buffer layer. The mixed-mode tool of Silvaco software is employed to simulate the proposed ICN architecture.

The capacitor can be implemented in VLSI circuits via two methods. The first method is the MIMCAP (Metal-Insulator-Metal Capacitance) technology, which occupies an enormous chip area [39]. The second method, which has been widely considered in the VLSI literature, uses MOS capacitors (MOSCAP) available in the CMOS process technology [40]. Tying the drain and source of a MOSFET together makes a MOSCAP. Gate length determines the size of the MOSCAP. The implementation of the proposed approaches using MOSCAP allows simultaneous communication at different voltage levels.

4. New design based on capacitor with four different voltage levels (DC-1)

The performance of nearly all modern digital systems is limited by interconnection [41]. It seems strange, but designing high-speed low-power arithmetic or logical cells cannot lead to high performance. Today, the main bottleneck is the time and power dissipated in wires [42,43]. This is more apparent when the two processing elements (PEs) try to communicate. No matter the geographical

topology of the network (e.g., off-chip, on-chip, wide range local network, multimedia, or any consumer electronics domain), the main design challenge is still the interconnection [44,46]. Therefore, reducing the number of interconnecting wires may result in higher speed and less power dissipation [46]. Capacitors can be used to implement linear summation as shown in Figure 17. We begin with two coupled capacitors C_{PE1} and C_{PE2} driving a load capacitor C_{load}. For driving the related equations, we use a simple superposition, which is illustrated in Eq. (9). If C_{load} is neglected compared to $C_{PE1}$and C_{PE2}, Eq. (1) is reduced to Eq. (10). Choosing the same value for C_1 and C_2 results in a new equation, as shown below:

$$V_{out}(v_1,v_2)=\frac{C_1}{C_1+C_2+C_{load}}V_1+\frac{C_2}{C_1+C_2+C_{load}}V_2 \quad (9)$$

$$V_{out}(v_1,v_2)=\frac{C_1}{C_1+C_2}V_1+\frac{C_2}{C_1+C_2}V_2 \quad (10)$$

$$V_{out}(v_1,v_2)=\frac{C}{2C}(V_1+V_2)=\frac{V_1+V_2}{2} \quad (11)$$

For realizing an MVL-ICN, we need two voltage levels in PE1 to implement logical 0 and 1 and two higher levels in PE2 to implement logical 0 and 1. Table.1 demonstrates the relationship between silence, logical 0 and logical and voltage levels. The voltage levels of v_{out} are shown in Table.2. This design has the advantage of low static power dissipation, but it suffers from needing four different voltage levels. Besides, the variation of voltage levels is too high. To avoid these problems, this method is improved in the following section.

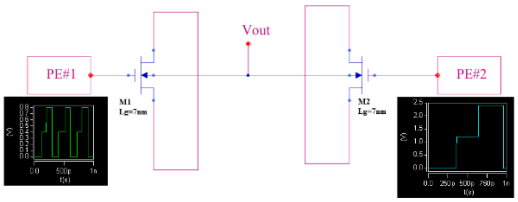


Fig. 17. Connecting two processing elements(DC-1)

Table.1.
Relation between voltage levels in PE1 and PE2

Logical state	*Voltage level of PE1*	*Voltage level of PE2*
S*	0	0
0	1	3
1	2	6

Table.2.
Corresponding voltage of voltage points

Logical state PE2	*Logical state PE1*	*Voltage levels of* V_{out}
S	S	0
S	0	1
S	1	2
0	S	3
0	0	4
0	1	5
1	S	6
1	0	7
1	1	8

5. New design based on capacitor with two different voltage levels (DC-2)

If logical voltages for both PEs are equal in Eq. (12), the following equation must be solved to achieve the proper values of C_1 and C_2. Figure 18 shows the related schematic. Substituting Eq. (13) into Eq. (9) results in:

$$V_{out}(v_1,v_2)=\frac{C_1V_1+C_2V_2}{C_1+C_2}\Big|_{V_2=0}=\frac{1}{3}\times\frac{C_1V_1+C_2V_2}{C_1+C_2}\Big|_{V_1=0} \quad (12)$$

$$V_{out}(v_1,v_2)=\frac{C_1V_1}{C_1+C_2}=\frac{1}{3}\times\frac{C_2V_2}{C_1+C_2} \quad (13)$$

$$C_1=\frac{1}{3}\times C_2 \quad (14)$$

$$C_1=C\rightarrow V_{out}=\frac{C}{C+3C}\times V_1+\frac{3C}{C+3C}\times V_2 \quad (15)$$

$$V_{out}=\frac{V_1}{4}+\frac{3V_2}{4} \quad (16)$$

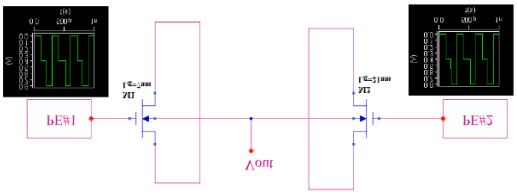


Fig. 18. Connecting the two PEs to the modified capacitors (DC-2)

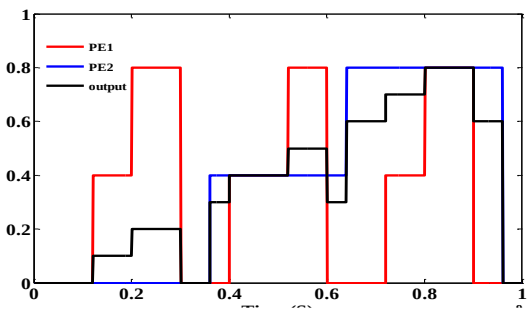
Table.3 illustrates all possible configurations of the interconnection line.

Table.3.
Possible configuration for DC-2 design

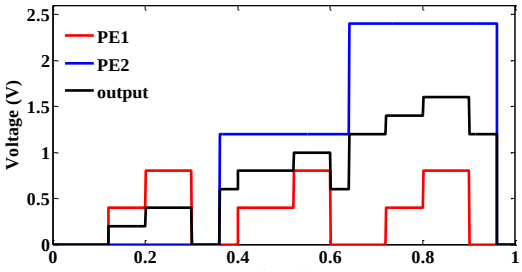
Logical state PE2	*Logical state PE1*	*Voltage levels of* v_{out}
S	S	0
S	0	1/4
S	1	1/2
0	S	3/4
0	0	1
0	1	5/4
1	S	3/2
1	0	7/4
1	1	2

6. Simulation results of DC-1 and DC-2 structures

To simulate the DC-1 and DC-2 structures, the proposed GAA-JL-FET-with-oxide buffer layer is used. Moreover, the mixed-mode module of Silvaco is employed to simulate the proposed structures. Since the capacitors in DC-1 have the same size, the gate length is assumed to be 7 nm in both transistors. In DC-2, the size of one capacitor is three times larger than the other one, so for simulating DC-2, the transistors' gate length is assumed to be 7 and 21 nm, respectively. The simulation results for DC-1 and DC-2 are displayed in Figures 19 (a) and (b), respectively. Evidently, the output values for both structures confirm the predictions made in Eqs. (10) and (15). In fact, by using the proposed designs, PEs can simultaneously communicate, so the speed of communication is twice that of the conventional systems. Moreover, the total system bandwidth is twice larger than convention systems for ICNs. Table 4 presents the maximum delay, consumed power, and power delay product (PDP) for the novel DC-1 and DC-2 designs. From this table, the maximum delay of DC-1 and DC-2 are considerably reduced. As mentioned before, the use of a peripheral gate and a high-permittivity oxide markedly improves the subthreshold parameters and ION/IOFF of the proposed device. This significantly reduces the maximum delay of DC-1 and DC-2. The maximum delay of DC-1 is lower than that of DC-2. In DC-2, the gate length of one of the transistors is three times the gate length of the other transistor. Increasing the gate length increases the travel distance of the electron from the source to the gate. Consequently, as the gate delay increases, the maximum delay of DC-2 increases compared to DC-1. In DC-2, by reducing the voltage levels, the consumed power is reduced by three orders of magnitude compared to DC-1. In fact, DC-2 consumes less power than DC-1; however, since transistors with smaller gate lengths are utilized in DC-1, the maximum delay in DC-1 is less than that in DC-2. The delay in DC-1 is less than in DC-2 and the consumed power is higher in DC-1 than in DC-2. Therefore, by considering PDP, we conclude that DC-2 is more efficient.



(a)



(b)

Fig. 19. Fig. 19 Simulation results in 7 nm process for (a) DC-1 and (b) DC-2

Table.4.
Comparison between the two proposed methods (DC-1 & DC-2) in 7 nm process

Parameters	*Design with four voltage levels (DC-1)*	*Design with two voltage levels (DC-2)*
Max. Delay	$4.235e^{-16}$	$2.1471e^{-14}$
Average Power	$6.214e^{-7}$	$2.3598e^{-10}$
PDP	$2.63e^{-22}$	$5.064e^{-24}$

7. Conclusion

The ION / IOFF ratio is one of the most figure of merit in digital devices. The larger ION / IOFF ratio indicates an increase in transistor switching speed. In this paper, the use of high permittivity oxide is proposed to increase of ION / IOFF ratio. The use of high permittivity oxide increases the electrostatic control of the gate on the channel. The optimum value for K is chosen so that the off state current is minimized and the on state current remains almost intact relative to the device with K = 3.9. The use of high permittivity oxide leads to an undesirable interface with silicon. To prevent this adverse effect, it is proposed to use a buffer oxide layer with K = 5.7 and a thickness of 0.5 nm. In fact, the proposed oxide thickness is 1.5nm, which is a buffer layer with K = 5.7 and a thickness of 0.5nm, and a high K-oxide with K = 29 and a thickness of 1nm. In GAA-JL-FET-with-oxide buffer layer, the ION / IOFF ratio has been improved by about 106 and 102 times compared to the structure with K = 3.9 and K = 7.5, respectively. Two novel architectures were introduced for designing high-efficiency interconnection networks using the GAA-JL-FET-with-oxide buffer layer transistor. The simulation results in mixed mode of Silvaco showed that the average power, max delay and PDP parameters of the proposed interconnection network were significantly improved.

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