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A Modified SOGI-FLL with DC-Offset Rejection Feature for Grid-Connected Single-Phase PV Inverter in Shipboard Power System

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Abstract

By increasing the use of different power electronic devices in the propulsion system and other applications in ships, the shipboard grid voltage may face issues, including dc-offset voltage, variations in voltage, and frequency. When a photovoltaic (PV) generation is utilized in a ship to provide auxiliary or emergency power to inject the current into the grid, the grid voltage needs to be accurately monitored to synchronize the injected current with the grid voltage. Phase-locked loops (PLLs) are responsible for extracting the phase, frequency, and amplitude of the grid voltage in the control unit of a grid-tied inverter. The proper and fast estimation of grid information under grid disturbances has a significant role in the system's stability. In this paper, a phase-lock loop (PLL) algorithm based on a new frequency-lock loop (FLL) structure is proposed. The proposed PLL algorithm has a high-speed performance in estimating the phase, frequency, and amplitude of the grid voltage. Unlike conventional PLL-based FLLs, the phase shift variation in the proposed algorithm is not dependent on the frequency. Moreover, the proposed PLL algorithm doesn't have the drawback of the input DC offset due to using DC offset rejection loop. The proposed approach has been simulated in MATLAB/Simulink environment. The simulation results for variations in voltage frequency, amplitude, and phase have been presented in the paper to confirm the validity of the proposed method.

Keywords: Phase Locked Loop, PV Power, Shipboard Power, SOGI.

1. INTRODUCTION

According to the maritime laws, the energy system should become more efficient so that less pollution is entered into the environment [3]. The shipboard power system is exposed to new developments in the use of different forms of energy resources nowadays, and environmental concerns have also affected

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the use of fossil fuels as the primary energy supplier. Besides, PV systems as a form of clean energy can play an essential role in providing power to be injected into the shipboard power system [6, 7]. The shipboard power system is classified as an islanded alternating current (AC) microgrid (MG) [9]. Hence, like other islanded MGs, the shipboard power system may also confront issues related to the power quality of the system. The propulsion system of the vessel consumes a considerable amount of power, and the power consumption may vary rapidly during the sailing procedures. Consequently, the shipboard grid may encounter high variations in terms of voltage and frequency [12, 13].

According to [15], the variations of grid voltage and the frequency in the shipboard AC power system should be limited in the allowed range of -10% to +6% and -5% to +5%, respectively. It should also be noted that the use of power electronic equipment is increasing day by day. These power electronic devices will bring about various power quality issues in the shipboard AC grid [18], including unbalance between the phases of the voltage and the dc-offset voltage [19, 20]. In case a photovoltaic (PV) generation is employed in a ship to act as the auxiliary or emergency power source to inject the current into the grid, the injected current must be synchronous with the grid voltage [21, 22].
Solar panels produce DC power. Therefore, a power conditioning system is needed to convert the power and inject it into the grid [23, 24]. One of the most crucial parts of the control unit in a power conditioning system is phase-locked loop (PLL). PLLs are responsible for synchronizing the inverter output current with the grid voltage in order to improve power factor value to make it reach unity or nearby unity [25-27].

The structure of conventional phase-locked loops is usually complex, and its dynamic response is also slow. The second-order generalized integrator (SOGI) and second-order generalized integrator frequency-locked loop (SOGI-FLL) were introduced in [2, 28] to address these issues, where SOGI-FLL includes the conventional SOGI and FLL. The SOGI generates the quadrature signals using two integrators and a frequency-locked loop to detect the input signal frequency of the PLL. In [29-32], a central frequency adaptive control structure for SOGI block based on quadrature signals generator (SOGI-QSG) has been proposed. However, in a similar approach that is proposed in [21], no feedback signal has been applied in the output of the PLL. In [33], the tracking accuracy and speed of the PLL has been investigated in FFSOGI structure has been proposed based on the trade-off between the accuracy and the speed of the grid monitoring. In [34], two SOGI-FLL-WPF and SOGI-FLL-WIF have been proposed to reject the grid harmonics, which is a troubling issue in SOGI. However, these structures are complex. The frequency estimation can also be realized by incorporating FLL and SOGI-QSG. In this method, the estimated frequency can empower SOGI to achieve a more satisfying performance in synchronizing the inverter current with the grid voltage. However, the FLL algorithm increases the dependency of PLL input variations to the estimated frequency, and the phase error directly enters the frequency-locked loop that leads to

distraction of the estimated frequency value. In [35], SOGI-FLL grid frequency monitoring has been proposed to perform well in grid voltage variations, but it does not have the DC-offset rejection feature.

The main drawback of SOGI and SOGI-FLL is that they cannot eliminate the DC offset [36, 37]. A hybrid filtering-based PLL technique has been investigated in [38] to block DC-offset voltage. A fixed-parameter PLL structure with a systematic design procedure of cascaded generalized integrator PLL has been proposed in [39] to tackle the DC offset problem. A Phase-lead compensator has been applied in the proposed technique in [40] to overcome the DC offset issue. In [41], two SOGI are connected in series in order to tackle the DC-offset issue. General DC offset rejection techniques in PLLs have been investigated and compared in [42, 43]. More complex concepts like Fuzzy can also be employed in the PLL design [44-46]. However, these methods require a lot of computational efforts in terms of experimental implementation. As tracking speed is a major priority in the performance of the PLLs, the computational time should be reduced as much as it is possible. In [47], it has been shown that the phase and frequency estimation speed are decreased by adding the DC rejection loop. In [16], the new structure of the DC rejection filter is proposed. The main disadvantages of this method are mathematical complexity and dependency on the operating points. Hence, this technique needs to be modified for further simplification. In [48], the auxiliary loop is added to the PLL system, and the DC offset effect is eliminated in the estimated frequency.

In the proposed approach, a modified SOGI-FLL structure has been presented. This structure has decreased the transient time of the frequency detection by using an adaptive method. As a result, the variation in the input of the PLL is no longer dependent on frequency detection. Thus, the dynamic response of the PLL has been enhanced. Moreover, the oscillation problem caused by

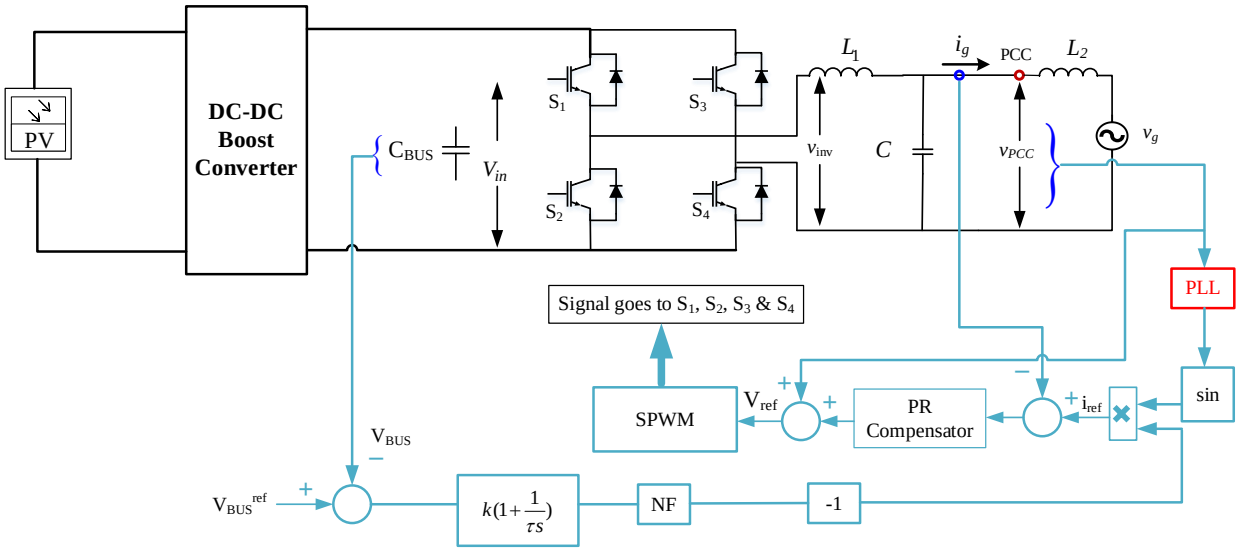

Fig. 1. PLL in grid-connected single-phase PV inverter in shipboard network.

the DC offset in the phase and frequency detection has also been compensated by adding the DC offset rejection loop in the proposed PLL and SOGI-FLL. The proposed approach aims at addressing multiple issues at once, while the previous works were only focusing on improving limited features of the PLL.

This paper is organized as follows: SOGI-PLL and its performance are analyzed in section 2. In section 3, a frequency-locked loop is investigated and designed. The design procedure of the proposed SOGI-PLL is presented in Section 4. The DC offset rejection loop structure is presented in section 5. Section 6 covers the simulation results. Finally, section 7 concludes the paper.

2. SOGI-PLL ANALYSIS

2.1. Review Stage

As shown in Fig. 1, the PLL is employed in grid-connected PV as a power source to inject power into the shipboard power grid. The PLL unit synchronizes the injected current into the grid (i_g) with the shipboard grid voltage (v_g). The PLL plays a critical role, as it helps to generate the current reference waveform (i_{ref}). The grid current and the grid voltage are sampled at the point of common coupling (PCC). The sampled voltage signal goes into the PLL block, and the PLL generates phase and frequency according to the sampled voltage signal.

Fig. 2 indicates a PLL based on the second-order generalized integrator (SOGI) [29]. Where v_i is the input signal and $\hat{\omega}$ and $\hat{\theta}$ ($\hat{\theta} = \hat{\omega}t + \hat{\varphi}$) represent the estimated frequency and phase angle, respectively. In addition, ω_{ff} indicates the nominal frequency [47].

The SOGI block diagram is demonstrated in Fig. 3, and Equ. (1) is the transfer matrix (dq frame).

$$T = \begin{pmatrix} \cos\hat{\theta} & \sin\hat{\theta} \\ -\sin\hat{\theta} & \cos\hat{\theta} \end{pmatrix} \quad (1)$$

Equs. (2)-(3) are the transfer functions of the SOGI block output α and β voltages to the input voltage (v_i).

$$G_\alpha(s) = \frac{v_\alpha(s)}{v_i(s)} = \frac{k\hat{\omega}s}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \quad (2)$$

$$G_\beta(s) = \frac{v_\beta(s)}{v_i(s)} = \frac{k\hat{\omega}^2}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \quad (3)$$

where k (damping coefficient) is a constant value [28].

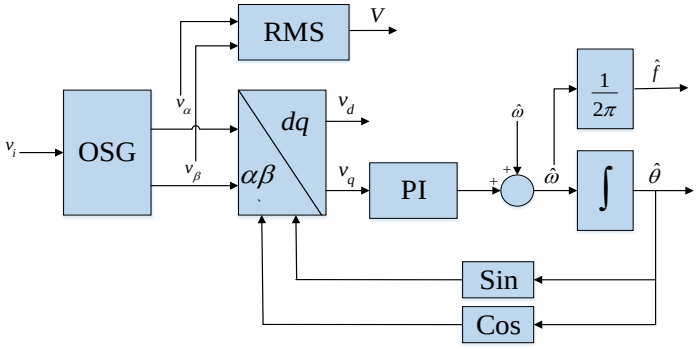

Fig. 2. Schematic diagram of SOGI-PLL.

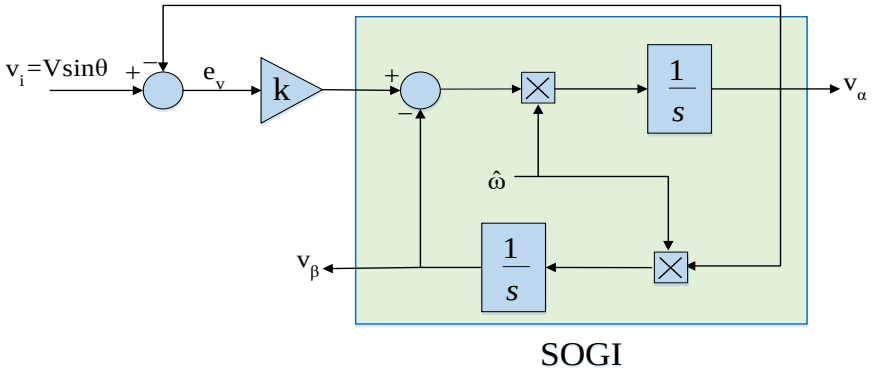

Fig. 3. Second-order generalized integrator (SOGI).

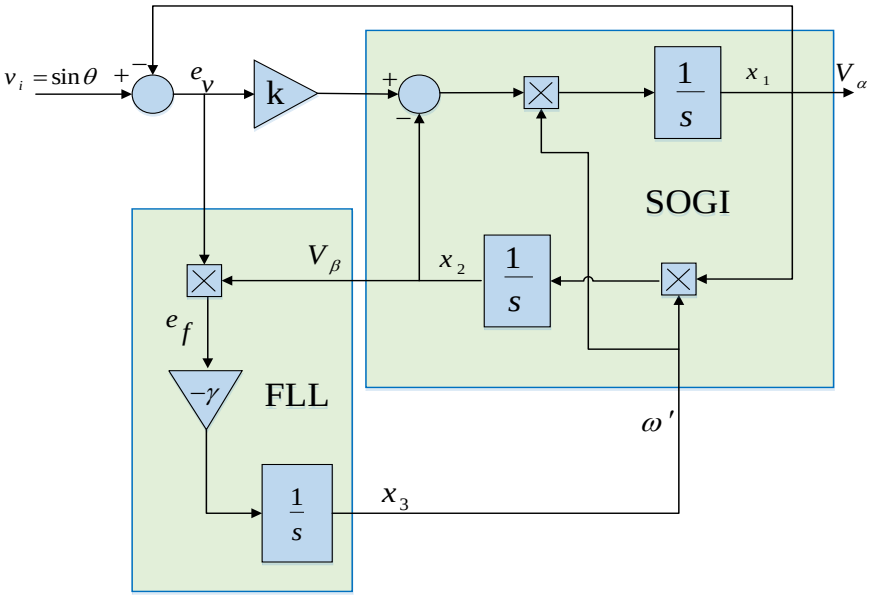

Fig.4. SOGI-FLL, a single-phase grid synchronization.

According to [2], G_α is a band-pass filter whose center frequency is represented by $\hat{\omega}$. The bandwidth of the band-pass filter is limited by k. k improves the grid harmonics filtering capability of the PLL performance. Assuming G_α as the transfer function of v_α to v_i and $\omega = \hat{\omega}$, v_α will equal v_i in terms of the phase angle and amplitude after the transient state. Considering that the transfer function of v_β to v_i is G_β (which is a low-pass filter), and also assuming $\omega = \hat{\omega}$, v_β will equal v_i in terms of the amplitude in the steady-state. However, the phase angle of $v_\beta$will be 90 degrees lead from the phase angle of v_i (since $G_\alpha/G_\beta = s/\hat{\omega}$). Consequently, due to the phase difference of 90 degrees between v_α and v_β, sinusoidal orthogonal signals are generated (quadrature signal generation) [7]. SOGI-PLL structure is used for the proposed PLL. The basic construction of the SOGI-PLL is designed according to [1, 49].

3. ANALYSIS AND DESIGN OF THE FREQUENCY-LOCKED LOOP

As depicted in Fig. 4, the frequency-lock loop has been added to the SOGI structure [31]. According to [21] and Fig. 4, Equ. (4) indicates the average of the frequency error.

$$< e_f > \approx -\frac{\Delta\omega}{k\omega} \tag{4}$$

where $< e_f >$ refers to the average value of e_f. $\Delta\omega$ in Equ. (4) is defined as follows:

$$\Delta\omega = \omega - \hat{\omega} \tag{5}$$

The performance of the loop can be investigated using Fig. 4. When the estimated frequency surpasses the input frequency ($\hat{\omega} < \omega$), $-\gamma \times \bar{e_f}$ would be negative because the frequency error is positive, and $-\gamma$ is negative in this condition. This negative phrase reduces the frequency $\hat{\omega}$ as it passes the integrator. The reduction in the value of $\hat{\omega}$ continues until the estimated frequency equals the input frequency ($\omega = \hat{\omega}$). At this moment, according to Equ. (4), both the frequency error average and the multiplication of $-\gamma \times \bar{e_f}$ will equal to zero. Thus, thanks to the FLL structure (that is depicted in Fig. 4), $\hat{\omega}$ does not change.

When the estimated frequency is less than the input frequency ($\omega > \hat{\omega}$), $-\gamma \times \bar{e_f}$ will be positive due to the negative value of the frequency error in $\omega > \hat{\omega}$ and the negative value of $-\gamma$. This positive phrase increases $\hat{\omega}$ due to the presence of the integrator in the forward path. The increase in $\hat{\omega}$ continues until the estimated frequency will equal to the input frequency ($\omega = \hat{\omega}$). At this time, both the frequency error average and the multiplication of $-\gamma \times \bar{e_f}$ will be 0 according to Equ. (4). Therefore, the value of $\hat{\omega}$ does not change due to the FLL structure of Fig. 4 [2]. Since the frequency adaptive loop is significantly non-linear, it is not possible to directly apply linear methods to determine the value of γ in the FLL in the SOGI-FLL structure. In this part, the linear model of the FLL can be achieved by considering the definition of the local stability and equations averaging. This linear model, which is derived from [28], is demonstrated in Fig. 5.

The transfer function of the frequency adaptive loop is expressed in Equ. (6)

$$\frac{\hat{\hat{\omega}}}{\omega} = \frac{\Gamma}{s+\Gamma} \tag{6}$$

Thus, the settling time (frequency loop speed) depends only on Γ. The settling time almost equals Equ. (7).

$$t_s(FLL) \approx \frac{5}{\Gamma} \tag{7}$$

According to Equ. (7), Γ can be derived in Equ. (8).

$$\Gamma = \frac{\gamma V^2}{k\hat{\omega}} \tag{8}$$

Thus, Equ. (7) can be rewritten as Equ. (9).

$$t_s(FLL) \approx \frac{5}{\Gamma} = \frac{5k\hat{\omega}}{\gamma V^2} \tag{9}$$

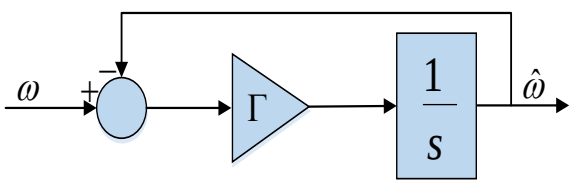

Fig. 5. Normalized FLL block diagram.

4. PROPOSED SOGI-FLL

According to section II, the frequency-lock loop is another method for frequency estimation. In the FLL, the estimation is performed using the quadrature signal generator. Hence, FLL is faster in comparison with the standard SOGI-PLL. However, this method increases the dependency of the estimated frequency on the variations of the PLL input due to the existence of the FLL in the PLL input. The phase error enters the frequency-lock loop directly and disturbs the estimated frequency value. The FLL control signal (e_f) should be limited during the phase jump to minimize the phase error impact on the estimated frequency to tackle this problem. For example, when the input phase changes, the error signal is no longer zero ($e_f \neq 0$) and it is like what is depicted in Fig. 6. This frequency error is caused by the multiplication of the voltage error and v_β that enters the frequency-adaptive loop.

The estimated frequency by the frequency lock-loop can be observed in Fig. 7. As demonstrated in this Fig. 7, the phase changes from 0 to 45 degrees at $t = 0.1\ s$, which causes a considerable transient state in the frequency estimation. The estimation of frequency variation amplitude within the transient state is 13 Hz, and the transient time is 0.052 s.

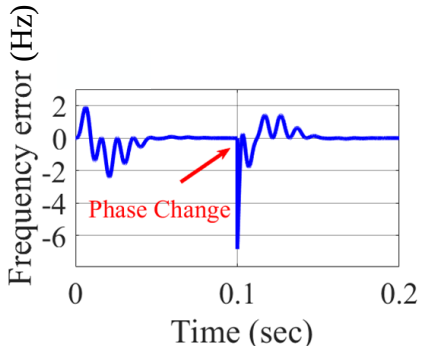

Fig. 6. Frequency error of signal in phase.

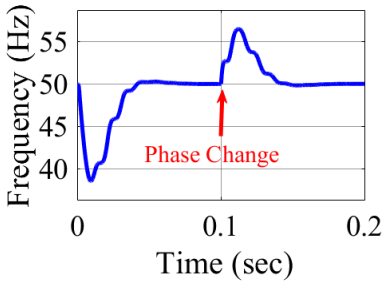

Fig.7. Phase change dependence to frequency estimation analysis in standard SOGI-FLL.

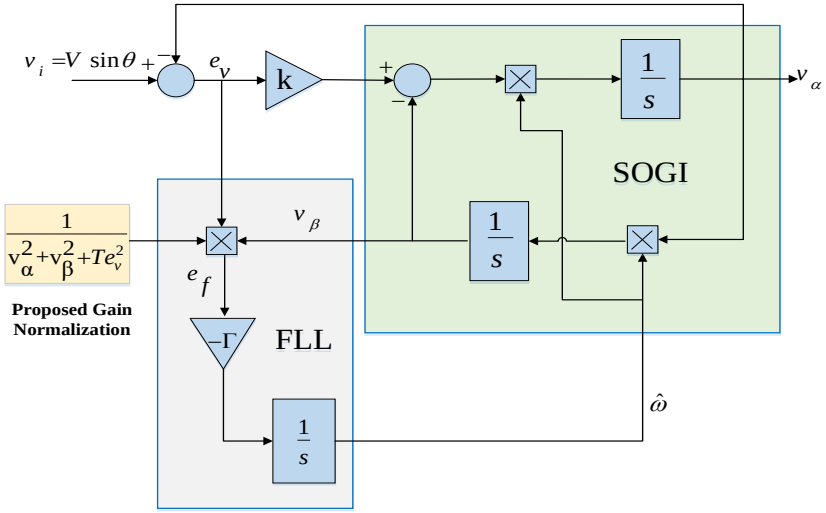

Fig 8. Primary proposed SOGI-FLL.

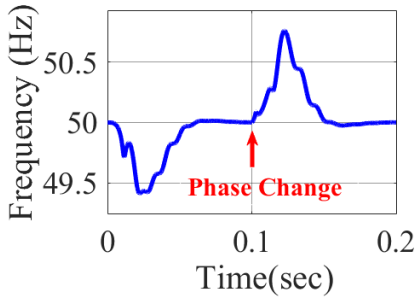

Fig. 9. Phase change dependence to frequency estimation analysis in proposed SOGI-FLL.

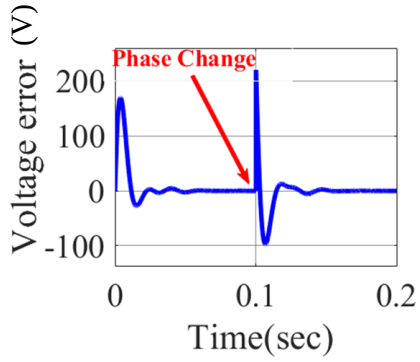

Fig. 10. Voltage error caused by phase variations waveform.

A structure is suggested in Fig. 8 to solve this problem. In this structure, Te^2 is added to the denominator of $\frac{1}{v_\alpha^2+v_\beta^2}$. In other words, instead of multiplying e_f by $\frac{1}{v_\alpha^2+v_\beta^2}$ in the FLL's input (as it is depicted in Fig. 4), e_f is multiplied by $\frac{1}{v_\alpha^2+v_\beta^2+Te_v^2}$ (as it is shown in Fig. 8).

The dependency of the phase jump to the estimated frequency decreases when a jump happens in the input phase. This jump causes the voltage error (e_v) and subsequently, the frequency error (e_f). Applying $\frac{1}{v_\alpha^2+v_\beta^2+Te_v^2}$ instead of $\frac{1}{v_\alpha^2+v_\beta^2}$ in the proposed structure leads to more reduction. Hence, when there is a jump in the phase of the grid voltage, the frequency-lock loop will be affected less. The transient state caused by the jump in the input signal phase can be eliminated considerably in the frequency estimation by choosing a large T. The resulted estimated frequency by applying the proposed FLL is shown in Fig. 9. As depicted in Fig. 9, the phase jump from 0 to 45 degrees occurs at $t = 0.1\,s$. This phase jump does not lead to a transient state in the frequency estimation (unlike the standard SOGI-FLL in Fig. 3). In the proposed structure, the frequency variation in the transient state is less than 0.6 Hz, and the transient state duration (settling time) is 0, as shown in Fig. 9.

Adding Te_v^2 in $\frac{1}{v_\alpha^2+v_\beta^2+Te_v^2}$ does not affect the steady state of the system because, as depicted in Fig. 10, the value of e_v will be zero after the transient state. As a result, the value of Te_v^2 will be zero in the steady-state.

4.1. Selecting T

The simulated diagrams for the frequency estimation of the PLL and input phase jumps are like Figs. 11 and 12 to choose among a variety of T input phase jumps values, respectively. As shown in Fig. 11 there is no significant change in the settling time of the estimated frequency (no dependency) for $T > 100$. Fig. 13 shows the estimated frequencies diagram in a variety of T values. As depicted in Fig. 13, the rise of T value increases the PLL speed. However, for $T > 100$, the PLL speed will only enhance slightly. Therefore, $T = 100$ is chosen.

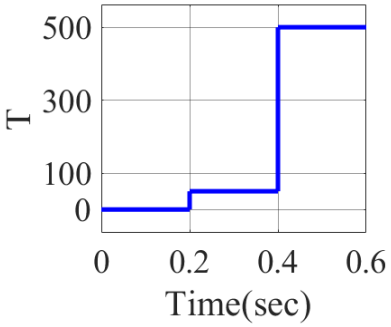

Fig. 11. Different given T values used in Simulink with regard to time period.

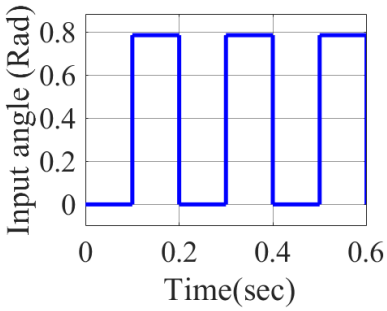

Fig. 12. Given PLL input phase jumps with regard to time period.

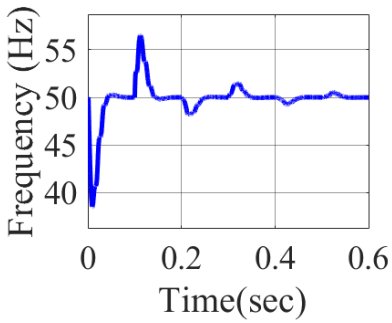

Fig. 13. Estimated frequencies for different T.

4.2. The Effect of T On Dynamic Response Analysis

It can be proved that the increase in the value of T reduces the settling time. Hence, the input signal v_i is assumed $V\cos(\omega t)$. In the steady state, $v_\alpha = V\cos(\omega t)$ and $v_\beta = V\sin(\omega t)$. A change in the value of ϕ changes the PLL input signal into $V\cos(\omega t + \phi)$. However, at the first moments, v_α and v_β do not follow the input phase change. Therefore, they still remain at their previous values. As shown in Fig. 7, the value of e_f at the first moment can be obtained by applying Equ. (10).

$$e_f = v_\beta \times e_v = (V\sin(\omega t)) \times (v_i - v_\alpha) \quad (10)$$

By substituting the input signal (v_i) with $V\cos(\omega t + \phi)$ and v_α with $V\cos(\omega t)$ in (1), Equ. (11) can be achieved.

$$e_f = (V\sin(\omega t)) \times (V\cos(\omega t + \phi) - V\cos(\omega t)) \quad (11)$$

By applying simplification and averaging in the two sides of Equ. (11), Equ. (12)) can be obtained as follows:

$$\bar{e}_f = -\frac{1}{2}\sin\phi \quad (12))$$

As e_f is multiplied by $\frac{1}{v_\alpha^2+v_\beta^2+Te_v^2}$ and taking account of Equ. (12)) and Fig. 7, the FLL integrator input is derived as follows:

$$\frac{1}{v_\alpha{}^2 + v_\beta{}^2 + \mathrm{T}e_v{}^2} \times -\frac{1}{2}\sin\phi \times -\Gamma \quad (13)$$

According to Equ. (13), by adding Te_v^2 to the denominator of $\frac{1}{v_\alpha^2+v_\beta^2}$, the input of the FLL integrator is reduced. This reduction leads to a decrease in the value of $\hat{\omega}$. Hence, according to Equ. (13), a reduction in the value of $\hat{\omega}$ decreases the settling time. Subsequently, adding the Te_v^2 factor to the denominator of $\frac{1}{v_\alpha^2+v_\beta^2}$ enhances the dynamic response of the PLL.

5. DC OFFSET REJECTION IN PROPOSED PHASE LOCK LOOP

The existence of the DC offset in the PLLs input is one of the major challenges that leads to the oscillation in the estimated frequency and phase angle. The DC offset can be generated by various factors such as the voltage sensor, analog to digital converter (ADC), the mismatch between semiconductor components, and distorted shipboard power grid. One of the drawbacks of the phase-lock loops that use SOGI and SOGI-FLL structures and the proposed SOGI-FLL is the lack of the DC offset rejection capability. In [42], general methods for the DC offset rejection have been surveyed. In this section, a method for the proposed SOGI-FLL is presented in order to reject the DC offset, as demonstrated in Fig. 14. According to the bode diagram in [20], the filtering capability of $\frac{v_\beta}{v_i}(s)$ is better than $\frac{v_\alpha}{v_i}(s)$. However, the value of $\frac{v_\beta}{v_i}(s)$ equals Equ. (14) at $\omega = 0$.

$$\frac{v_\beta}{v_i}(j0) = 1 \tag{14}$$

It can be inferred from (14) that the generated signal (v_β), which is perpendicular to the input signal, has the DC offset. Thus, if the input signal includes the DC offset, the second-order generalized integrator cannot reject it. According to [42], using the modified integrator is one of the typical methods to reject the DC offset. By adding the DC offset rejection loop to the proposed structure, the structure in Fig. 14 is achieved. Adding the DC rejection loop, as depicted in Fig. 14, leads to the DC offset estimation by the third integrator and the gain of $k_0\omega$. Finally, this estimated value is subtracted from the input signal to reject the DC offset [50].

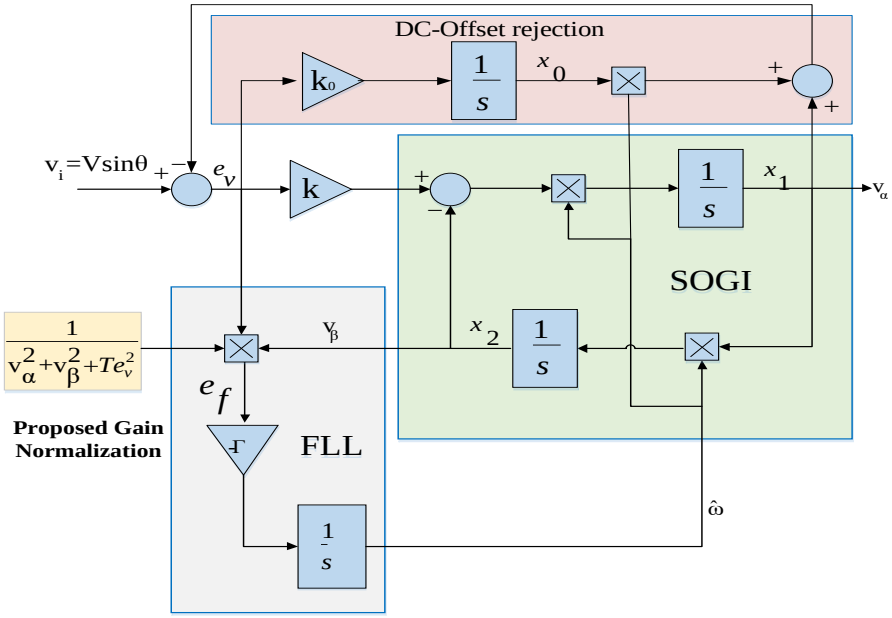

Fig. 14. Proposed SOGI-FLL with DC offset rejection loop.

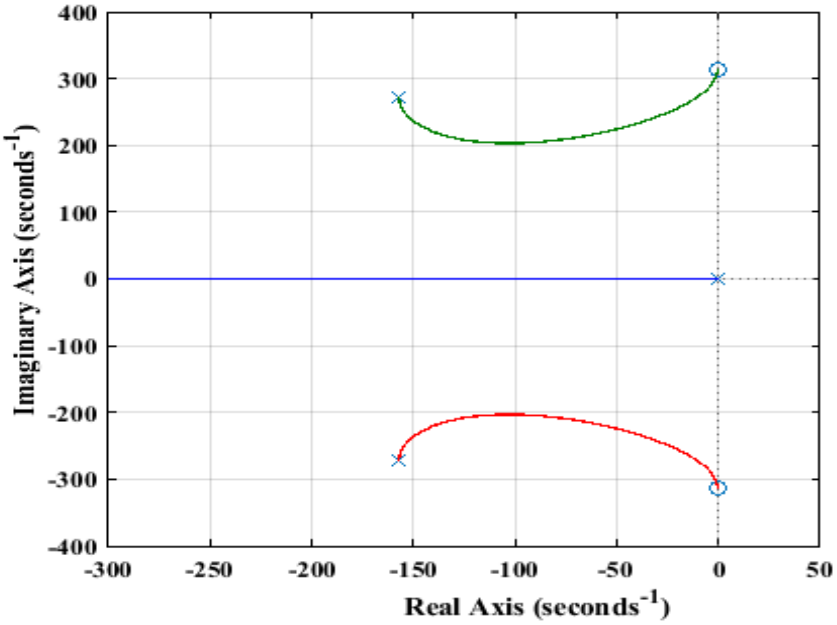

Fig. 15. $\Delta(s)$ ***root locus for*** $\Delta(s)$.

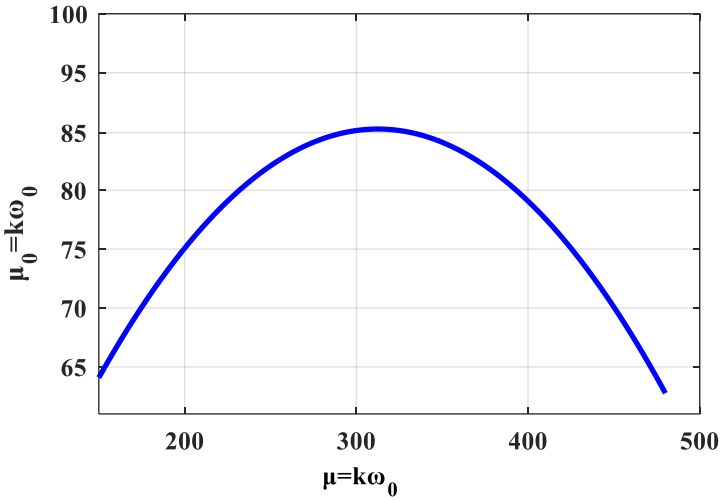

Fig. 16. Relation between $k_0\omega_0$ ***and*** $k\omega_0$.

Equs. (15)-(17) express the transfer functions of the new structure. Assuming that $\Delta(s) = s^3 + (k + k_0)\omega_0 s^2 + \omega_0^2 s + k_0\omega_0^2$, at the main frequency ($\omega = \omega_0$), $\Delta(j\omega_0) = -k\omega_0^3$. Thus, it can be explained that x_1 is an input signal band-pass filtered sample, x_2 is an input signal band-pass filtered sample with 90 degrees phase shift, and x_0 is the input low-pass filtered notch sample. Therefore, it can be concluded that neither x_1 nor x_2 carry the DC component of the input signal, whereas x_0 equals the input signal DC component [14, 50].

$$\frac{x_1(s)}{v_i(s)} = \frac{k\omega_0 s^2}{s^3 + (k + k_0)\omega_0 s^2 + \omega_0^2 s + k_0\omega_0^2} \quad (15)$$

$$\frac{x_2(s)}{v_i(s)} = \frac{k_0\omega_0^2 s}{s^3 + (k+k_0)\omega_0 s^2 + \omega_0^2 s + k_0\omega_0^3} \quad (16)$$

$$\frac{x_0(s)}{v_i(s)} = \frac{k_0\omega_0(s^2+\omega_0^2)}{s^3 + (k+k_0)\omega_0 s^2 + \omega_0^2 s + k_0\omega_0^3} \quad (17)$$

In this section, different values of k_0 is used for $\Delta(s)$ root locus plotting. The root locus for $\Delta(s)$ is plotted for $k = 2.1$ in Fig. 15. For smaller values of k_0, the DC value is estimated slower, while the larger values of k_0 result in oscillations in the orthogonal signals [51]. Thus, this trade-off should be dealt. Assuming all three roots of the characteristic equation have the same real values, the characteristic equation can be rewritten as Equ. (18).

Therefore, k_0 should be applied in (19). Fig. 16 shows the relationship between k_0 and k. The parameters are selected as $k = 2.1$ and $k_0 = 0.4$.

$$s^3 + (k+k_0)\omega_0 s^2 + \omega_0^2 s + k_0\omega_0^3 = (s+\alpha)(s+\alpha+j\beta)(s+\alpha-j\beta) \quad (18)$$

$$k_0^3 + 3kk_0^2 + (3k^2+9)k_0 + k^3 - 4.5k = 0 \quad (19)$$

6. SIMULATION RESULTS

In this section, various simulations have been conducted to investigate the performance of the proposed approach in different conditions. $v_i = 311\sin(100\pi t)$ is assumed as the input of the PLL, which is based on the proposed SOGI-FLL. Fig. 17 represents the value of the estimated frequency. In this Figure, the settling time for the frequency estimation is $0.023\ s$. The settling time has improved noticeably in comparison with the conventional SOGI-PLL and the PLL structure that is based on the SOGI-FLL. Subsequently, as depicted in Fig. 17, when a step phase-jump from 0 to 45 degrees is applied to the PLL input at $t = 0.1\ s$, there will be a transient state at $t = 0.1\ s$ in the estimated frequency diagram. This scenario has been applied to analyze the performance of the proposed approach in a probable distorted shipboard grid. The transient state time (settling time) for this phase jump is 0.024 seconds, which is a short time duration.

The estimated amplitude by the proposed PLL structure is demonstrated in Fig. 18 ($v_i = 311\sin(100\pi t)$). As depicted in Fig. 18, the settling time of the amplitude is 0.014 seconds. This time period is significantly improved compared to the conventional SOGI-PLL and PLL structure that is based on the SOGI-FLL structure.

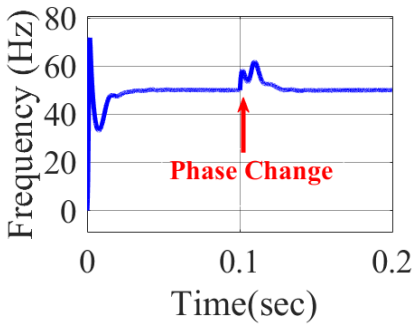

Fig. 17. Transient state of estimated frequency for the proposed PLL based on SOGI-FLL.

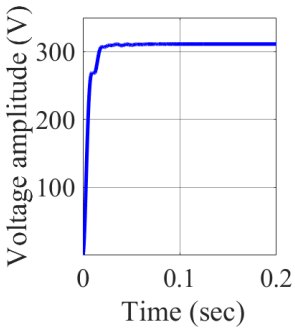

Fig. 18. Estimated amplitude by the proposed PLL based on SOGI-FLL.

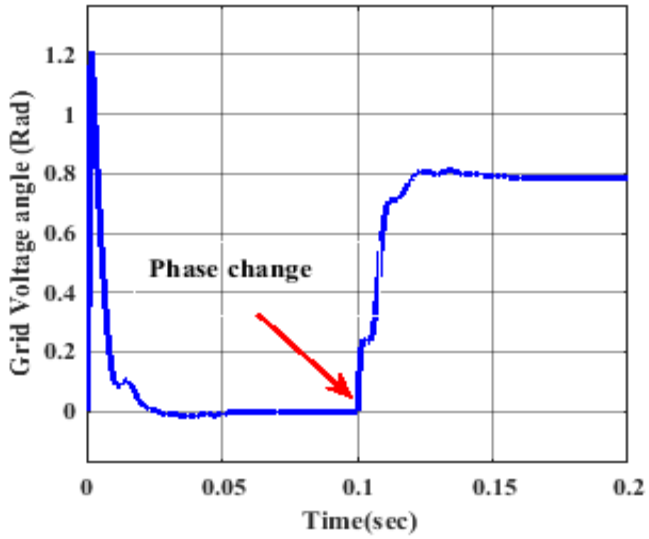

Fig. 19. Transient state of phase estimation caused by the step phase jump in the proposed PLL based on SOGI-FLL.

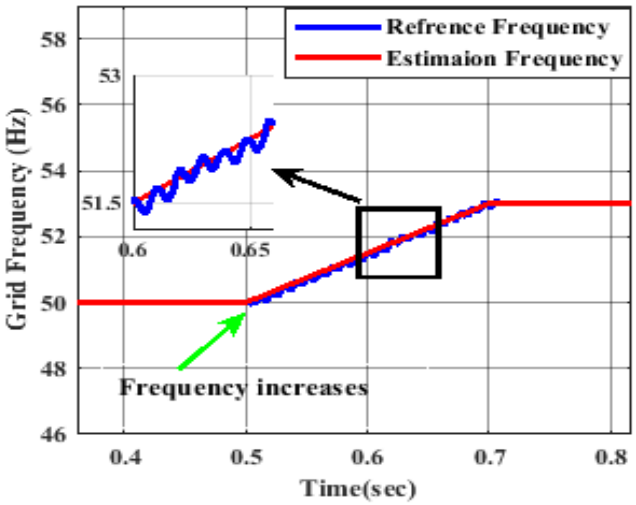

Fig. 20. Ramp frequency jump effect on estimated frequency diagram in the proposed PLL based on SOGI-FLL.

When a phase jump from 0 to 45 degrees occurs at $t = 0.1\ s$ for the proposed PLL, which is based on SOGI-FLL structure, a transient state will happen in the estimated phase at $t = 0.1\ s$ as demonstrated in Fig. 19. This transient state in the frequency estimation lasts for 0.011 seconds (the settling time is 0.011 seconds). This time has been improved significantly in comparison with the conventional SOGI-PLL and the PLL based on the SOGI-FLL structure.

When a ramp frequency jump of 50Hz to 53Hz occurs in the PLL input at $t = 0.5\ s$ (the red diagram in Fig. 5), the estimated frequency would be just like the blue diagram in Fig. 20 for the PLL based on the SOGI-FLL structure.

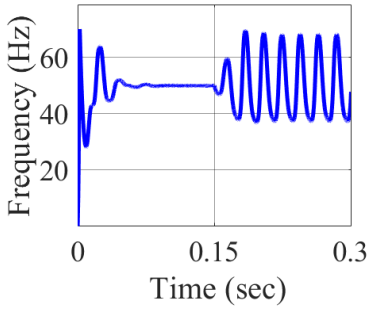

Fig. 21. DC offset effect on PLL without DC offset rejection loop.

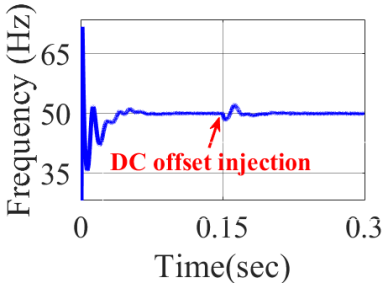

Fig. 22. DC offset effect on PLL with DC offset rejection loop (the time at which the DC offset is injected, is 0.15s).

As shown in Fig. 21, the existence of the DC offset in the input of PLLs is one of the main challenges that causes the oscillation in the estimated frequency and phase. Finally, as depicted in Fig. 22, these oscillations (which are caused by the DC offset) are eliminated by applying the proposed structure in Fig. 14.

According to the abovementioned simulation results, the proposed approach has been successful in dealing with voltage swings, and it presented a satisfactory performance in estimating the frequency, amplitude, and phase of the grid voltage. Besides, Table 1 compares the proposed approach with similar works in different aspects and provides a better understanding of the effectiveness of the proposed PLL.

Table 1. ***Comparison between proposed modified approach and basic structures.***

structures	frequency prediction settling time (s)	phase prediction settling time (s)	Dependency of the phase variation on frequency variation	DC offset rejection capability
proposed in [1]	0.052 s	0.054	depended	no
proposed in [2]	0.045 s	0.046	depended	no
proposed in [4]	0.081s	0.084s	not depended	yes
proposed in [5]	0.084s	0.087s	not depended	yes
proposed in [8]	0.075s	0.078s	not depended	yes
proposed in [10]	0.023s	0.024s	not depended	yes
proposed in [11]	0.1s	0.1s	not depended	yes
proposed in [14]	0.03s	0.03s	not depended	yes
proposed in [16]	0.020s	0.020s	not depended	yes
proposed in [17]	0.06s	0.06s	not depended	yes
proposed modified PLL	0.023 s	0.024 s	not depended	yes

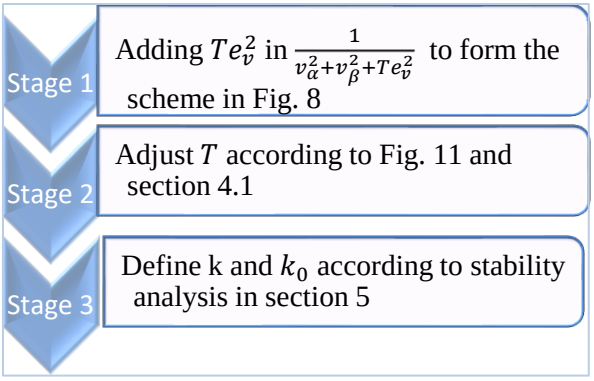

Fig. 23. Design process of the proposed scheme.

In addition, a flowchart has been provided to summarize the design process of the proposed approach. This flowchart has been demonstrated in Fig. 23.

7. CONCLUSION

The Phase-Locked Loop (PLL) structures play an important role in generating the reference waveform to inject current into the shipboard power grid. Due to the importance of high-quality filtering and fast dynamic response in the shipboard power system, SOGI-PLL structure was chosen in this study. The PLL structures, which are based on SOGI-FLL structures, have the advantage of better speed in comparison with SOGI-PLLs. However, they increase the dependency of the phase change to the estimated frequency. The proposed structure is employed to eliminate this dependency, raise the phase and frequency lock loop speed, and provide the DC-offset rejection capability. In addition, the offset rejection part is added to the PLL in order to avoid input DC offset. The final scheme is the proposed PLL plus the DC offset rejection loop. Adding this loop eliminates the persistent oscillation due to the DC offset. The tracking performance of the proposed PLL approach have been proven to be suitable even in a distorted grid voltage through different simulations.

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