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New Fault-Tolerant Majority Gate for Quantum Dots Cellular Automata

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Abstract
In the high voltage (HV) electrical power systems, different materials are used as the role of insulation to protect the incipient failure inside the HV power equipments. One of the common phenomenas in insulations is Partial Discharge (PD). Because of the high voltage stress, the weak section inside the insulator causes the partial discharge (PD), which is known as a local electrical breakdown. The maximum amplitude of PD could accelerate the destruction process of insulation material. Also, during practical applications in the power systems, voltages with different levels are used or created suddenly. Therefore, it is necessary to analyze the effect of voltage characteristics on the PD. In this paper, the effect of DC, AC and impulse voltage on the maximum amplitude of PD are studied within the MATLAB Simulink platform. Finally, to show the effect of each voltage level on the PD, results are compared with each other in the single and multi cavity situations. The test materials for this research are epoxy resin and oil-impregnated paper. Also, this paper provides a comparison between two different insulation materials.

Keywords: Quantum-dot cellular automata; Majority gate; Nanoscale circuits; Fault tolerance.

1. INTRODUCTION

Current CMOS technology is going to approach a scaling limitation in deep nanometer technologies. The CMOS technology in nanoscales experienced some problems due to increase in amounts of variation in every aspect of a nanometer design. Quantum-dot cellular automata (QCA) is one of the promising new technologies for the future generation ICs that overcomes the limitation of CMOS [1–3]. The fundamental unit of QCA-based design is majority gate; hence, efficient construction of QCA circuits using majority gates has attracted a lot of attention [4–9]. Since every QCA circuit can be implemented by using only majority and inverter gates, inverter becomes another important component in constructing QCA circuits. Hence, efficiently constructing an inverter in QCA is of the great importance [10–12].

Fault-tolerant design of QCA logic circuits is absolutely necessary for characterization of defective behavior of QCA circuits. In recent years the fault-tolerant properties of QCA circuits has been demonstrated by many researchers [13–17].

As already mentioned, the basic building block of QCA circuit is the majority gate; majority logic is the way of implementing digital operations in a way different from that of Boolean logic. The logic process of majority logic is more sophisticated than that of Boolean logic; consequently, majority logic is more powerful for im-

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plementing a given digital function with a smaller number of logic gates [18, 19].

This paper investigates a new design for fault-tolerant majority gates. By applying this new proposed scheme for fault-tolerant majority gates, we can obtain high degree of robustness in terms of the misalignment, missing, and dislocation cells. The presented method is justified based on some physical proofs. In comparison to other existing implementations, this majority gate demonstrates significant improvement in terms of the area, complexity, and robustness.

One of the most important components in any arithmetic and digital circuit in QCA and VLSI is the full adder [4–7, 20– 24]. A fault-tolerant QCA full adder can be implemented using the new fault-tolerant majority gate. Improving the robustness of the majority gate cells leads to the efficient designing of many arithmetic circuits.

2. MATERIALS AND METHODS

2.1. Background

Quantum cellular automata (QCA) is a new device architecture, which is proposed by Lent and Tougaw [25]. A quantum cell can be viewed as a set of four charge containers or dots, positioned at the corner of a square. The cell contains two extra mobile electrons, which can lead the quantum mechanically into the tunnels between dots but not cells. The electrons are forced to the corner positions by Columbic repulsion. These two possible polarization states represent logic "0" and "1," as shown in Fig. 1(a) [2].

As shown in Fig. 1(b), an ordinary QCA gate implementing the majority function is as follows: assuming three inputs labeled A, B, and C, the logic function of the majority gate is:

M(A, B, C) = AB + AC + BC.

As illustrated in Figure 1(b) each QCA majority gate requires only five cells. In Fig. 1(c), a QCA inverter is shown which simply returns the opposite value that was put in.

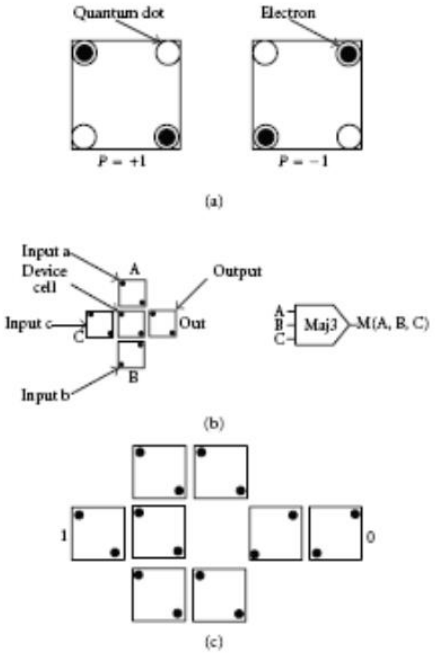

Fig. 1 (a) Basic QCA cell and binary encoding, (b) a QCA majority gate, (c) a QCA inverter.

2.2. Faults of QCA Circuits

Three major categories of faults can occur during the assembly of a QCA circuit. First, faults may occur when quantum cells are shifted from their intended locations which are called "misalignment" of cells. Sometimes misalignment of cells have no effect on functionality of a QCA circuit, and also sometimes a misalignment of cells may cause a polarity opposite what it should be. The second type of faults occurs when the quantum cell itself is "missing" resulting in the cell defection situation. If the gap between ideal cells is large enough, it would have no influence on its neighbors and it can cause a circuit to cease functioning well. The third type of the faults occurs when quantum cells are rotated relative to the other cells in the array which is called "dislocation" cells. Also, in this case, the circuit may cease to function (Fig. 2).

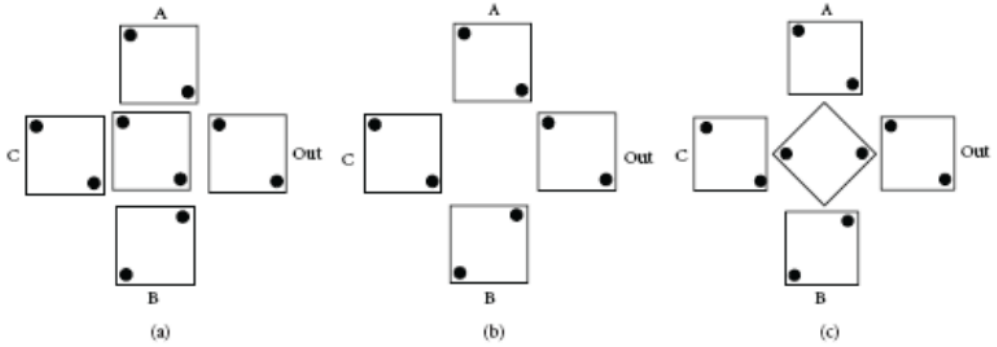

Fig. 2 Faults of majority gate, (a) misalignment cell, (b) missing cell, and (c) dislocation cell .

Based on the researches which have been performed so far, some fault-tolerant QCA circuits have been designed and tested [14–16]. But, these circuits are not robust enough to operate correctly when facing the faults. In the next section, we have attempted to make a novel fault-tolerant majority gate using the physical relation, in such a manner that can continue to operate correctly at the presence of the above-mentioned faults.

2.3. Novel Design for Fault-Tolerant Majority Gate

Majority is a voter. In our new structure, a fault-tolerant majority gate can be implemented as shown in Figure 3. In this scheme we have three inputs labeled A, B, and C and the output cell is shown by *out*. In addition, there are nine middle cells labeled 1, 2, 3, 4, 5, 6, 7, 8, and 9. Polarization of input cells is fixed and middle cells and output cell are free to change.

As it is clear in Fig. 3, a new fault-tolerant majority gate only needs 13 cells and by considering some physical relations it is implemented.

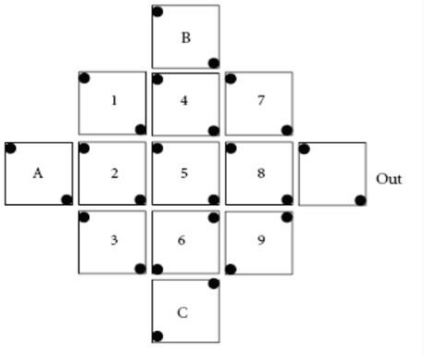

Fig. 3 Proposed fault-tolerant majority gate

Regarding the physical proofs, assume that all cells are similar and the length of each one is a (a = 18 nm) and there is a space of x (x = 2 nm) between each two neighbors.

In all figures, rectangles show a QCA cell and the circles inside show the electrons within that cell. It should be noted that in order to achieve more stability, electrons of QCA cell are arranged in a way to reach the minimum kink energy.

The kink energy between two electron charges is calculated using (1a). In this equation, U is the kink energy, k is the fixed colon, $q1$ and $q2$ are the electric charges, and r is the distance between two electric charges. By putting the values of k and q, we obtain (1b). UT is the summation of the kink energies that is calculated from (2) [4, 26–28].

$$U\frac{kq_1q_2}{r}, \tag{1a}$$

$$\begin{aligned} kq_1q_2 &= 9 * 10^9 * (1.6)^2 * 10^{-38} \\ &= 23.04 * 10^{-29} = A = cte, \end{aligned} \tag{1b}$$

$$U_T = \sum_{i=1}^{2} U_i. \tag{2}$$

2.4. Physical Proof

The proposed fault-tolerant majority gate has nine different middle cells, so we should check all the faults that might occur in the middle cells to verify the correctness of this scheme. Here, only one of the faults (missing cell 5) is proved and the others can be proved as well. The assumed values of input cells are A = B = 1, C = 0.

Initially, we calculate the kink energy existing between each electron (*e*1, *e*2, *e*3, *e*4, *e*5, *e*6, *e*7, *e*8, *e*9, and *e*10) with electrons "*x*" and "*y*" in (a) and (b) states using (1a) and (1b) equations. For example, *Ui* is the kink energy existing between electrons *ei* and *x* (or *y*). Also, *ri* is the distance between two electron charges. Then we calculate the total kink energy (*UT*) in both states using (2). The comparison of the total kink energies in both (a) and (b) states shows which state (a or b) is more stable. We consider the state that has the lower kink energy level as the more suitable one.

As the proof method is similar for all cells and their values and also due to lack of space, only the first part of this proof is stated and the rest of the relations are omitted (Fig. 4).

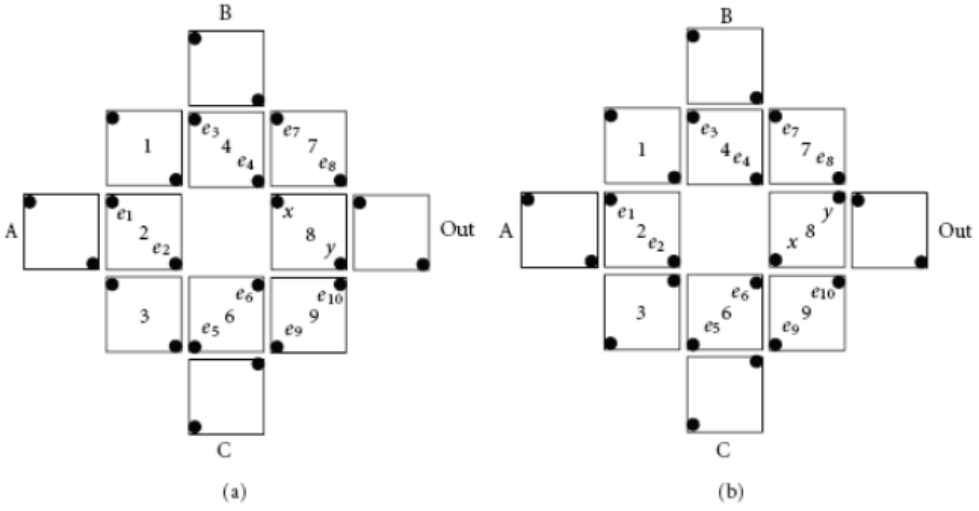

Fig. 4 (a) The one value in cell 8, (b) the zero value in cell 8.

Fig. 4(a) (Electron *x*):

$$U_{T_{11}} = \sum_{i=1}^{10} U_i = 15.92 * 10^{-20}(J),$$

$$U_{T_1} = \sum_{i=1}^{2} U_{1i} = 36.36 * 10^{-20}(J).$$

$$U_{T_{12}} = \sum_{i=1}^{10} U_i = 20.44 * 10^{-20}(J).$$

Fig. 4(b) (Electron *x*):

$$U_{T_{21}} = \sum_{i=1}^{10} U_i = 18.1 * 10^{-20}(J),$$

$$U_{T_2} = \sum_{i=1}^{2} U_{2i} = 40.03 * 10^{-20}(J).$$

$$U_{T_{22}} = \sum_{i=1}^{10} U_i = 21.93 * 10^{-20}(J).$$

By comparing the achieved results, the electrons in the cell 8 are positioned in the state (a) which is more stable and has the lower kink energy. It is worth mentioning that in all cells *UT*1 is the kink energy in +1 polarization and *UT*2 is the kink energy in −1 polarization.

From the above computing, we can infer that the proposed structure for implementing a fault-tolerant majority gate is completely correct and resulted in a correct state for the output cell when faults occur.

3. CONCLUSION

In this paper, we analyzed fault-tolerance properties of the conventional design for the majority gate as the base logic gate for implementing QCA circuits. High performance logic component can be achieved by utilizing this fault-tolerant majority gate. We analyzed robustness of the proposed majority gate in terms of

(i) Misalignment cells,

(ii) Missing cells,

(iii) Dislocation cells.

Some physical proofs have verified the functionality of this scheme. The presented structure

demonstrates significant improvements in terms of the area, complexity, and robustness in comparison to previous designs.

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