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Research Article

Efficient Design of Parity-Preserving Reversible Non-Restoring Divider

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Abstract

One of the basic challenges in high-density integrated circuits is loss of power consumption, which is caused by presence of transistors in circuits and causes the temperature of the circuit to increase. The design of digital circuits in a reversible way can be used as one of efficient approaches to solve this challenge. In addition, the design of parity-preserving reversible circuits can be very effective in detecting faults in circuits. Dividers are used as one of the most widely used circuits in digital computing systems. Divider circuits include an adder, a multiplexer and two sequential register and parallel-in to parallel-out left shift register circuits. This paper is presented a new and efficient design of a parity-preserving reversible non-restoring divider. For this purpose, first, a parity-preserving reversible D-latch is proposed. second, a parity-preserving reversible n-bit register is presented using the proposed reversible D-latch. Third, a parity-preserving reversible (n+1) bit shift register using the proposed reversible D-latch and other reversible gates is proposed. Finally, a parity-preserving reversible n bit divider is developed based on the non-restoring algorithm. The results of comparisons show that the proposed circuit is superior in terms of evaluation criteria of reversible circuits such as quantum cost, number of constant inputs and number of garbage outputs compared to previous works.

Keywords: Divider, non-restoring algorithm, Parity-preserving reversible circuit, Quantum computing, Reversible logic.

Highlights

- Proposing a reversible D-latch memory with parity preserving ability.
- Introducing a reversible register with parity preserving ability.
- Providing a parity preserving reversible left-shift register with parallel load capability (PIPO).
- Development of an efficient parity preserving reversible non-restoring divider using the proposed circuits.

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1. Introduction

One of the important challenges in the development of high-density integrated circuits is power loss, which leads to increased circuit temperature. This issue is a major concern in the design of classical circuits. Therefore, circuit design at the nanoscale level is paramount importance [1-3]. Circuit design using reversible logica1 can overcome the fundamental challenge of power consumption and, due to its quantum implementation capability, can significantly reduce circuit complexity and density [4]. Therefore, soon, we will see widespread use of reversible logic and quantum computing in digital circuit design [5, 6]. Furthermore, to design circuits with detect computational errors capability, we can use parity-preserving reversible circuits [7]. In 1961, Landauer proved that in modern classical computing, for every bit of data that is lost, KTLn2 joules of energy is released as heat, where K is Boltzmann's constant and T is the absolute temperature of the environment [8]. In 1965, Moore theorized that the hundred percent increase in the number of transistors every 18 months would lead to heat generation and energy dissipation, becoming a significant challenge in integrated circuit design [9]. In 1973, Bennett proposed that using reversible logic would reduce power consumption in circuits [10]. Quantum operations are inherently reversible, and reversible gates with parity-preserving capability are important factors in the design of reversible circuits. Also, the parity-preserving feature using parity-preserving gates, by comparing the parity-preserving between the inputs and outputs helps to detect permanent and transient computational errors in reversible circuits. Therefore, designs of parity-preserving reversible gates reduce the probability of computational errors [11]. Divider circuits are considered one of the essential parts of digital computing units. Dividers can perform division operations using either restoring or non-restoring approaches [12], which include a set of shift, subtraction, and addition operations. Therefore, divider circuits consist of sequential units such as registers, and shiftregisters, as well as combinational units such as adders and multiplexers. In 2009, Nayem et al. proposed the first n-bit reversible divider to perform division operations over the range of positive integers using the non-restoring algorithm [13]. In the proposed design, an n-bit multiplexer, an n-bit reversible register, and an (n+1)-bit left-shift register are based on the FRG gate, and the MTSG reversible adder gate and the 3-TS gate are used to design the (n+1)-bit parallel reversible adder. In the presented divider, the constant inputs are equal to (10n + 11), the garbage outputs are equal to (11n+18), and the quantum cost is equal to (50n+61). Although the presented divider is reversible, it does not have the parity-preserving feature. In 2011, Dastan and Haghparast presented the first n-bit reversible parity-preserving non-restoring divider [14]. In this article, two different designs are presented using D-latch and without D-latch. In the presented structure, using the FRG and DFG gates and by proposing various reversible gates, two (n+1)-bit adder circuits and one (n+1)-bit left-shift register are proposed. The first design consists of (11n+14) constant inputs, (12n+18) redundant outputs, and a quantum cost of (75n+60). The second approach also has (11n+12) constant inputs, (12n+16) garbage outputs, and a quantum cost of (75n+53). In 2016, Babu et al. an n-bit reversible non-restoring parity-preserving divider is presented [15]. In the divider design, by presenting the reversible RR and F2PG gates, and using the DFG gate, a (n+1)-bit reversible left-shift register is designed, also by presenting the NFTFAG gate and using the DFG, a (n+1)-bit reversible parallel adder is designed. The divider has (10n + 17) constant inputs, (12n + 17) garbage outputs, and a quantum cost of (67n + 69). In 2022, Talebi et al. proposed an n-bit reversible parity-preserving divider [16]. In this divider, efficient designs have been performed including the adder, the left-shift register, and the n-bit register. In this divider, the reversible adder is based on the TMB1 reversible gate, and the TMP1 left-shift register is based on the FRG, DFG, and E1-latch reversible gates. The circuit includes (13n +18) constant inputs, (15n +18) garbage outputs and quantum cost equal to (66n + 68).

2. Innovation and contributions

This paper presents a reversible parity-preserving divider based on a non-restoring approach, where reversible design principles are correctly observed. The ideas and innovations of this article are as follows:

- Efficient design of a one-bit reversible parity-preserving D-latch
- Proposal of an n-bit reversible register using the proposed D-latch with n constant inputs, n garbage outputs, and quantum cost of 6n
- Proposal of a parity-preserving Parallel-In Parallel-Out left-shift register using proposed D-latch and reversible FRG and DFG gates
- Development of an efficient parity-preserving non-restoring reversible divider using the proposed circuits

3. Materials and Methods

Dividers are one of the most commonly used circuits in digital computing systems. Divider circuits consist of basic units such as adders, multiplexers, and two sequential circuits: a register and a Parallel-In Parallel-Out left shift register. This article presents an efficient design of a parity-preserving non-restoring reversible divider. For this purpose, a reversible D-latch with balance preservation capability is proposed initially. Then, a reversible n-bit parity-preserving register is presented using the proposed reversible D-latch. Subsequently, a reversible (n+1)-bit parity-preserving left-shift register is proposed using the proposed D-latch and other reversible gates. Finally, an n-bit reversible parity-preserving divider is developed based on the non-restoring algorithm.

4. Results and Discussion

This section reviews the efficiency evaluation of the proposed designs from the perspective of reversible circuit evaluation criteria, including constant inputs, garbage outputs, and quantum cost. The used criteria are independent of the technology used for construction. The proposed reversible register is compared with two reversible registers presented in the references [17, 18], with

the results shown in Table 7. The proposed reversible register demonstrates superiority in terms of reduced quantum cost, garbage outputs, and delay compared to the reference [17], and it excels in reference [18] in terms of fewer garbage outputs and parity-preserving.
The proposed (n+1)-bit reversible left shift register is evaluated and compared with four existing designs in references [13-15, 18], with the results presented in Table 8. Compared to the design in reference [13], it excels in terms of the number of garbage outputs and delay, to reference [14] in terms of quantum cost and delay, to reference [15] in terms of quantum cost, and finally to reference [18] in terms of fewer garbage outputs and parity-preserving.
Lastly, the proposed n-bit reversible divider is compared with designs presented in references[14-16]. The proposed n-bit divider has a quantum cost of (66n+50), garbage outputs of (12n+16), constant inputs of (10n+12), and a delay of (98△). The comparison results of the proposed divider with the designs in references [14-16] are shown in Table 10. The proposed divider demonstrates improvements over the first design in reference [14] in terms of quantum cost, garbage outputs, constant inputs, and delay, and also over the second design in reference [14] in terms of quantum cost, constant inputs, and delay. Compared to the design in reference [15], it shows superiority in terms of quantum cost, garbage outputs, and constant inputs, and compared to the design in reference [16], it shows optimization in terms of quantum cost, garbage outputs, constant inputs, and delay. The results indicate that the proposed design offers better evaluation parameters and lower quantum cost compared to existing designs.

5. Conclusion

This paper proposes an optimized design of an n-bit non-recovery reversible divider with balance preservation capability for dividing positive integers. For this purpose, initially, a reversible D-type memory flip-flop with balance preservation capability is proposed. Then, an efficient reversible register is presented using the proposed state holder. Next, a left-shift register is proposed using the synergy of the proposed D-type state holder and the reversible gates FRG and DFG. Finally, with the help of the proposed reversible circuits, an optimized non-recovery reversible divider is developed. Additionally, to reduce the complexity of the proposed divider, the best available reversible adders and multiplexers were used. The evaluation results show that the proposed divider has (10n+12) fixed inputs, (12n+16) redundant outputs, and a quantum cost of (66n+50). Comparison results indicate the superiority of the proposed design in many evaluation criteria compared to the best previous design.

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Appendix

Table 1: truth table of the DFG gate

Input			Output		
A	B	C	P	Q	**R**
0	0	0	0	0	**0**
0	0	1	0	0	**1**
0	1	0	0	1	**0**
0	1	1	0	1	**1**
1	0	0	1	1	**1**
1	0	1	1	1	**0**
1	1	0	1	0	**1**
1	1	1	1	0	**0**

Table 2: truth table of the FRG gate

Input			Output		
A	B	C	P	Q	**R**
0	0	0	0	0	**0**
0	0	1	0	0	**1**
0	1	0	0	1	**0**
0	1	1	0	1	**1**
1	0	0	1	0	**0**
1	0	1	1	1	**0**
1	1	0	1	0	**1**
1	1	1	1	1	**1**

Table 3: truth table of the BHPF gate

Input				Output			
A	**B**	**C**	**D**	**P**	**Q**	**R**	**S**
0	0	0	0	0	0	0	**0**
0	0	0	1	0	0	0	**1**
0	0	1	0	0	0	1	**0**
0	0	1	1	0	0	1	**1**
0	1	0	0	0	1	1	**1**
0	1	0	1	0	1	1	**0**
0	1	1	0	0	1	0	**1**
0	1	1	1	0	1	0	**0**
1	0	0	0	1	1	0	**1**
1	0	0	1	1	1	0	**0**
1	0	1	0	1	1	1	**1**
1	0	1	1	1	1	1	**0**
1	1	0	0	1	0	1	**0**
1	1	0	1	1	0	1	**1**
1	1	1	0	1	0	0	**0**
1	1	1	1	1	0	0	**1**

Table 4: truth table of the TMB1 block

Input					Output				
A	B	C	D	E	P	Q	R	S	T
0	0	0	0	0	1	1	0	0	0
0	0	0	0	1	1	1	0	0	1
0	0	0	1	0	1	1	1	1	1
0	0	0	1	1	1	1	1	1	0
0	0	1	0	0	1	1	1	0	0
0	0	1	0	1	1	1	1	0	1
0	0	1	1	0	1	1	0	1	1
0	0	1	1	1	1	1	0	1	0
0	1	0	0	0	1	0	1	0	1
0	1	0	0	1	1	0	1	0	0
0	1	0	1	0	1	0	0	0	1
0	1	0	1	1	1	0	0	0	0
0	1	1	0	0	1	0	0	1	0
0	1	1	0	1	1	0	0	1	1
0	1	1	1	0	1	0	1	1	0
0	1	1	1	1	1	0	1	1	1
1	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	1	0	1
1	0	0	1	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	1
1	0	1	0	0	0	0	0	1	1
1	0	1	0	1	0	0	0	1	0
1	0	1	1	0	0	0	1	1	1
1	0	1	1	1	0	0	1	1	0
1	1	0	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0	1	1
1	1	0	1	0	0	1	1	0	1
1	1	0	1	1	0	1	1	0	0
1	1	1	0	0	0	1	1	1	0
1	1	1	0	1	0	1	1	1	1
1	1	1	1	0	0	1	0	0	1
1	1	1	1	1	0	1	0	0	0

Table 5: truth table of the N1 block

Input				Output			
A	B	C	D	P	Q	R	**S**
0	0	0	0	0	0	0	**0**
0	0	0	1	0	0	0	**1**
0	0	1	0	0	0	1	**0**
0	0	1	1	1	1	1	**1**
0	1	0	0	0	1	0	**0**
0	1	0	1	0	1	0	**1**
0	1	1	0	0	1	1	**0**
0	1	1	1	1	0	1	**1**
1	0	0	0	1	1	1	**0**
1	0	0	1	0	0	1	**1**
1	0	1	0	1	1	0	**0**
1	0	1	1	1	1	0	**1**
1	1	0	0	1	0	1	**0**
1	1	0	1	0	1	1	**1**
1	1	1	0	1	0	0	**0**
1	1	1	1	1	0	0	**1**

Table 6: Control functions of left-shift register inputs

Mode control		Output Q_i	Operation
E	**SV**		
0	0	Q_{i-1}	left-shift
1	0	I_i	Parallel load
×	1	Q_i	No change

Table 7: comparison of proposed reversible register with previous works

Parity-Preserving	Delay n=1	Constant-Inputs	Garbage-Outputs	Quantum Cost	Designs
Yes	5△	n	n	6n	Proposed design
Yes	6△	n	n+1	7n	Design in [17]
No	5△	n	n+1	5n	Design in [18]

Table 8: comparison of proposed reversible PIPO left-shift register with previous works

Parity-Preserving	Delay n=1	Constant-Inputs	Garbage-Outputs	Quantum Cost	Designs
Yes	15△	3n	3n + 2	18n	Proposed design
No	19△	3n	3n + 3	18n	Design in [13]
Yes	16△	3n	3n + 2	19n	Design in [14]
Yes	-	3n	3n + 1	22n	Design in [15]
No	14△	3n	3n + 3	15n	Design in [18]

Table 9: results of evaluation of proposed parity-preserving reversible divider

Parity-Preserving	Delay n=1	Constant-Inputs	Garbage-Outputs	Quantum Cost	Designs
Yes	4△	0	n	5n	n-bit MUX
Yes	4△+4△	0	n+1	5n+5	(n+1) bit MUX
Yes	5△	n	n	6n	n-bit register
Yes	15△	3n	3n+2	18n	n-bit PIPO left-shift register
Yes	15△+15△	3n	3n+5	18n+18	(n+1)-bit PIPO left-shift register
Yes	9△	n+4	3n+2	8n+3	(n+1)-bit adder
Yes	27△	2n+8	6	6n+24	Other gates

Table 10: comparison results of proposed reversible divider with previous works

Parity-Preserving	Delay n=1	Constant-Inputs	Garbage-Outputs	Quantum Cost	Designs
Yes	98△	10n+12	12n+16	66n + 50	Proposed design
Yes	112△	11n + 14	12n + 20	75n + 60	First Design in [14]
Yes	106△	11n+12	12n+16	75n + 53	Second Design in [14]
Yes	-	10n+17	12n+17	67n + 69	Design in [15]
Yes	110△	13n+18	15n+18	66n + 68	Design in [16]

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