Improved Structure Design of a Single Phase Multilevel Inverter with the Aim of Reducing Switching Devices

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Abstract – In this paper, a multilevel inverter has been designed and improved in order to lower the number of switching devices, especially when the number of level of the output power is large. The input to the inverter comes from internal direct current (DC) resources which are interconnected via the power circuit breaker. Compared to the classical topologies and similar designs, the proposed method needs lower number of switching device to provide the same power levels at the output. As a precursor, we have drawn the desired topology for a 9-level power level. The procedure can be completed using switching by a phase shift keying techniques, which in addition, make practical output power with higher number of levels. The proposed topology has been tested against topologies of the power class 1 and/or similar classes, based on the simulations in the MATLAB/Simulink environment. The results of the simulation deemed to be promising for future networks.

Keywords: Total Harmonic Distortion (THD), Multi-Level Inverter (MLI), device reduction, classical topology.

I. Introduction

Over the last decades the multi-level voltage inverters have been considered as a viable solution for high power applications [1]. Using the high power and various DC inputs (extracted from capacitors or voltage/current resources), and control circuits, the output voltage can be tuned to any amplitude and frequency. In multi-level inverters, compared to the input voltage as well, the stress voltage over the power switches are lower due to multi-level structures [2]. Moreover, waveform include lower harmonic contents compared to traditional two-level convertors. Other advantages include less stress of *dv/dt* and improved reliability for possible faults [3]. The benefits, altogether, results in researchers' attentions to focus on the application of multi-lever inverters for low power applications [4].

The quality of the output waveform is a function of number of the levels. As a rule of thumb, for higher qualities, number of power switches and startup gates will be rises, too. This, in turn, makes the system more complex and more costly in one hand, and reduce the reliability as well as efficiency of the system, on the other. Thus, in the optimization problem, in order to produce output waveforms with satisfied quality, the number of switches and gates must be lowered as many as possible [5]. Typical topologies which are studied more and commercially available as well are: Neutral Point Clamed (NPC), Cascaded H-Bridge (CHB) and Flying Capacitor (FC) [1, 3, 5-7]. Nonetheless, increasing the number of levels in the output wave will still increase the number of power switches and thus total costs, researchers still need to focus on lowering the number of power switches and startup gates. The horizon of viewpoints, here, can be subdivided into 3 cases: 1) Topological changes [8-12], 2) usage of asymmetrical resources [13-15] and 3) a combination of the two cases [16-18].

In this study, we have proposed a generalized topology in which lower number of electronic power switches are needed. In comparison with classical topologies of similar researches, the proposed topology needs a noticeable lower number of power switches. Furthermore, paralleled to symmetric DC inputs, the suggested topologies look liked CHB from two different aspects: 1) they both need individual DC input voltage resources and 2) the output voltage level is constructed using a combination of DC input resources. Therefore, the proposed topology can be used as a converter for renewal energy resources in which there are lots of individually separated DC resources [2, 7, and 9]. Besides, it can be used as medium voltage resources due to seperable DC inputs [6]. Potential application include cases such as electrical vehicle and driving force or propulsion in submarines, which depends on batteries, it can be used easily.

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The structure of the paper is as follows. In the next section, the general structure of the proposed topology is presented along with the corresponding mathematical relationships. The operational performance of the adopted topology, will also be explained in this section using a single phase inverter with 9 output levels. In section III, a control scheme based on Pulse-Width-Modulation (PWM) is proposed for the inverter; this can be also used for other multilevel structures. Section IV presents the simulation results while section V, our results when compared with those driven from the classic and similar researches. Finally, conclusions of the paper will be given in section VI.

II. The proposed multi-level topology

In this section, the proposed inverter structure will be shown and the roles of different parts will be highlighted with the help of a single phase one-level inverter.

A. The general structure

The generalized single phase along the proposed topology are illustrated in fig.1. A general single phase encompasses n individual DC sources. In this figure, E_j, $j=1,,, n$, denote the input sources while current of each source is referred to by $I_j(t)$. The power switches can be implemented using transistors (such as MOSFET or IGBT) finally paralleled with an opposite direction diode. In fig.1, we have used IGBTs as power switches completed with the protective diode. In this figure, power switches, voltages and currents are referred to T_j, $V_L(t)$ and $I_L(t)$, respectively.

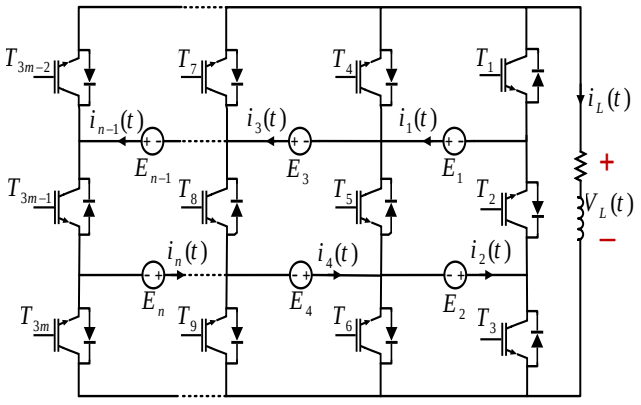


Fig. 1: The generalized Topology of proposed single phase inverter.

B. principle of operation

Here, operation the topology will be explained for a single phase inverter and four current sources E_1, E_2, E_3 and E_4. As depicted in fig. 2, this provide us with 9 operational switch (T_j , j=1,2,3,4,5,6,7,8,9) which altogether, create 25 states for the output power and 9 level for the output voltage. These states are listed in Table I along with the corresponding voltages.

Table I shows the output voltage $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 2V_{dc}$, $\pm 4V_{dc}$ and zero when the DC current sources are $E_1 = E_2 = V_{dc}$, and $E_3 = E_4 = 2V_{dc}$, respectively. In this case, states 1 and 2 and 3 are used for zero output, while states 4,5,6,7, for outputs $+V_{dc}$, states 8,9,10,11 for outputs $+2V_{dc}$, states 12 and 13 for voltage outputs $+3V_{dc}$ and finally, state 14 is used to produce $+4V_{dc}$ at the output. In the same line of thought, states 15,16,17,18 are used to produce $-V_{dc}$, states 19-22 for $-2V_{dc}$, states 23-24 for $-3V_{dc}$, and finally states 25 for the $-4V_{dc}$ output voltages.

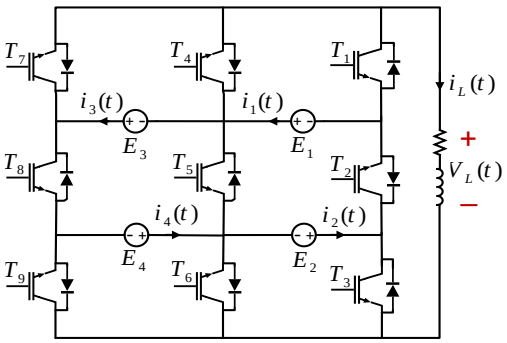


Fig. 2: the single phase inverter based on the nine level topology

It must be noted that the DC voltage sources are not permitted to variations, while in practice, this can be a possibility. For example, battery charges are prone to variation. Moreover, in case of using Photo-Voltaic (PV) resource to supply the battery charges, topographical variations such as shadowing might take place. To remedy these problems, there are hardware-based solutions (*e.g.*, using individual DC-DC inverters [8]) and software based answers where focus on output voltage control (batteries inter balances [19]).

Referring to the fig. 1, switching function of T_j (j=1,,,m) are defined as follows:

$$S = \begin{cases} 1, & if \;\; T_j \;\; is \;\; on \\ 0, & if \;\; T_j \;\; is \;\; off \end{cases} \qquad (1)$$

Moreover, the number of the output voltages will be:

$$N = 2n + 1 \qquad (2)$$

where n denotes number of DC input sources and N, the number of output voltages.

Table I: Various switching modes for the proposed topology with 4 DC sources

mode	Switch States(1=on:0=off)									Output Voltage
	T1	T2	T3	T4	T5	T6	T7	T8	T9	
1	1	1	1	0	0	0	0	0	0	0
2	0	0	0	1	1	1	0	0	0	0
3	0	0	0	0	0	0	1	1	1	0
4	1	1	0	0	0	1	0	0	0	+Vdc
5	0	0	0	1	1	0	0	0	1	+Vdc
6	0	1	1	1	0	0	0	0	0	+Vdc
7	0	0	0	0	1	1	1	0	0	+Vdc
8	1	1	0	0	0	0	0	0	1	+2Vdc
9	0	1	1	0	0	0	1	0	0	+2Vdc
10	0	0	0	0	1	0	1	0	1	+2Vdc
11	0	1	0	1	0	1	0	0	0	+2Vdc
12	0	1	0	1	0	0	0	0	1	+3Vdc
13	0	1	0	0	0	1	0	0	1	+3Vdc
14	0	1	0	0	0	0	1	0	1	+4Vdc
15	0	0	1	1	1	0	0	0	0	-Vdc
16	0	0	0	0	0	1	1	1	0	-Vdc
17	1	0	0	0	1	1	0	0	0	-Vdc
18	0	0	0	1	0	0	0	1	1	-Vdc
19	0	0	1	0	0	0	1	1	0	-2Vdc
20	1	0	0	0	0	0	0	1	1	-2Vdc
21	1	0	1	0	1	0	0	0	0	-2Vdc
22	0	0	0	1	0	1	0	1	0	-2Vdc
23	0	0	1	1	0	0	0	1	0	-3Vdc
24	1	0	0	0	0	1	0	1	0	-3Vdc
25	1	0	1	0	0	0	0	1	0	-4Vdc

III. Switching scheme

For the multilevel inverter modulation, high frequency modulations such as multicarrier PWM and spatial modulation techniques can be used [22, 23]. On the other hand, low frequency modulations such as active harmonic removal, selected harmonic removal, among others, are applicable [24-26]. The proposed topology can be adapted with either of these methods. In this paper, we have used the multi-carrier PWM for the switching purposes. In this scheme, the carrier signals are first compared with the reference signal and then, the results would be used to drive the power transistors. In the proposed scheme, one single switch possibly contribute to produce more than one single output at the output terminal. Therefore, in this section, we have come up with a control scheme which is to be used output with nine levels. The scheme can be generalized to cover higher level of the output, too.

The inverter switching modulation scheme and the related waveforms are, respectively, depicted in figs 3 and 4. In this scheme, 8 triangular waveform with the frequency 350Hz have been used as the carriers. The carriers are configured based on their initial phases.

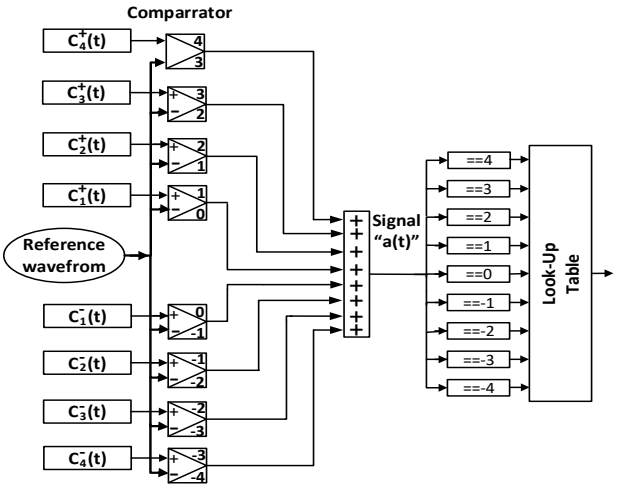


Fig. 3. The proposed control scheme for the 5 level inverter

Table II: The reference table for nine level inverter based on the proposed topology

On switches	Load voltage	state	Levels "*a*"
T_2,T_7,T_9	96	14	4
T_1,T_4,T_9	72	12	3
T_1,T_2,T_9	48	8	2
T_1,T_2,T_6	24	4	1
T_7,T_8,T_9	0	3	0
T_3,T_4,T_5	-24	15	-1
T_3,T_7,T_8	-48	19	-2
T_1,T_3,T_8	-96	25	-4

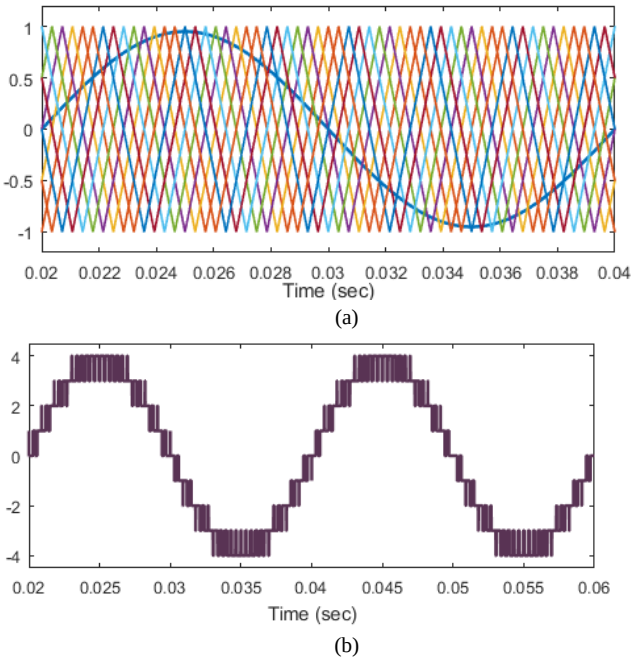


Fig. 4: (a) The reference and the carrier waveform for the proposed scheme of nine output level and (b) the signal "$a(t)$"

A sinusoid 50Hz waveform has been considered as the

reference signal. The carrier signals are in the form of $C_k^+(t);(k=1,2,3,4)$ with initial phases 0, 45, 90 and 135 and $c^-_k(t);(k=1,2,3,4)$ with initial phases 180, 225, 270, 315. The carriers and reference signals would be compared continuously with each other.

When the reference signal is greater than the carrier $C_k^+(t)$, the output of the comparator is equal to "*k*"; otherwise it is equal to "*k−1*". On the other hand, when the reference signal is greater than the carriers $C^-_k(t)$, the output of the comparator is equal to "−(*k−1*)"; otherwise it will be equal to "−*k*". Finally, the resulted signals are combined to give the signal *a*(*t*). The inverter switching will be according to the signal *a*(*t*). For example, when *a*(*t*) is equal to one, the output voltage must be $+V_{dc}$, which in turn determines that switches T_1,T_2,T_6 must be turned on. Table II illustrate which switches must be turned on and off for a given level of output.

IV. Simulation Results

In order to evaluate the performance of the proposed control scheme, a single phase nine output-level inverter has been in MATLAB/SIMULINK. For V_{dc}=55*V*, the switching pulses are drawn in fig. 5. The output voltage, which is combined of nine-level inverter outputs, as well as a Total Harmonic Distortion (THD) equal to 15.4% has been shown in fig. 6. In addition, fig. 7 illustrate the current waveforms and their corresponding THD.

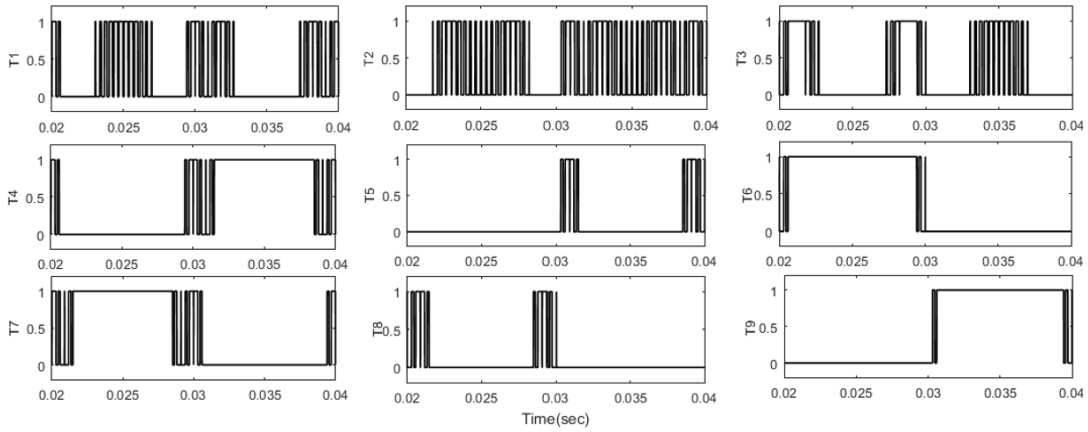
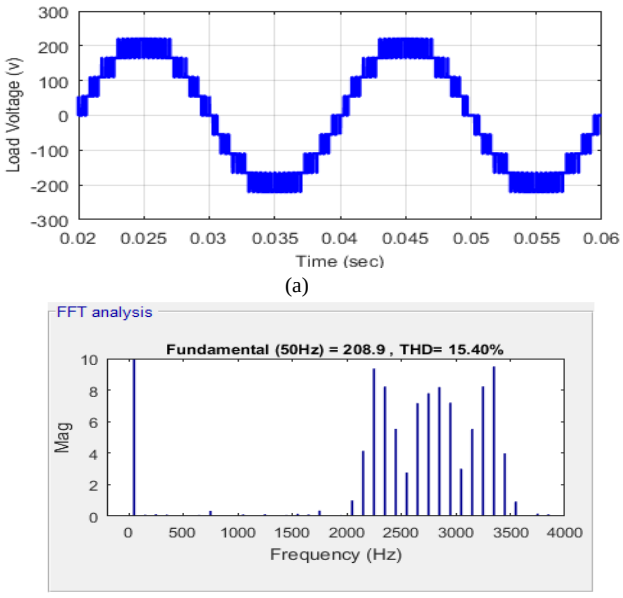


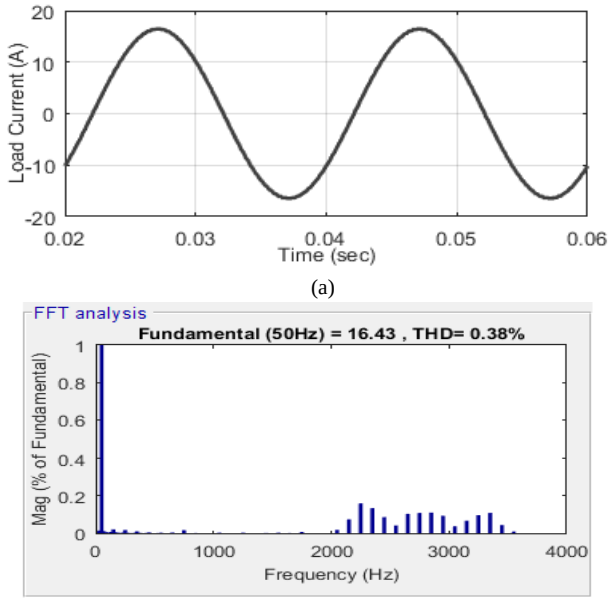
Fig. 5: The switching scheme for the nine level inverter



(a)

(b)

Fig. 6: The simulation results. (a) The output of the nine level voltage when the load is (RLR = 10Ω, L = 20 *mH*); (b) the distribution of the load harmonics (L = 20 *mH* , RLR = 10Ω).



(a)

(b)

Fig. 7: The simulation results. (a) The waveforms of the load currents and (b) the corresponding harmonics.

Now, if three more level be added to E_2, 6 more levels to E_3 and 2 more levels to E_4, then 8 more levels will be added to the number of levels of the outputs, which sums it up to 17. Results of the simulation for this case is shown in fig .8. We observe that the THD has been decreased from 15.4% to 7.56%, roughly to the half. In this case, size of the output filter will be naturally smaller than before which means saving in costs.

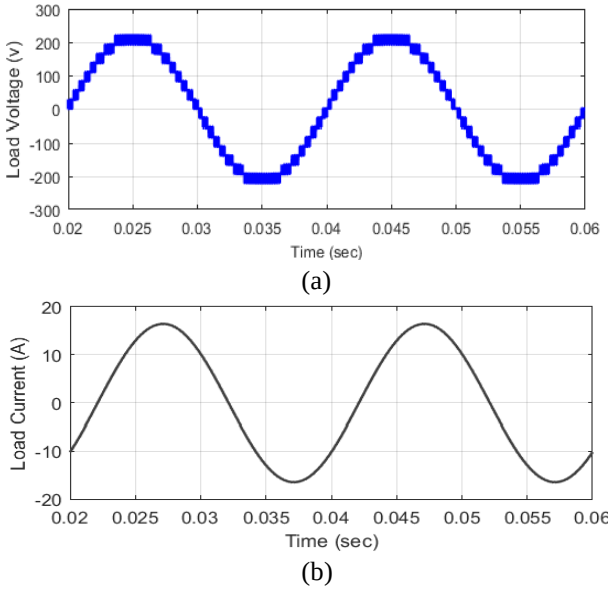


Fig. 8: waveforms of the load (a) voltages and (b) currents for RLR = 10Ω, L = 20 mH .

V. Comparisons with other Topologies

Conventional In this section, the proposed topology will be compared with its other counterparts. The comparison is made with the similar researches and based on elements' usages. To this end, we have used a function which is the relation of the number of the elements to the numbers of inverter's phase voltage [7]. The lower the function is, the less number has been used in the structure of the topology. As a matter of fact, this function is a one used for evaluation purposes which is defined,

$$F_{Componets/Level} = \frac{n_{Switch} + n_{Diode} + n_{Capacitore} + n_{Source}}{N_{Level}} \quad (1)$$

In Table III, numbers of the elements contributing in the construction of the different topologies have been shown for a single phase nine level inverter. From the table, it can be inferred the superiority of the proposed topology to the other counterparts. We also observe that, in the proposed topology, number of the power switches including power transistors and diodes are lower compared to the suggested topologies of the similar studies.

As it can also be seen from Table III, the proposed topology has lower FC/L with respect to conventional topologies as well as other similar researches. This indicate, thus, its less switching power loss and lower cost, which makes it a suitable candidate for industrial applications.

Table III: Comparison of the proposed topology with the conventional designs as well as the similar studies

FC/L	Diode	Capacitor	Source	Switches	Level	
2.22	0	0	4	16	9	CHB
4.33	14	8	1	16	9	NPC
5.88	0	36	1	16	9	FC
1.77	0	0	4	12	9	[28]
1.55	3	0	4	7	9	[29]
1.55	0	0	4	10	9	[30]
2.88	4	4	2	16	9	[31]
2.22	6	0	4	10	9	[32]
1.55	0	3	1	10	9	[33]
2.66	8	4	2	10	9	[34]
1.55	2	0	4	8	9	[35]
1.77	0	0	4	12	9	[36]
1.44	0	0	4	9	9	Proposed Topology

VI. Conclusion

Since multilevel inverters have many applications nowadays, researchers have done much efforts in order to reduce the number of the elements of their structure in one hand, and to increase number of the output levels, on the other. In this paper, a new topology has been proposed and its performance was explained. We claimed that the proposed topology has a lower number of parts compared to its counterparts with the same number of output levels. This has been proved with the help of computer simulation. Thus,

the proposed topology can be less costly and more practical, and hence suitable for industrial applications.

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