# A W-band Simultaneously Matched Power and Noise Low Noise Amplifier Using CMOS 0.13µm

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Received 10 December 2011; accepted 8 January 2013

**Abstract**

A complete procedure for the design of W-band low noise amplifier in MMIC technology is presented. The design is based on a simultaneously power and noise matched technique. For implementing the method, scalable bilateral transistor model parameters should be first extracted. The model is also used for transmission line utilized in the amplifier circuit. In the presented method, input/output matching networks and transistor gate width have been optimized for simultaneous maximum gain and minimum noise figure. It is easily shown that due to the low gain property of amplifier at high frequency, it is unconditionally stable; so, the common source topology has superior performance compared to other topologies. In addition, better noise figure, lower size and higher gain with the same power consumption can be achieved compared with those of the cascode topology. The simulation results show a gain of better than 18dB and noise figure of 7.4dB at 94GHz while input/output return losses are better than 20dB.

*Keywords:* Unilateral transistor model, Low Noise Amplifier (LNA), W-band amplifier, Monolithic Microwave Integrated Circuit (MMIC)

## 1. Introduction

Low noise amplifier (LNA) is one of the important components in high-frequency receiver front-end circuits. CMOS technology is especially popular to fabricate the circuits because of its maturity, low power consumption, high level of integration, small size and hence low-cost and also efficient and robust fabrication process compared with high performance SiGe and III-V technologies[1]-[2]. Due to these facts, CMOS technology has recently emerged as a suitable candidate in millimetre and sub-millimetre wave communication systems [1]-[3]. In [1] the first millimetre wave LNA using CMOS technology was presented. More recently, LNAs with higher frequency of operation using 90nm CMOS technology have been reported [4], [5].The challenging tasks for the design of amplifier are to take into account the effect of parasitic elements and different sources of loss, which limit the performance of the amplifier. In addition, optimum device selection and circuit design make the design process a time-consuming task at millimetre-wave.

130 nm CMOS technology has been implemented by many researchers in 60GHz and 77GHz bands [1]-[6]. In this paper, we designed a 94GHZ LNA using 130nm CMOS technology which is the highest frequency reported by this technology node. This amplifier is widely used in car radar.

## 2. Original Methodologies for Simultaneous Noise and Input Impedance Matching

There are four methods for noise matching which can be categorized as follows:

1) Classical Noise Matching (CNM)
2) Simultaneous Noise and Input Matching(SNIM)
3) Power Constrained Noise Optimization (PCNO)
4) Power Constrained SNIM (PCSNIM)

The original methodology for achieving simultaneous noise and input impedance match in integrated LNAs can be summarized in 4 steps. Detailed description and theoretical description and theoretical derivation of each step are given in [7]-[8]. In all CMOS technologies there is an optimum current density that minimizes transistor noise figure. The LNA should be biased at this current density. So transistor biasing is the first step in LNA design.

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Choosing the transistor size is the second step in LNA design. The size should be chosen such that the real part of the optimum noise impedance is equal to source impedance at the design frequency.

The input impedance matching is the third step in optimum LNA design. For the LNA shown in Fig. 1, the input impedance should be tuned to the $Z_0$ (source impedance) using two source and gate inductors $L_s$ and $L_g$. For Fig. 1, the input impedance can be written as:

$$Z_{in} = \omega_T L_s + j(\omega L_s + \omega L_g - \frac{1}{C_{gs}\omega}) \qquad (1)$$

where $\omega_T = \frac{g_m}{C_{gs}}$ is cut-off frequency of FET transistor.

For input impedance matching, weshould have:

$$\mathrm{Re}[Z_{in}] = Z_0 \qquad \mathrm{Im}[Z_0] = 0 \qquad (2)$$

From (2) one can write [9]:

$$L_s = \frac{Z_0}{\omega_T} \qquad L_g = \frac{1}{C_{gs}\omega^2} - L_s \qquad (3)$$

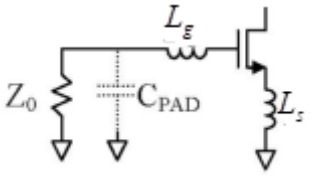


Fig. 1 Schematic of LNA input [9]

The fourth step is gain and noise optimization. For gain and noise optimization, an inductive load is employed to maximize gain and also linearity. In general to have simultaneous input impedance match and minimum noise figure (noise match), we should have [9]:

$$\begin{aligned} &Re[Z_{in}] = 50\Omega \\ &Im[Z_{in}] = 0 \\ &Re[Z_s] = Re[Z_{opt}] \\ &Im[Z_s] = Im[Z_{opt}] \end{aligned} \qquad (4)$$

where $Z_{opt} = R_{opt} + jX_{opt}$ is optimum noise impedance. Fig. 2 shows the one stage of designed amplifier with input/output matching circuit.

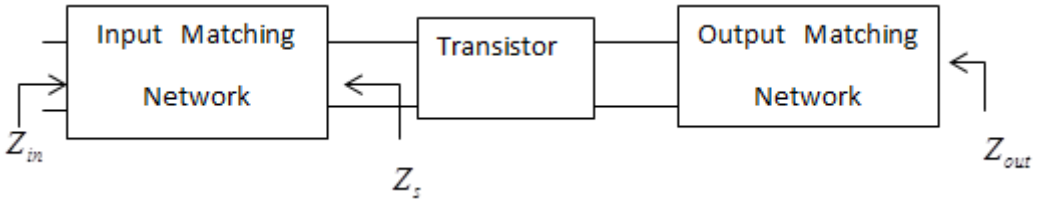


Fig. 2.One stage of designed amplifier with input/output matching circuit.

For a MOSFET transistor with no source inductor $L_s$ which its small signal model is shown in Fig. 3, noise parameters can be written as [9]:

$$Y_{opt0} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} - sC_{gs}(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}) \qquad (5)$$

$$F_{min0} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)} \qquad (6)$$

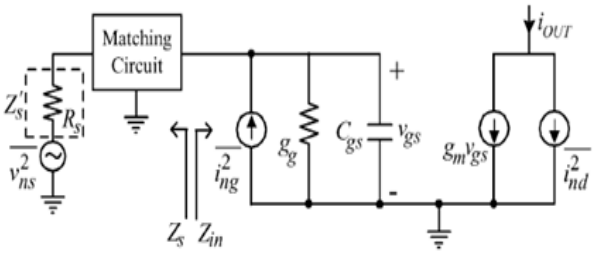


Fig. 3 Small signal model of MESFET transistor with its noise sources [10]

In Fig. 3, the noise parameters can be expressed as:

$$\bar{i}_{ng}^2 = 4kT\delta g_g \Delta f \qquad (7)$$

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \qquad (8)$$

In the above equations, $\delta$ is a constant which is $\frac{4}{3}$ for long channel transistor and $C_{gs}$ is gate-source capacitance.In equations (5) and (6), subscript 0 refers to

However, by adding inductor to the source of transistor (inductively source degenerated transistor) we can simultaneously match noise and input impedance. The case where no source inductor has been used, and parameter $c$is correlation coefficient which is given by:

$$c = \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\bar{i}_{ng}^2} \cdot \sqrt{\bar{i}_{nd}^2}} \qquad (9)$$

small signal model of inductively source degenerated transistor is shown in Fig. 4.

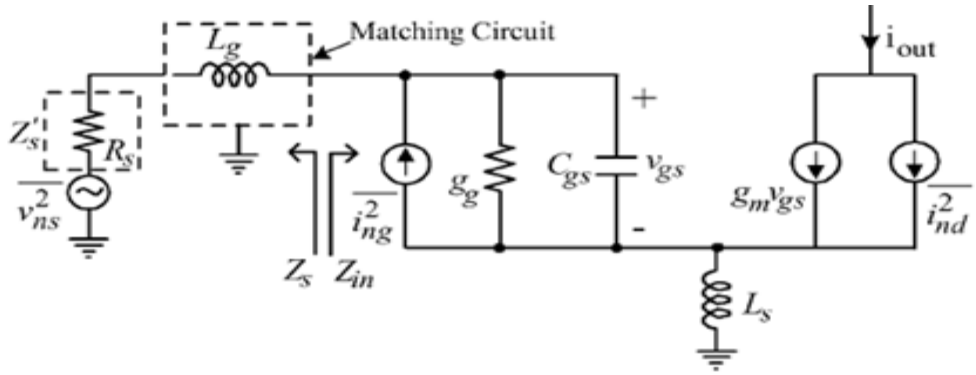


Fig. 4 Small signal of inductively source degenerated transistor with its noise sources [10]

For this topology the noise parameters are as follows [9]:

$$Z_{opt} = Z_{opt0} - sL_s \qquad (10)$$

$$F_{\min} = F_{\min 0} = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta(1 - |c|^2)} \qquad (11)$$

$$F = 1 + \frac{1}{g_m^2 R_s} \cdot \{\gamma g_{d0} \cdot \{[1 + s^2 C_{gs}(L_g + L_s)(1 + |c|\alpha\sqrt{\frac{\delta}{5\gamma}})]^2 -$$

$$(sC_{gs}R_s)^2 1 + |c|\alpha\sqrt{\frac{\delta}{5\gamma}})^2\} - \frac{\alpha\delta}{5}(1 - |c|^2) g_m (sC_{gs})^2 (R_s^2 - sL_g^2)\} \qquad (12)$$

Comparing (10)-(12) with (5)-(6) for Fig. 3 and Fig. 4, one can see that only $Z_{opt}$ for these figures is different and noise equivalent resistance and minimum noise figure are the same for both figures. In addition Eqs. (10)-(12) for any matching circuit and each source impedance $Z_s'$ are valid. From (5), optimum noise impedance for Fig. 3 can be expressed as:

$$Z_{opt0}=\frac{1}{Y_{opt0}}=\frac{\alpha\sqrt{\frac{\delta}{5\gamma(1-|c|^2)}}+j(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}})}{\omega C_{gs}\{\frac{\alpha^2\delta}{5\gamma(1-|c|^2}+(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}})^2\}} \quad (13)$$

As can be seen from (14), adding inductor to transistor's source creates a real part in input impedance while this impedance is purely imaginary without source inductor and $Y_{opt}$ has real part. In other word without adding inductor to the source this is not possible to satisfy $Z_{opt}=Z_{in}^{*}$ in order to simultaneously match power and noise. Therefore by adding inductor to the source one can reduce the difference between real parts of $Z_{opt}$ and $Z_{in}$. In addition the imaginary part of $Z_{in}$ changes with $sL_s$ and this followed by same change in $Z_{opt}$ as can be seen in Eq. (13). From (13), (10) can be re-expressed as:

$$Z_{opt}=\mathrm{Re}[Z_{opt0}]-m\frac{1}{sC_{gs}}-sL_s \quad (15)$$

where the constant $m$, for the typical device parameters of long channel MOSFETs, is approximately equal to 0.6. With technology scaling, the ratio $\frac{\delta}{\gamma}$ stays nearly constant at 2 and $\alpha$ is near unity. The constant $c$ is slightly higher than 0.4 . Comparing (14) and (15) it can be seen that by adding inductor to the source, it is possible to bring $Z_{opt}$ close to $Z_{in}^{*}$ while causing no degradation to $\mathrm{F_{min}}$ and $\mathrm{R_n}$.

$$\mathrm{Re}[Z_{opt}]=\mathrm{Re}[Z_s]$$

b)For transistor with certain gate width or $C_{gs}$, inductor $L_s$ is selected such that

$$Im[Z_{opt}]=-Im[Z_s]$$

c)Having $C_{gs}$ and $L_s$, then $V_{GS}$ is chosen to satisfy eq. (20).

Input impedance for Fig. 4 is given by:

$$Z_{in}=\frac{g_m L_s}{C_{gs}}+sL_s+\frac{1}{sC_{gs}}=L_s\omega_T+sL_s+\frac{1}{sC_{gs}} \quad (14)$$

The condition for minimum noise and maximum gain (simultaneously noise and gain match) is as follow:

$$Z_{opt}=Z_{in}^{*} \quad (16)$$

Using $Z_{opt}=Z_s=Z_{in}^{*}$, the condition for gain and noise match can be written as follows:

$$\mathrm{Re}[Z_{opt}]=\mathrm{Re}[Z_s] \quad (17)$$

$$\mathrm{Im}[Z_{opt}]=\mathrm{Im}[Z_s] \quad (18)$$

$$\mathrm{Im}[Z_{in}]=-\mathrm{Im}[Z_s] \quad (19)$$

$$\mathrm{Re}[Z_{in}]=\mathrm{Re}[Z_s] \quad (20)$$

As mention earlier, based on (14) and (15) Eqs. (18) and (19) are the same. Therefore (19) can be ignored considering the importance of noise performance.

Now, from (11) to (14), the design parameters which can satisfy (17), (18) and (20) are $V_{GS}$, gate width , $W$ (or $C_{gs}$) and $L_s$. To increase cut-off frequency of transistor the minimum gate length should be chosen for transistor. Therefore for certain value of $Z_s$, one should solve Eqs., (17), (18) and (20) as three equations with three unknowns. Hence the procedure for designing an amplifier with minimum noise and maximum gain can be summarized as follows:

a) For arbitrary source impedance $Z_s$, gate width $W$ (or $C_{gs}$) is chosen in order to satisfy

d)Note that, as discussed above, for the given $L_s$ , the imaginary value of the optimum noise impedance would automatically be approximately equal to that of the input impedance with an opposite sign($Im[Z_{opt}]=-Im[Z_s]$).

## 3. Low Noise Amplifier Design

Based on the above procedure, a low noise amplifier has been analyzed and designed. The input/output matching elements and transistor gate width are obtained based on the simultaneous power and noise match conditions. To model transmission line implemented in the amplifier design, the measured S-parameters of the line are first converted to Y- parameters. Then element values in Fig. 5 are calculated by minimizing the difference between converted and modeled Y- parameters**.** The software used to simulate the amplifier performance is Advance Design system (ADS)

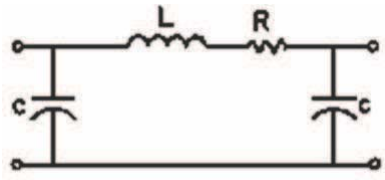


Fig. 5. The lossy transmission line model [11].

To obtain the transistor model we implement small signal model of a single gain cell as shown in Fig. 6. The intrinsic elements of the model can be easily found using the same procedure as implemented for transmission line extraction. As the measured S-parameters are obtained in term of gate width of the transistor, W, the model element value are also extracted versus W.

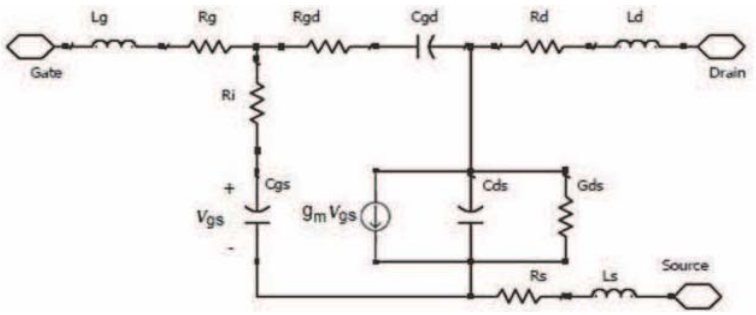


Fig. 6. The small signal model of a common source transistor at millimetrewave. [10]

The advantage of this scalable model is the possibility to include the gate width of the transistor as an important parameter in the amplifier design optimization.Fig. 7 depicts the input/output stability factors of the gain cell. As can be seen from Fig. 7, the amplifier is highly stable.

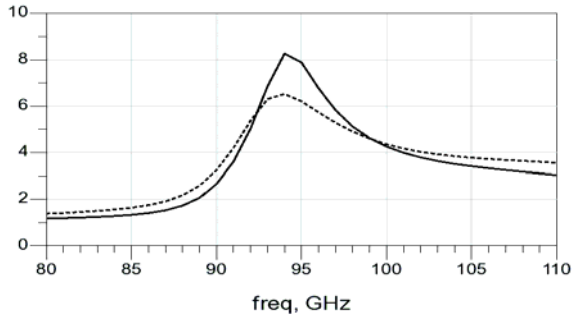


Fig. 7 Input (dotted line) and output (solid line) stability factors

To increase gain of designed amplifier, 5 single gain cell are cascaded as shown in Fig. 8.

Fig. 9 shows the S-parameters of the designed amplifier for $V_g = 0.7V$ and $V_d = 1.7V$ . The amplifier consumes 85mW DC power in this bias condition. As can be seen from Fig. 8, gain and input/output return loss are better than 18dB and 20dB respectively which shows excellent input/output match.

Fig. 10 shows the noise figure and minimum noise figure of the designed amplifier. As can be seen from this figure, the noise figure is quite close to minimum noise figure which shows a very good noise match for a designed amplifier. The noise figure is 7.4dB at 94GHz which is the best value reported in this frequency band so far.

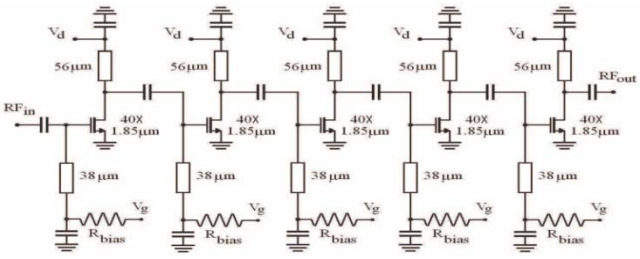


Fig. 8 Designed 5 stage cascaded amplifier

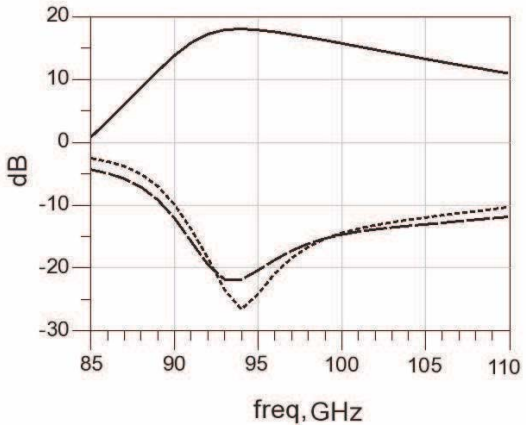


Fig. 9 Gain (solid line), input return loss(dotted line) and output return loss (dashed line) for the designed amplifier.

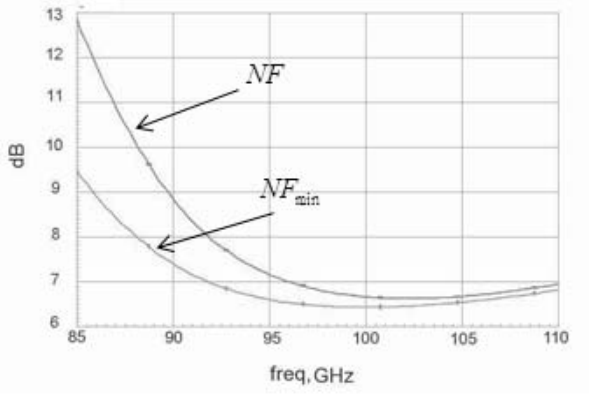


Fig. 10 Noise figure and minimum noise figure of the amplifier.

It should be mentioned that the design procedure at 94 is more complicated than that of thelow frequency due to the high number of parasitic elements should be used to model the amplifier at 94 GHz. Atthe high frequency, the assumption of unilateral model is no longer valid and bilateral small signal model should be used in the amplifier analysis. It is also worth to mention that as the model has been obtained at high frequency and noise matched was performed for this frequency range, the low frequency noise figure is not close to $NF_{min}$ as it is evidence from Fig. 10.

## 4. Conclusion

A 5-stage cascaded amplifier at W-band in 0.13-µm CMOS technology was analyzed and designed using common source topology. Gain and noise figure of the amplifier have been optimized by proper choice of input/output matching circuit elements and transistor gate width and also simultaneously match gain and noise procedure. The designed amplifier is highly stable without using inductive source degeneration. The simulation results show a gain of better than 18dB and noise figure of 7.4dB at 94GHz while input/output return losses are better than 20dB. This is the highest frequency of operation for an LNA reported in the literature using0.13-µm CMOS technology**.**

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