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(Research paper)

30 GHz Bandwidth 0.18µm-CMOS Cascaded Differential Distributed Amplifiers

Massomeh Ghaleh Agha Babaei, Majid Babaeinik*[1]

Department of Electrical Engineering, Semnan Branch, Islamic Azad University Semnan, Iran

babaei.masi@gmail.com, m.babaeinik@semnaniau.ac.ir

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*Corresponding Author's Email Address:
m.babaeinik@semnaniau.ac.ir

Abstract

One of the most important things in designing modern telecommunication systems is the need to increase data transfer speeds. Increasing the transmission speed requires a wider bandwidth and work in a higher frequency range, and this has led to more attention to broadband circuits. For applications with a bit rate of 40 Gb/s, the bandwidth required for the amplifier is 28GHz. For this purpose, in this paper, 30GHz broadband amplifiers are designed. In this paper, 5 amplifiers with distributed cascade pseudo-differential topology with cascade classes of 2 to 6 stages in which there is only one gain cell in each floor are designed. The proposed circuits were implemented in RF_CMOS 0.18 µm technology and simulated in ADS software. The compromise of the parameters is in favor of the 4-stage amplifier. In this amplifier, the voltage gain in the 30GHz bandwidth is 25dB, while other scattering parameters are below 10dB. Power consumption is 162mW and chip area is 0.74mm2 and noise figure is 5dB, which are good results compared to other designs.

Introduction

With the increasing demand for the capacity of optical telecommunication systems, the demand for sending data has increased from 10Gb/s (for PDH transmission systems) to 40Gb/s (SDH transmission systems) and even higher than 100 Gb/s. In urban communication, the data rate of 40 Gb/s (SDH systems) is used, which depending on the type of modulation that is done on the line, the number of different channels can be defined. [1]

It is shown that the optimal bandwidth for the transmission impedance amplifier is approximately 0.7 times the bit rate of the system. Therefore, for SONET OC-768 applications with a bit rate of 40 Gb/s, the bandwidth required for the amplifier is 28GHz. [2]

Therefore, an amplifier with a bandwidth of 30GHz is used as a broadband amplifier in the receiver of an optical transmission system.

The methods and designs that are used in the design of broadband amplifiers are as follows: compensator matching method, active matching method, feedback amplifier, TIS/TAS amplifier, balanced amplifier and Distributed Amplifier (DA). Table 1 shows a comparison of broadband amplifiers. As can be seen, the distributed amplifier has major advantages such as high bandwidth, compared to other broadband amplifiers, while optimally maintaining other parameters of the broadband amplifier.

[1] Corresponding author: Majid Babaeinik, m.babaeinik@semnaniau.ac.ir

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Table1: comparison of wideband amplifier approach

Topology	BW	Gain	Impedance matching	Stability	Noise	Output Power	Power consumption	Area
Resistive matching	Moderate	Low	Tradeoff with gain and noise	Very High	High	limited by the output resistance	Moderate	Very compact
Active matching	High	High	Good	can be critical in non-differential circuits and feedback	Low	Limited	High	compact
TIS-TAS	High	Moderate	Good	Good	Moderate	Moderate	Moderate	Very compact
Balanced amplifier	Moderate	Low due to losses of couplers	Good - depending on the coupler bandwidth	Good	Relatively low	Good	Moderate	Large
Distributed amplifier	Very High	Low but can be cascaded	Good	High	Relatively low	Good	Very High	Very large

Due to the advantages of distributed amplifiers, they can be used as broadband amplifiers for the mentioned purposes.

I. Distributed amplifiers (DA)

Reducing the effect of transistor capacitors on T-shaped lines is a major goal of DA amplifiers in order to increase amplifier bandwidth. Figure 1 shows the arrangement of a DA amplifier with artificial lines, which is the most common type.

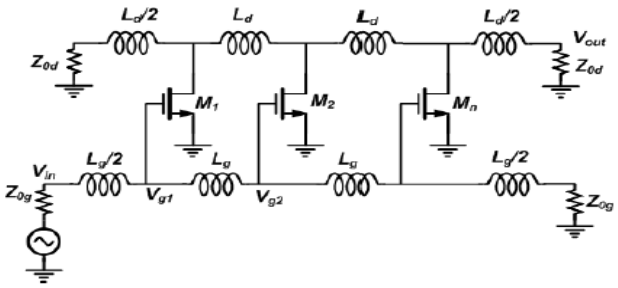

Figure 1: Schematics of DA amplifier with artificial lines

The values Zod and Zog are the characteristic impedance of the drain and gate lines, respectively. To obtain the impedance matching, these impedance characteristics are obtained as follows:

$$Z_{0d} = \sqrt{\frac{L_d}{C_d + \frac{C_{ds}}{l_d}}} \quad ; \quad Z_{0g} = \sqrt{\frac{L_g}{C_g + \frac{C_{gs}}{l_g}}}$$

The power gain is obtained as follows:

$$G_P = \frac{1}{4} n^2 g_m^2 R_{0g} R_{0d} e^{-2n\alpha_g(\omega)} \frac{1}{1 - \left(\frac{\omega}{\omega_c}\right)^2}$$

Where αg is the line propagation coefficient, ωc is the cutoff frequency and Ziπ is the line image impedance. In this case, artificial transmission line is lossless and the gain and cut-off frequency can be obtained as:

$$|A_v| = \frac{1}{2} n g_m Z_{0d}$$

$$f_c = \frac{1}{\pi\sqrt{l_g C_g}} = \frac{1}{\pi\sqrt{l_d C_d}} = \frac{1}{\pi Z_0 C_0}$$

Many studies have been done on distributed amplifiers, some of which are categorized in the table 2, [3-16].

Table2: comparison of distributed amplifier topology

Method	Advantage	Disadvantage
Increasing gain	Increase gain	Increase power consumption and reduce bandwidth
Cascode	Increase bandwidth	It is often considered as part of the design to improve performance
Cascade	Increase gain	Increase power consumption
Matrix DA	Increase gain	Increase power consumption and increase circuit dimensions
CMSDA	Increase gain and bandwidth	Increase power consumption and increase circuit dimensions
HPDA	EMC less than the LP structure	Lack of high bandwidth
DA based on	Achieve lower impedances	Reduction of bandwidth

integrated transformer	at input and output	by transformer inductors
DDA	Improve bandwidth performance	Increase chip area and power consumption
DDA with active balloon	Provides the conditions for using the DDA topology	Increase power consumption and reduce bandwidth
PDDA	increasing bandwidth	Low voltage gain
DA with Darlington	Improved bandwidth	Low voltage gain
Tapered DA	Gradual decrease in impedance	Output matching
DA with negative resistance	Compensation for the effect of series resistors at high frequencies	Increase power consumption and increase chip level
DA with negative capacitance	increasing bandwidth	Increase power consumption and increase chip level

Circuit Design

Differential amplifier, due to its advantages, can provide suitable performance parameters for the amplifier, including bandwidth gain performance. In general, the advantages of differential amplifier are as follows: high voltage gain, differential input, good bias stability, suitable parameters for placement inside the chip, low noise, DC amplifier, and appropriate bandwidth. So differential amplifiers can be a good choice for gain cells in distributed amplifiers

Figure 2 shows the design of DA amplifier structure with pseudo differential amplifier. In this circuit, the m1 and m2 are differential pair and m3 is a current source for biasing transistors m1 and m2. This amplifier has been designed and simulated in TSMC 0.18-µm RF-CMOS technology

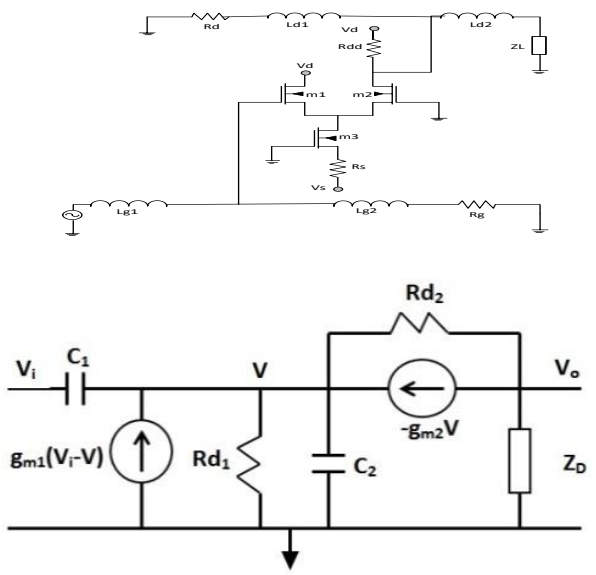

Figure 2: Schematics of PDDA, and small signal circuit of PDA

The voltage gain of PDA is given by [4].

$$\frac{V_O}{V_i} \approx \frac{g_{m2}(g_{m1} + SC_{gs1})}{\left[\frac{1}{r_{d1}} + S(C_{gs1} + C_{gs2}) + \frac{1}{r_{d2}} + g_{m1}\right]} (r_{d2} \parallel Z_D)$$

If $g_{m1} = g_{m2} = g_m$; $r_{d2} >> Z_D$ and $\frac{1}{r_{d1}} + \frac{1}{r_{d2}} << g_{m1}$

Then

$$A_V(0) \approx g_m \cdot Z_D$$

The S parameter for pseudo differential amplifier is given by

$$[S]_{PDA} = \begin{bmatrix} 1 & 0 \\ \frac{2g_{m1}g_{m2}}{g_{m1} + g_{m2}} & 1 \end{bmatrix}$$

For cascaded pseudo distributed differential amplifier (CPDDA), which consist of m cascaded PDDA with n stages, the voltage gain is obtained as [5]:

$$\left|A_{v(0)}\right|_{cascade} = \left(\frac{1}{2} n g_m R_{0d}\right)^m$$

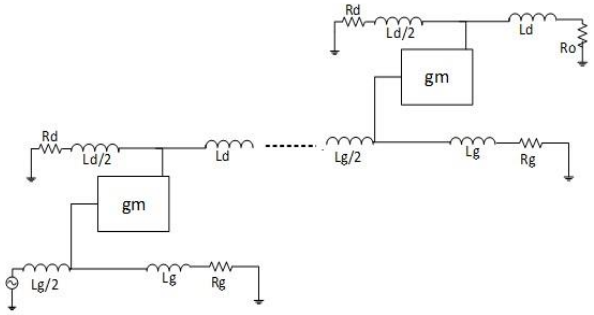

Figure3: cascaded pseudo distributed differential amplifier (m-Stages)

In our proposed circuit as shown in Figure 3, each DA

consists of only one amplifier cell, so n = 1. But the numbers of m distributed amplifiers are cascaded.

$$|A_{v(0)}|_{cascade} = \left(\frac{1}{2} g_m R_{0d}\right)^m$$

In this paper, circuits with m = 2 to m = 6 are designed and simulated.

Simulation

The 5 CPDDA with 2 to 6 cascaded PDDA are designed in CMOS technology and simulated by ADS software in TSMC-0.18µm-RF design kit. Figure 4 shows CPDDA (2-Stages cascade) in TSMC_RF_CMOS 0.18µm. Other amplifiers have the same parameters and only the number of cascaded stages is different.

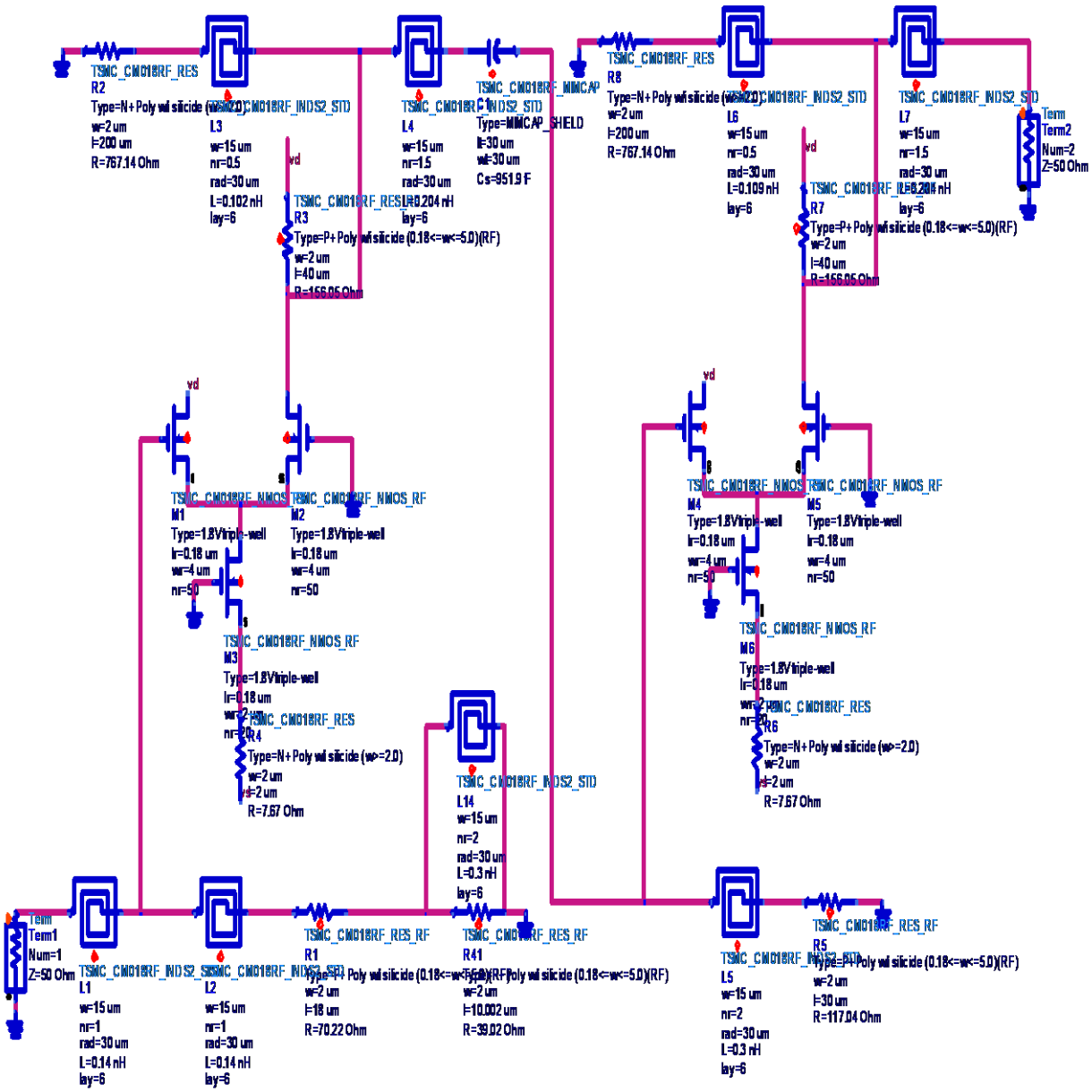

Figure 4: CPDDA (2-Stages cascade) in TSMC_RF_CMOS 0.18µm

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The results of all 5 CPDDA are investigated and compared. As can be seen in this amplifier S21 is differing from 12dB to 38dB with 30GHz bandwidth for 2 to 6 cascaded stages. The frequency response is flat in the number of cascade stages 2 to 4, but when the cascade stages are greater than 4, the frequency response will not be flat.

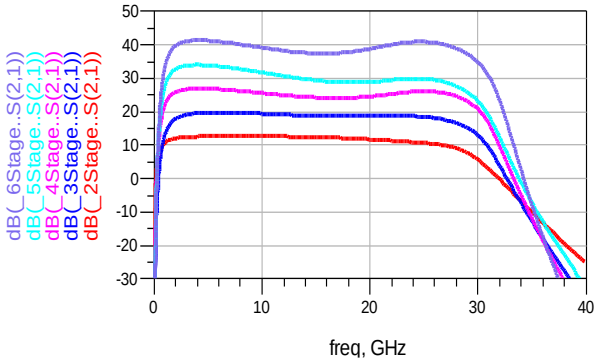
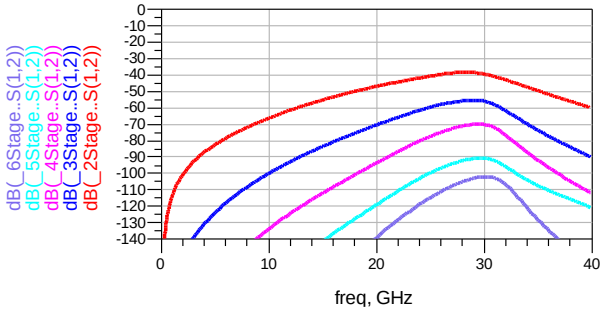
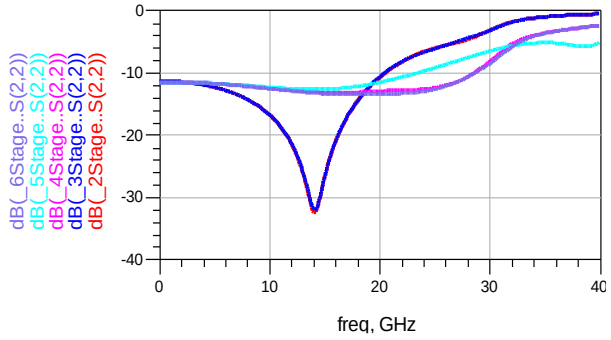


Figure 5: S21 for CPDDA (2 to 6 Stages cascade)

The results of other scattering parameters of this amplifier are shown in Figure 6. However, all amplifiers have acceptable results, but the 4 to 6 cascade amplifiers have better scattering parameters than 2 and 3 cascade amplifiers.





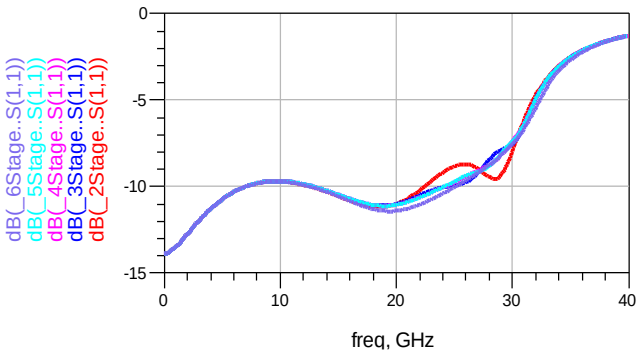


Figure 6: S11, S12, and S21 for CPDDA (2 to 6 Stages cascade)

Stability factor and Noise figure for CPDDA (2 to 6 Stages cascade) are shown in figure 7. All amplifiers are stable and have a similar noise figure of 5dB.

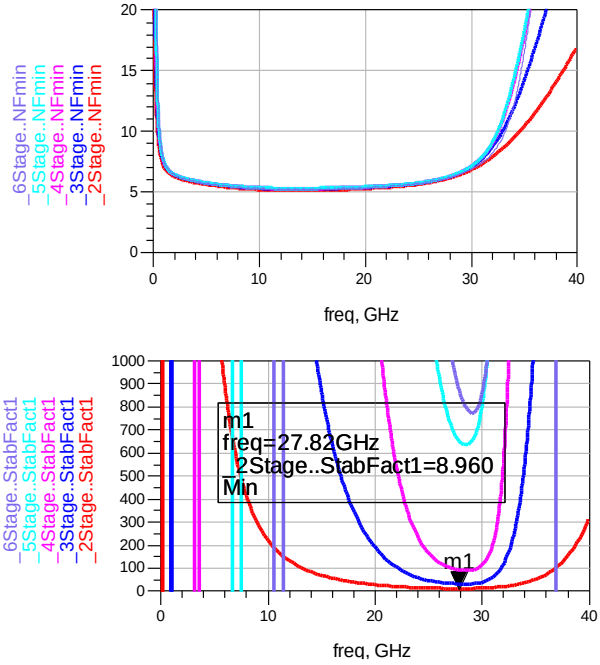


Figure 7: Stability factor and Noise figure for CPDDA (2 to 6 Stages cascade)

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Table3: Performance of the last reported DAs and this work

References	Gain (dB)	BW (GHz)	S11 (dB)	S22 (dB)	NF (dB)	Pdc (mW)	Area (mm2)	Technology
[4]	6.4	0-40	<-16	<-12	4.27	115	0.27	0.18 µm CMOS
[5]	10	0-40	<-12	<-10	4.6	230	0.58	0.18 µm CMOS
[6]	29.4	7.5	< -8	< -10	2.93	61	-	0.13 µm CMOS
[9]	10.7	36.4	< -10	< -4.6	3.8	28.8	0.67	90 nm CMOS
[10]	14	3-10	< -18	< -18	1.95	26	-	0.13 µm CMOS
[11]	24	33	< -10	< -10	6.5-7.5	238	0.83	0.18 µm CMOS
[12]	25	1.5 - 35.5	< -10	< -10	6.5-8	176	0.86	0.18 µm CMOS
[13]	10.5	0-10.5	-	-	3.2	29	-	0.18 µm CMOS
[14]	17.1	1.5 - 8.2	< -11	< -10.1	3.52	46.85	-	0.18 µm CMOS
This work-2Stage	12	1-31	< -8	< -8	5	81	0.37	0.18 µm CMOS
This work-3Stage	19	1-31	< -10	< -8	5	122	0.56	0.18 µm CMOS
This work-4Stage	25	1-31	< -10	< -10	5	162	0.74	0.18 µm CMOS
This work-5Stage	30	1-31	< -10	< -10	5	203	0.96	0.18 µm CMOS
This work-6Stage	38	1-31	< -10	< -10	5	244	1.13	0.18 µm CMOS

The comparison results of this design with other designs presented in other articles are summarized in the table 3. With the results obtained from this table, it can be seen that the proposed 4-cascaded amplifier has a good and optimum performance.

Conclusion

In this paper, distributed amplifiers were introduced as broadband amplifiers. Distributed pseudo-differential cascade amplifier was introduced and various designs for high bandwidth and high gain were presented and simulated.

The 5 CPDDA with 2 to 6 cascaded stages were designed and simulated by ADS software in TSMC-0.18µm-RF design kit and the results were reviewed and compared.All amplifiers were stable and had a bandwidth of 30GHz and had acceptable parameters S11, S12, S22. Increasing the number of cascade stages of amplifiers leads to an increase in voltage gain but also increases power consumption and chip area. An optimal choice is a CPPDA with 4 cascading stages. In this amplifier, the parameters S11 and S22 are less than -10dB. The noise figure is 5, the power consumption is 162mW and the chip area is 0.74mm2.

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