Design of a Digital Sigma Delta Modulator with Separate Pipeline Lines for Fractional Frequency Synthesizers

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ABSTRACT:
Digital Sigma Delta Modulator architecture is widely used in fractional frequency synthesizers. A frequency synthesizer is a major component of wireless communication systems. The output of the frequency synthesizer system is locked based on the phase lock loop at a specific reference frequency. In this case, the output frequency is the same as the oscillator frequency of the VCO. The main advantage of digital sigma delta modulator with multi-layer structure is its ability to be implemented as a pipeline. This method will reduce the delay and increase the sampling frequency. In this paper, a digital sigma delta modulator of separate lines is designed by pipeline method and its power spectral density is plotted. This method increases the speed of the modulator and reduces the hardware consumption.

KEYWORDS: Digital Sigma Delta Modulator, Pipeline Method, Hardware Consumption, Speed.

1. INTRODUCTION

Synthesizer circuits are divided into two categories: integer and fractional frequency. The structure of the integer frequency synthesizer is shown in Fig.1, in which the input frequency divider is removed for simplicity. The reference frequency corresponds to the input frequency of the phase detector. In a integer synthesizer, the relationship between the reference frequency and the output frequency is (1). These types of synthesizers produce a frequency called f_{out}.

$$f_{out} = N.f_{ref} \quad (1)$$

Where N is the division ratio and is a positive integer. Frequency accuracy is equal to f_{ref}. The error signal is generated by a phase detector with a cycle length of $1/f_{ref}$, which is called the reference tones. To reduce these tones, the bandwidth of the loop filter must be much smaller than f_{ref}. Therefore, first, the temporal response of the loop is relatively low. Second, the energy-saving elements in the loop filter are physically large.

These integer synthesizers are widely used in telecommunication systems. But these structures have disadvantages. Among the frequency accuracy of these synthesizers is very limited. That is, only integers multiplied by the reference frequency can be synthesized. Stability requirements limit the bandwidth of the loop. As the reference frequency decreases, the sitting time increases and the loop bandwidth lessens. Also, reducing the bandwidth increases the noise of the oscillating phase. In addition, in these integer synthesizers, whenever the division ratio increases, there is a trade-off between phase noise and settling time. In these phase lock loop circuits, the phase noise of all parts of the circuit is multiplied by the division ratio. In order to increase the output frequency accuracy, the input frequency must be low and the division ratio high. This large division ratio increases the bandwidth noise.

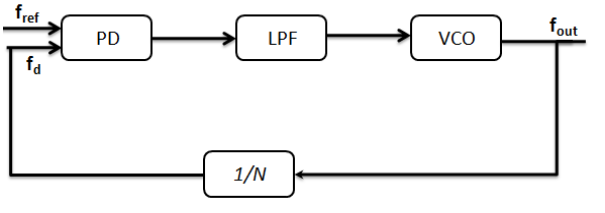

Fig. 1. Integrated phase lock loop (PLL) structure.

In integer frequency synthesizers, integer multiples of the reference frequency can be synthesized, so the reference frequency and the bandwidth of the loop can be increased. This frequency synthesizer is commonly used due to its flexibility and convenient frequency adjustment. The output frequency is divided by an

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integer number and locked with the reference frequency and a fractional frequency multiplier is obtained. This will be done by dividing the frequency by different integers in each cycle length. The output frequency is equal to the product of the average value of the division ratio at the input reference frequency. This type of synthesizer has many benefits. Including: Larger reference frequency reduces lock time. The wider the bandwidth of the loop, the less bandwidth noise will be reduced, and the reference tones are far away and are eliminated by the low-pass filter. [1]- [4] However, the divider cannot be synchronized with the reference frequency in each cycle length, so this additional division ratio at each cycle length will cause quantized noise and spurious tones around the carrier frequency. These only appear at the output. At low fractional frequencies, these spurious tones are in the base band and will increase the phase noise.

In Fig.2, the feedback path divider number with frequency f_s is represented. The implementation of this multiple divider is shown in Fig.3. This circuit includes the Sigma Delta modulator with input N_1, module M_1, and output Y_1. The average output value is $\frac{N_1}{M_1}$. The relationship between the output frequency and the reference in the fractional frequency synthesizer is (2).

$$f_{VCO} = \left(N_0 + \frac{N_1}{M_1}\right).f_{PD} \quad (2)$$

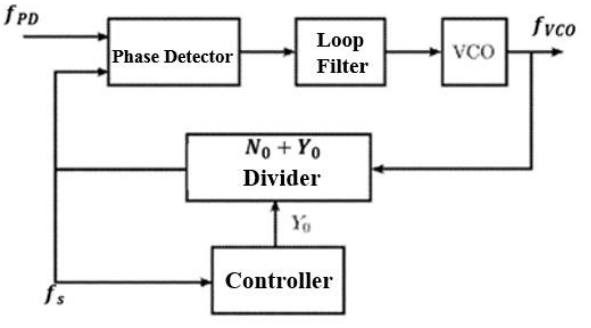


Fig. 2. Fractional frequency synthesizer structure with division ratio controller.

In the fractional frequency synthesizer, the division ratio is controlled by the Sigma Delta modulator. Usually M_1 is a large multiple of 2 and N_1 and N_0 are positive integers. The frequency accuracy is equal to the following equation.

$$f_{res} = \frac{f_{PD}}{M_1} \quad (3)$$

Therefore, frequency accuracy in fractional frequency synthesizers with M_1 factor has decreased. Advanced frequency synthesizers require a high f_{PD} to switch quickly and reduce phase noise. The M_1 synthesizer module needs to be increased to improve system performance.

Each fractional frequency synthesizer uses a digital sigma delta modulator. The first sigma delta pipeline modulator will be used to receive the digital signal. The second sigma delta modulator is used to receive part of the digital signal. Therefore, we will use the structure of separate lines in which low-value bits of the signal are inserted into the first modulator and the result is combined with the valuable bits of the signal and entered into the second-order modulator. In some cases, the nested pipeline structure will use separate lines in which the signal bus is divided into more than two parts. Therefore, with increasing f_{PD}, the speed will increase and the update rate of the fractional synthesizer will increase. By combining the properties of line splits and pipelining in fractional synthesizers, a division with a higher update rate and longer word length will be possible. As the update rate increases, the reference frequency increases, the loop filter and split ratio become smaller, and the phase noise decreases. As the word length increases, the module becomes larger and the reference frequency accuracy increases. The speed of each sigma delta digital modulator is based on when the slowest calculations are used to add two binary numbers. The modulus of the modulator is $M_1 = 2^N$, where N is the number of bits. The speed of each modulator is determined by the intrinsic speed of the f_{max} technology and the bit width N.

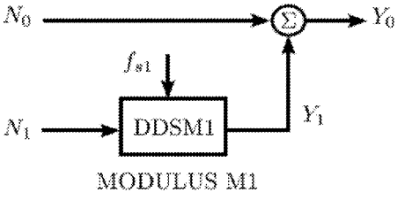


Fig. 3. Division ratio control method with digital sigma delta modulator/

2. LITERATURE REVIEW

MASH modulators are the simplest to configure, as they can only be implemented using adders and registers. In these structures, the accumulator units are cascaded together and the output of each stage will be fed into the noise cancellation network. Therefore, the quantized noise of the last stage accumulator will remain, which is formed according to the order of the modulator. Also, the signal transform function does not depend on the input. This structure is inherently stable and includes the dynamic range of all input quantization surfaces. The only drawback of this architecture is the possibility of creating spurious tones due to the intermittent output behavior. This feature will be further reviewed and eliminated.

These modulators use multi-stage noise shaping. Therefore, the order of modulators can be less. One method is to cascade lower-order modulators, such as first-order ones. For example, a multi-level modulator of order *l* arises from *l* of the first-order modulator

stage. A third-order modulator, for example, is a cascade of three first-order modulators called a 1-1-1 MASH structure. The main advantage of MASH modulators over single stage modulators is that they are progressive and stable. In addition, in a MASH sigma delta modulator, the input stability range is equal to the full-scale state, but in a single-stage structure, it is equal to a fraction of it. These modulators are widely used in N-bit fractional frequency synthesizers.

Fig.4 shows a block diagram of a conventional MASH 1-1-1 sigma delta modulator. Its output relationship is as follows:

$$Y(z) = STF(z).X(z) + NTF(z).E_{q3}(z) \quad (5)$$

The output of this MASH 1-1-1 modulator is as follows.

$$Y(z) = \frac{1}{M}.X(z) + (1 - z^{-1})^3 E_{q3}(z) \quad (6)$$

Therefore, the quantization noise components E_{q1}, E_{q2} are removed and the source component E_{q3} is formed with a third-order $(1 - z^{-1})^3$ high pass filter. Digital sigma delta modulators are used in digital to analog convertors and synthesizers.

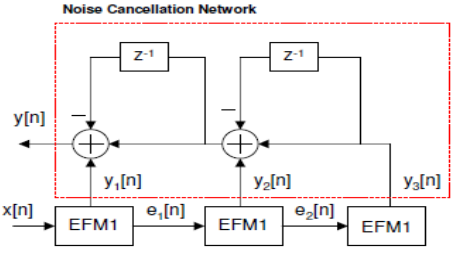


Fig. 4. Block diagram of the conventional MASH 111 DDSM [5].

3. PIPELINE NESTED SEPARATE LINE METHOD

References [5]-[7] provide a design method for digital sigma delta modulators. This method is based on separate lines and is applied to digital sigma delta modulators with dither signal, without it and fixed inputs. The rules for selecting the appropriate word length for modulators are stated to compare the efficiency of the power spectral density modulator of individual lines with conventional modulators and to reduce its hardware. In them, the digital input is divided into several sections; low-value bits will be applied to lower-order modulators, and then recombined with valuable bits. [8]- [11]

Fig.5 shows the structure of a third-order digital sigma delta modulator with separate nested lines as MASH 1-2-3. In this form, the digital input word is first divided into two parts, the N_{MSB} number of valuable bits and the rest of the bits. Then again the rest of the bits are divided into two parts, N_{ISB} number of middle bits and N_{LSB} number of low value bits. N-bit input can be expressed as (7).

$$X = X_{MSB}.2^{N_{LSB}+N_{ISB}} + X_{ISB}.2^{N_{LSB}} + X_{LSB} \quad (7)$$

Where

$$N = N_{LSB} + N_{ISB} + N_{MSB} \quad (8)$$

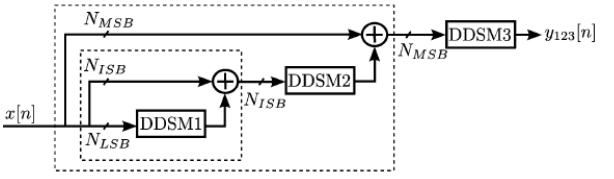


Fig. 5. the structure of third-order nested modulator as 1-2-3 MASH [5]

The output of the third-order nested separate line modulator 1-2-3 in the z-domain is expressed as (9).

$$Y_{123}(z) = \frac{X(z)}{2^N} + \frac{1}{2^{N_{ISB}+N_{MSB}.2^{N_{LSB}}}}(1 - z^{-1}).E_1(z) + \frac{1}{2^{N_{MSB}.2^{N_{ISB}}}}(1 - z^{-1})^2.E_2(z) + \frac{1}{2^{N_{MSB}}}(1 - z^{-1})^3.E_{123}(z) \quad (9)$$

Where E_1, E_2, E_{123} are the quantization errors of sigma delta modulators of order one to three. In this relation, the quantization errors of the sigma delta modulators of the first and second order are, but the end of the relationship is similar to the conventional relationship with the third-order digital sigma delta modulator.

The output of the digital nested sigma delta modulator includes the E_1 shaped noise, which is scaled by a factor of $\frac{1}{2^{N_{MSB}+2^{N_{ISB}}}}$ and the second-order E_2 noise scale, which is scaled by a factor of $\frac{1}{2^{N_{MSB}}}$.

The next section describes how to select the appropriate N_{ISB}, N_{LSB}, and N_{MSB} values to eliminate the middle-class quantization error by the last section.

The output of the three-order separate line modulator as nested 1-2-3 is expressed as (10).

$$Y_{123}(z) = \frac{X(z)}{2^N} + N_1(z) + N_2(z) + N_3(z) \quad (10)$$

Where

$$N_1(z) = \frac{1}{2^{N_{ISB}+N_{MSB}.2^{N_{LSB}}}}(1 - z^{-1}).E_1(z) \quad (11)$$

$$N_2(z) = \frac{1}{2^{N_{MSB}.2^{N_{ISB}}}}(1 - z^{-1})^2.E_2(z) \quad (12)$$

$$N_3(z) = \frac{1}{2^{N_{MSB}}}(1 - z^{-1})^3.E_{123}(z) \quad (13)$$

N_1 is quantization noise in the first-order modulator, N_2 is quantization noise in the second-order modulator, and N_3 is quantization noise in the third-order modulator. It is assumed that all quantization noises are modeled with collectible white sources. Therefore, the power spectral density N_1, N_2, N_3 is (14)-(16).

$$S_1(f[k]) = \frac{1}{12L_1}\left(\frac{1}{2^{N_{ISB}+N_{MSB}}}\right)^2 |1 - z^{-1}|^2_{z=e^{j2\pi k/L_1}} \quad (14)$$

$$S_2(f[k]) = \frac{1}{12L_2}\left(\frac{1}{2^{N_{MSB}}}\right)^2 |(1 - z^{-1})^2|^2_{z=e^{j2\pi k/L_2}} \quad (15)$$

$$S_3(f[k]) = \frac{1}{12L_3}|(1-z^{-1})^3|^2_{z=e^{j2\pi k/L_3}} \quad (16)$$

Where L_1, L_2, L_3 are the cycle length of quantization noise signals of sigma delta modulators of order one to three, which are $2^{N_{LSB}}$ and $2^{N_{LSB}+N_{ISB}}$, $2^{N_{LSB}+N_{ISB}+N_{MSB}}$, respectively.

In a digital Sigma delta modulator with L_s cycle length, the lowest frequency tone is at $\frac{f_s}{L_s}$. Therefore, since the cycle length of N_1, N_2 is equal to $2^{N_{LSB}}$ and $2^{N_{LSB}+N_{ISB}}$, respectively, so the lowest frequency tone in the spectrum N_1, N_2 is equal to $\frac{f_s}{2^{N_{LSB}}}, \frac{f_s}{2^{N_{LSB}+N_{ISB}}}$. In addition, at the output of the three-stage nested 1-2-3 modulator, since S_1, S_2 are formed first and second order, and S_3 is formed third order, if the lowest frequency tones S_1, S_2 are below S_3, then all tones S_1, S_2 will be below S_3. Therefore, it can be expressed (17)-(18).

$$s_1 < s_3, f = \frac{f_s}{2^{N_{LSB}}} \quad (17)$$

$$s_2 < s_3, f = \frac{f_s}{2^{N_{LSB}+N_{ISB}}} \quad (18)$$

Since

$$|1-z^{-1}|^2 = \left|1-e^{\frac{-j2\pi f}{f_s}}\right|^2 = |2\sin\left(\frac{\pi f}{f_s}\right)|^2, \sin\left(\frac{\pi f}{f_s}\right) \approx \frac{\pi f}{f_s} \quad \text{for } f \ll f_s \quad (19)$$

Therefore, at low frequencies, S_1, S_2, S_3 can be approximated as follows.

$$S_1 = \frac{1}{12L_1}\left(\frac{1}{2^{N_{ISB}+N_{MSB}}}\right)^2 2^2 . \left(\frac{\pi f}{f_s}\right)^2 \quad (20)$$

$$S_2 = \frac{1}{12L_2}\left(\frac{1}{2^{N_{MSB}}}\right)^2 2^4 . \left(\frac{\pi f}{f_s}\right)^4 \quad (21)$$

$$S_3 = \frac{1}{12L_3} 2^6 . \left(\frac{\pi f}{f_s}\right)^6 \quad (22)$$

By replacing (20)-(22) in (17)-(18):

$$4N_{LSB} - N_{ISB} - N_{MSB} - 4 < 6.6, 2N_{LSB} + 2N_{ISB} - N_{MSB} - 2 < 3.3 \quad (23)$$

Assume that relation (24) is established.

$$L=N_{MSB}, M=N_{ISB}+N_{MSB}, N=N_{ISB}+N_{MSB}+N_{LSB} \quad (24)$$

Therefore

$$4N - 5M - 4 < 6.6, 2N - 3L - 2 < 3.3 \quad (25)$$

If the input word length is given, M, L can be calculated with (26).

$$M = \left\lfloor\frac{4N-10.6}{5}\right\rfloor, L = \left\lfloor\frac{2N-5.3}{3}\right\rfloor \quad (26)$$

Therefore, the optimal values for N_{LSB} and N_{ISB}, N_{MSB} will be calculated with (27).

$$N_{MSB} = L, N_{ISB} = M - L, N_{LSB} = N - M \quad (27)$$

4. RESULTS AND DISCUSSION

Fig. 6 shows the output power spectral density of this modulator as separate lines. In this figure, the terms S_1 and S_2 correspond to the first and second modulators. By selecting the appropriate N_{MSB}, N_{ISB} and N_{LSB}, these additional quantization noise components are covered by S_3. In this case, the performance of the spectrum remains unchanged. But the maximum N_{MSB}, N_{ISB} and N_{LSB} are less than N. Although using a separate line structure reduces the bit width and increases the modulator update rate, using a pipeline structure will also speed up performance. The output of the third-order sigma delta pipeline modulator is as follows:

$$Y(z) = z^{-1}\frac{X(z)}{M} + (1-z^{-1})^3 E_{q3}(z) \quad (28)$$

Fig.7 shows a diagram of the MASH2, MASH3 modulator pipeline. Fig.8 shows the modulator block diagram of separate nested pipeline lines to maximize the output performance of the sigma delta modulator.

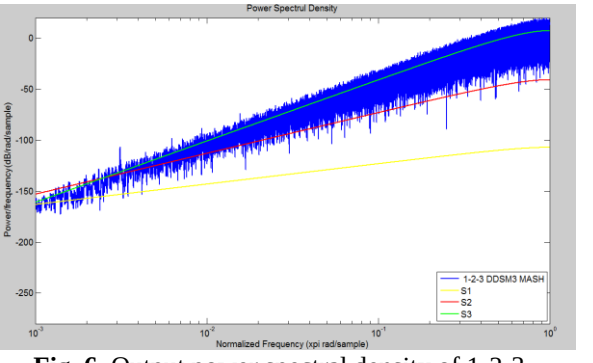
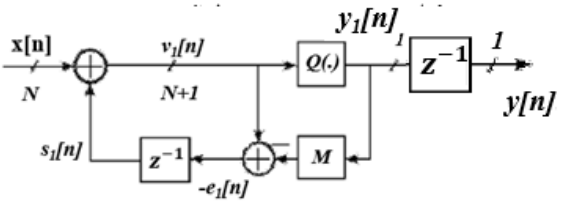
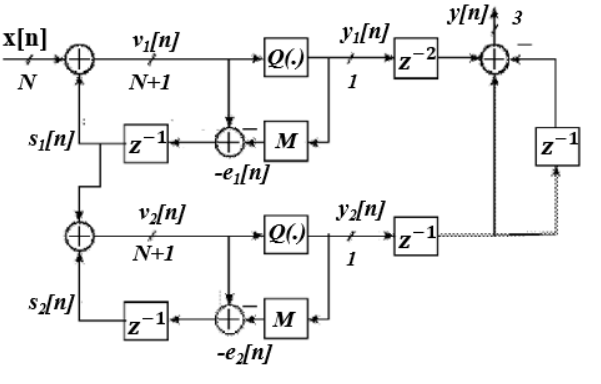


Fig. 6. Output power spectral density of 1-2-3 DDSM3 modulator with nested separate lines.

Fig.9 illustrates the power spectrum of the separate and nested 20-bit MASH modulator, with zero-order dither signal as 7-7-6 bits and pipeline. This range is similar to the conventional MASH modulator, but has only 7 bits.



(a)



(b)

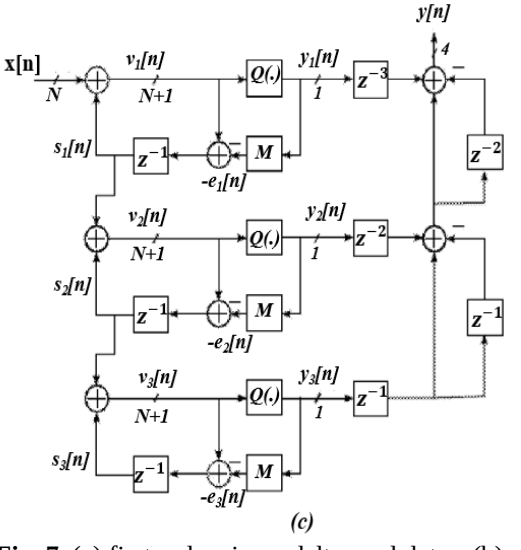


Fig. 7. (a) first order sigma delta modulator, (b) pipeline second order sigma delta modulator, (c) pipeline third order sigma delta modulator.

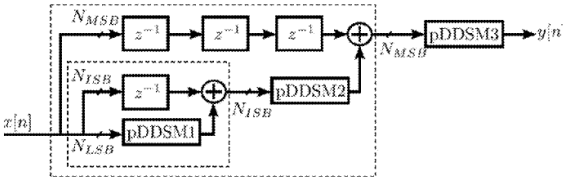


Fig. 8. Block diagram modulator of separate lines nested pipeline.

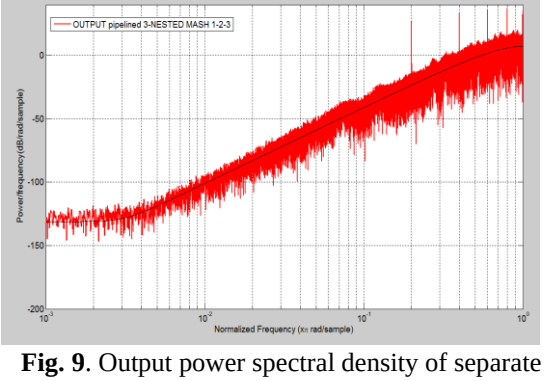


Fig. 9. Output power spectral density of separate line and nested pipeline modulator.

5. CONCLUSION

In this paper, a digital sigma delta modulator with separate nested lines is designed as a pipeline with less hardware and higher speeds. This modulator can be used in fractional frequency synthesizers. The power spectral density of this modulator was simulated with MATLAB, which shows that it has a slight spurious tone.

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