# A Bulk-Driven Variable Gain OTA in 180nm CMOS Technology

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**ABSTRACT:**
In this paper, an operational transconductance amplifier (OTA) is designed, simulated and configured so that input dynamic range is improved by bulk-driven technique of the input transistors. The bulk-driven structure is used in the proposed OTA to stabilize the transconductance and to achieve a high linearity. By changing the control voltage and the input common-mode voltage, the voltages and currents of the circuit are changed so that the transconductance and the voltage gain are changed linearly. Also, setting a reference voltage in the circuit can greatly reduce the destructive effects of undesired changes in the circuit operation during fabrication process. The proposed OTA is designed in 180 nm CMOS technology and required only 0.5 V supply voltage. The simulation results show the OTA voltage gain is varied from 0 dB to 14.2 dB by changing the control voltage from 0 to 0.5 V. Moreover, the input common-mode voltage of the OTA can be changed in the range of 0.125 to 0.375V and without linear degradation. The proposed OTA is dissipated 250 nW and makes it suitable for low-power applications.

**KEYWORDS:** Variable Gain Amplifier, Transconductance Amplifier, VGA, OTA.

## 1. INTRODUCTION

Today, transconductance-based variable gain amplifiers (VGAs) are one of the most widely used circuit blocks in the analog systems. In most of systems interfacing between analog and digital signals, after receiving the analog signal, the amplitude should be increased by an amplifier in order to be accepted by other system blocks. Therefore, considering the signals with different amplitudes, the variable gain amplifier are of particular importance, especially in systems with medical applications and low power. By these amplifiers, the voltage can be changed to the system requirements by changing the control voltage [1], [2].

Variable gain amplifiers are usually configured by several successive stages of OTAs and by connecting the voltage control of the cells to each other, one can change the circuit gain. To achieve a high linearity in the amplifier, OTAs should have a high linearity. In the other word, for control voltage change in a certain range, the voltage gain should decrease or increase linearly. Then, the structure of the cell should be able to provide currents and voltages of the circuit elements, so that by changing the control voltage, no significant nonlinear changes occur in the output parameters [2]. For this purpose, the following factors have been used in the recent studies: structure based on the reference voltage and current mirror amplifier [2], self-driving structures [3], a source degeneration approach [4], current-mode cell [5], the tuning circuits [6], controller feedback [7]. This improves the linearity of the cells.

The input dynamic range (ICMR) of the amplifier is one of the problems to design the systems interface between analog and digital signals. In fact, due to a low supply voltage of these systems, it is expected that the blocks used in the system are able to change the input common-mode voltage. It means that if the common-mode voltage level applied to the input of the variable gain amplifier decreases or increases, the circuit still provides the linearity and the expected operation. To solve such problem in the low supply in which it is not possible to increase the complexity of the circuit, usually the CMOS technology is used in driving the transistor bulk terminals [8]. By applying the input signal to the bulk terminal, one can increase the ability to change the common-mode voltage of the input differential pair because the dependence of transistor current to bulk voltage is much less than the gate terminal voltage. Thus, the change of the voltage applied to the bulk will not have much effect on the current and therefore the circuit operation. The

disadvantage of the approach is to reduce the transconductance of the input differential pair. This is not important in cells because a high voltage gain amplifier can be obtained by putting together several cells [2].

In this study, an OTA is designed based on the self-driving approach as well as the approach of driving the input transistor bulk terminal. Use of such approach leads to a high linearity of the circuit for the control voltage changes. Also, the change of the input common-more voltage has not a significant effect on the circuit operation. The study is organized as follows. In section 2 the proposed OTA is presented. Then, the important analyses such as noise, circulate rate, power supply rejection ratio in output, and common mode rejection ratio in the output will be investigated in the study. In the section 3, the results of the simulation are studied and the performance of the proposed cell is compared with other cells. Finally, in section 4, the conclusion will be presented.

## 2. PROPOSED OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Fig. 1 shows the current mirror amplifier with the approach of driving the bulk terminal. Considering the advantages such as simplicity, capability of self-driving and high input dynamic range, this amplifier is known as the base of the design of many present amplifiers [2]. To design a self-driving circuit in Fig. 1, we should determine voltages of Vb1 and Vb2 applied to the gate terminals of the transistors of M0, M5, M6, M2, M1, so that the voltages have a linear dependence to the circuit changes. Also, a control voltage is required to change the transconductance of the circuit.

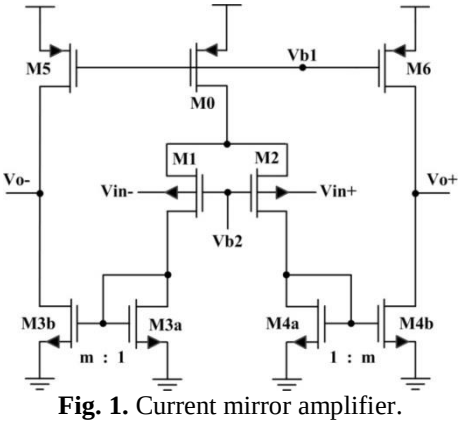


**Fig. 1.** Current mirror amplifier.

Fig. 2 shows the proposed OTA. As mentioned, the transistor of M0 is replaced by the current mirror transistors M5a:M5b and M6a:M6b with a current gain of n. In addition to providing the tuning voltages, adding the current mirrors and M4b and M3b transistors provides a reference voltage to remove or reduce the undesired effects on the circuit operation during the building process. In the other word, if the transistor dimension is changed unintentionally that affects the circuit operation, the reference voltage ($V_{ref}$) of the circuit can be manually returned to the initial state. The reference voltage change lead to change the mirror transistors of M5a:M5b and M6a:M6b and therefore, the current of all branches will be changed. This makes the circuit operation will be recovered and reformed.

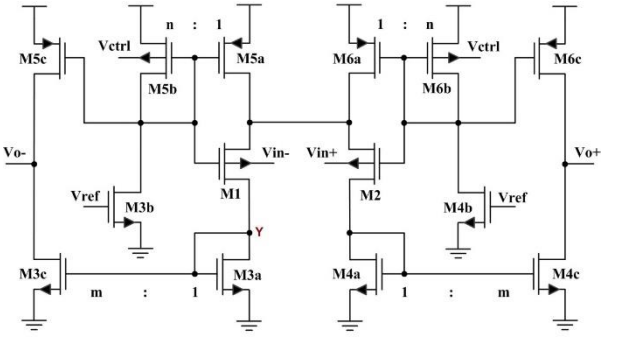


**Fig. 2.** Proposed operational transconductance amplifier (OTA).

To control the transconductance and the voltage gain of the proposed cell, the bulk terminal of the current mirrors of M5a:M5b and M6a:M6b could be an appropriate option. Considering a low effect of the voltage change of bulk of the transistor in the circuit current, it can be expected that by changing the terminal voltage of the mirror transistors, a high voltage range is obtained for linear control of the transconductance. Equation (1) shows the dependence of the transistor current of MOS to the parameters in the weak inversion region (sub-threshold region). This indicates the insignificant effect of the bulk terminal on the current.

$$I_d = I_S \times e^{\left(\frac{V_{GS}-(V_{T0}-(n-1)V_{BS})}{nU_t}\right)}\left(1-e^{\frac{-V_{DS}}{U_t}}\right) \qquad (1)$$

Where $I_s$ and $n$ are current component and slope in the under-threshold region, respectively. $V_{DS}$ and $V_{BS}$ are a drain-source and bulk-source voltage of the transistor.

As shown in Fig. 2, the input signal is applied to the bulk terminal of the differential pair of M1 and M2. As mentioned previously, the approach increases the input dynamic range of the proposed cell. According to (1), the change of the input common-mode voltage (source-bulk voltage of the input transistors) doesn't have a significant effect on the transistor current because the total current of the circuit is determined by the $V_{ref}$. Then, it is expected that the change of the input

common-mode voltage reduces the transconductance of the cell operation. Therefore, the differential voltage gain of the proposed cell is determined by (2). Parameter m is the mirror current gain of M4a:4c and M3a:M3c. Also, $r_0$ and $g_{mb}$ are output resistance and transconductance of the transistor terminal, respectively.

$$A_{V,diff} = m \times gmb_1 \left( r_{o,3c} \left\| r_{o,5c} \right. \right) \quad (2)$$

### 3.1. PSRR and CMRR Characteristics

To study the power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR) in output of transconductance of the proposed cell, we can use the half-circuit model in the Fig. 2. These two characteristics are very important because in amplifiers with a low voltage gain as well as the medical applications in which the input signal amplitude is very low, the ratio of signal to noise is reduced by amplifying the noise of the power supply and the input common-mode signal in the output node. This causes the circuit efficiency is reduced. Therefore, considering the small signal half-circuit model of the proposed cell and applying the signal to the power supply node and applying the common-mode signal to the Vin input, the PSRR and CMRR can be obtained from (3) and (4):

$$\left|PSRR\right| = \left[ \left(1 + gm_{2a} \left( r_{o,6a} \right) \right) \times \frac{gmb_{2a}}{gm_{2a}} \right] \quad (3)$$

$$\left|CMRR\right| = \left[ gmb_{2a} \left( r_{o,6a} \right) + 1 \right] \quad (4)$$

### 3.2. Analysis the noise and slew ratio

As stated in [1], the noise of those transistors that their transconductance does not affect the total transconductance of the cell can be ignored. In the proposed cell shown in the Fig. 2, the noise of the transistors of M6b, M5b, M6a, M5a, M4b, and M3b referred to input, can be ignored. This makes the calculation of the noise is simple and understandable. So, by calculating the noise of the other transistors at the output node and then referring to the input, the total thermal noise referred to the proposed cell input is calculated by (5). Parameter of $I_n$ is the thermal noise current of the related transistor:

$$\overline{V^2_{n,in}} = 2 \left[ \frac{\overline{I_{n,4c}{}^2} + \overline{I_{n,6c}{}^2} + \left( \overline{I_{n,2a}{}^2} \right) m^2 + \left( \overline{I_{n,4a}{}^2} \right) m^2}{m^2 \left( gmb_{2a} \right)^2} \right] \quad (5)$$

Equation (5) shows that the noise effects of M4a and M2a transistors in the input are more than other transistors because their value is multiplied by the current mirror gain as power of 2 ($m^2$). Therefore, the noise of two transistors should be reduced to obtain an OTA with a low noise.

To calculate the slew rate of the proposed cell, if it is assumed that a large negative and positive voltage are applied to the input Vin- and Vin+, respectively, these large voltages arrived to the bulk terminal of the transistors M1 and M2, but any of both transistors will not turn off. This is due to that the bulk voltage changes in the transistor is not so significant that turns off the transistor. In these conditions, it can be said that the current is reduced in one of the transistors and is increased in another transistor. In the other word, the current difference in the input differential pair is multiplied by current gain m and then arrived to the output to charge and discharge the output capacitor. Therefore, it can be said that the slew rate of the proposed cell is as (6).

$$SR = m \times \frac{I_{DS,1} - I_{DS,2}}{C_L} \quad (6)$$

Where $C_L$ is the output capacitor.

## 3. SIMULATION RESULTS

The proposed OTA is designed and simulated in 180 nm CMOS technology with 0.5 V supply voltage. The power dissipation of the cell is 250 nW while driving a 1 pF capacitive load. Fig. 3 shows the frequency response of the proposed cell, including the amplitude curve and phase curve. As shown in Fig. 4, voltage gain, unit frequency gain, and phase margin are obtained 14 dB, 12 kHz, and 95°, respectively. Moreover, by changing the control voltage ($V_{ctrl}$) in the range of 0-0.5V, the voltage gain of the cell is varied linearly in the range of 0-14.2 db. Fig. 5 shows the changes of the output signal swing for the control voltage changes, while a sinusoidal signal is applied to the input.

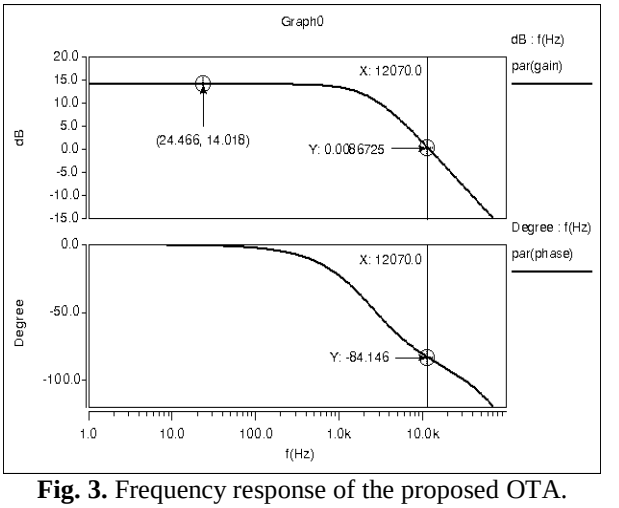


**Fig. 3.** Frequency response of the proposed OTA.

Table 1 reports the specifications of the proposed OTA.

## 4. CONCLUSION

In this paper, an operational transconductance amplifier (OTA) with the ability to change the transconductance is proposed for the linear range of control voltage. The used bulk-driven technique of input transistors increases the input dynamic range, significantly. The results of the simulations performed by HSPICE software in 180 nm CMOS technology show that the voltage gain is changed linearly from 0 dB to 14.2 dB for the control voltage in the range of 0 to 0.5 V. Also, the proposed OTA has the input dynamic range in the range of 0.175-0.375V under the supply voltage of 0.5 V, while consuming power of 250 nW.

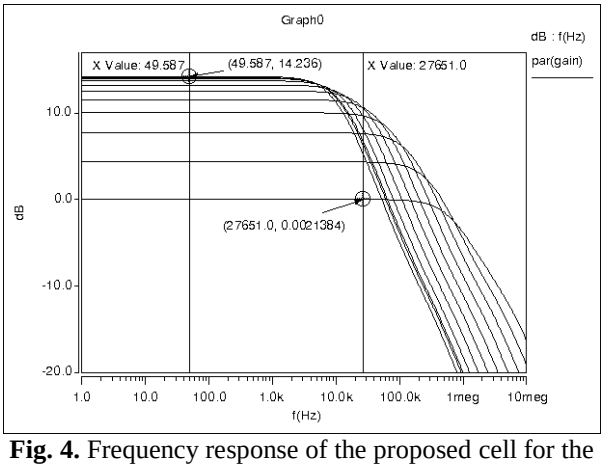


**Fig. 4.** Frequency response of the proposed cell for the changes of the control voltage.

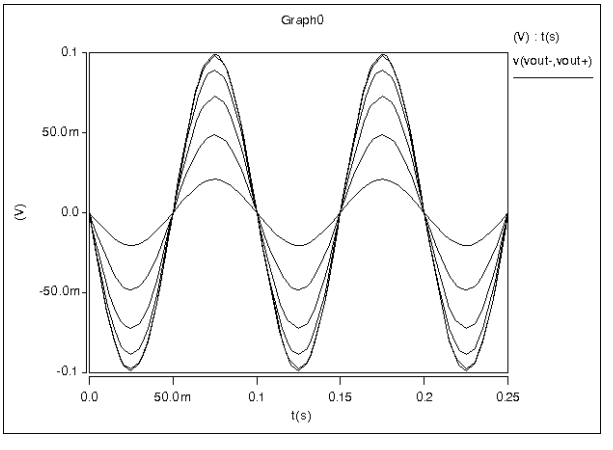


**Fig. 5**. Transient response of the proposed cell to changing the control voltage.

**Table 1.** Proposed OTA specifications.

| Parameter | Value | Units |
|---|---|---|
| Gain Range | 0-14.2 | dB |
| $V_{control}$ Range | 0-0.5 | V |
| Bandwidth | 12 | kHz |
| Capacitive Load | 1 | pF |
| Output Swing | 0.5 | V |
| THD | -30 | dB |
| CMRR | 32.4 | dB |
| PSRR | 14 | dB |
| ICMR | 0.25 | V |
| Power Supply | 0.5 | V |
| Average Power | 0.25 | µW |
| Technology | 180 | nm |

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