

# A Single Loop Feed Forward Sigma-Delta Modulator for GSM Standard

Ebrahim. Rahimi<sup>1</sup>, Mohsen. Beiranvand<sup>2</sup>, Gholamreza Babaabasi<sup>3</sup>

1- M.Sc., Arak Branch, Islamic Azad University, Arak, Iran.

Rahimiebrahim@yahoo.com

2- M.Sc., Islamshahr Branch, Islamic Azad University, Islamshahr, Iran.

mohsen.b\_66@yahoo.com

3- M.Sc., Shahab Danesh Institute of Higher Education, Iran.

r.babaabasi@yahoo.com

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## ABSTRACT:

A sigma-delta modulator designed as part of a complete GSM (enhanced data rate for GSM evolution) transceiver is described. High-resolution wide-band analog-to-digital converters enable the receiver to rely on digital processing, rather than analog filtering, to extract the desired signal from blocking channels. High linearity and High SNR are the most stringent requirements for the converters in this wireless application. In this paper a second-order modulator with feed forward structure in order to cover bandwidth correspond to GSM telecommunication standards is designed and simulated. In this modulator, low distortion structure and according to the relevant standard bandwidth is used. In order to provide minimum GSM standard requirement parameters, a second – order modulator is used and by an oversampling rate of 120 and bandwidth of 200 KHZ, SNR, 98 dB and the accuracy of 15.5 bits is achieved. Also its circuit structure by using capacitance switch method with 0.13 micron technology and 1.8 volt power supply has been implemented.

**KEYWORDS:** Analog to Digital converter, Sigma – Delta modulator, Low – power components, Low voltage.

## 1. INTRODUCTION

The global system for mobile communications (GSM), which originated from groupe special mobile developed by CEPT, has become the most popular standard for mobile communication all over the world, and analog-to-digital converters (ADCs) are one of the key modules in a GSM system. As used for GSM standard, 80–90 dB high signal to noise range (SNR) and 200 kHz bandwidth are required. Based on the above specifications, sigma–delta ADCs are no doubt the most appropriate structures among all kinds of ADCs because of their inherent tradeoff between high resolution and bandwidth along with low power. A sigma–delta ADC is made up of an anti-alias filter, a sigma–delta modulator and a decimator, among them, the modulator determines its performance, so this paper focuses on researching the modulator. The effective number of bits (ENOB) required for an ideal Nyquist-rate ADC to achieve the same resolution as an ideal sigma-delta ADC could be defined as:

$$\text{ENOB}_{\text{bits}} = \frac{(2^B - 1)(2L + 1)(2L + 1)^{1/2} R^{L+1/2}}{2a} \quad (1)$$

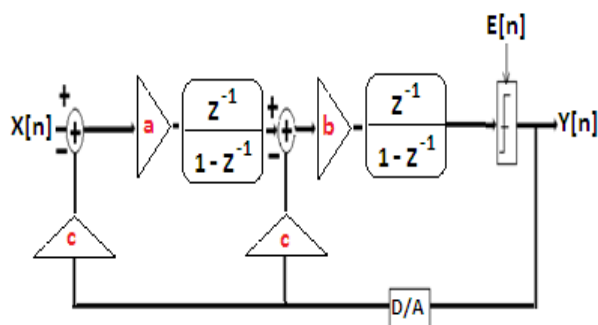
where L, R and B denote the modulator order, the oversampling ratio and the number of bits in the quantizer, respectively. According to Eq. (1), increasing L, R or B are all strategies to improve the ENOB. In most telecommunications standards, high dynamic range, high-bandwidth, low distortion and low noise level is very important. On the other hand the development of portable communication devices, in integration tendency make more number of communication channels at the level of a chip and low chip level and low power consumption important. Sigma-Delta converter has a low price. Also due to the development of related technologies and integration of analog to digital converter on the surface of a small chip with low power supplies, this requires that by designing an appropriate structure, large input signals can be processed without any problems. Loss power, signal to noise ratio and output bit rate (accuracy) are the most important features of standard. In the Sigma-Delta converter (SD) to obtain high bandwidth, they Reduce Over-sampling rate (OSR), which it causes increasing the sensitivity and the circuit non-ideal effects and also reducing converter performance. To overcome this challenge, methods such as increasing of modulator order and also increasing of the number of quantizer bit

is used[8],[2]. Considering the requirements of resolution, bandwidth and low circuit complexity, a 2th order, 1-bit modulator with R=120 has enough design margins for GSM applications.

For the purpose of satisfying the GSM high-resolution and near wideband requirements, a single-loop single-bit discrete-time topology should be a highly power-efficient choice because of its reduced building block sensitivity, low circuit complexity and high performance. In this paper, an improved loworder single-loop sigma-delta modulator has been designed in a 0.13- $\mu$ m CMOS technology. The integrated modulator achieves a 15-bit resolution over a signal bandwidth of 200 kHz. The prototype operates from a 1.8-V supply with a 64 MHz sampling rate.

**2. SIGMA - DELTA MODULATION**

Sigma - delta modulation is most often used in oversampling D/A and A/D converters. It allows for shaping of the quantization noise to improve the signal to noise ratio in the bandwidth of interest. As with traditional oversampling converters without noise shaping, sigma - delta modulators use oversampling to spread the quantization noise over a larger frequency range. When the oversampled signal is passed through a low - pass filter, there exists a greater signal to noise ratio than if the signal had been sampled at its Nyquist rate with the same quantizer. The noise - shaping transfer function used in a sigma - delta modulator can have arbitrary order. Higher - order noise shaping results in less quantization noise power in the bandwidth of interest, but more quantization noise power overall. Figure 2 shows a discrete -time block diagram for a second - order sigma - delta modulator [10].



**Fig.1.** Second-order sigma-delta modulator block diagram

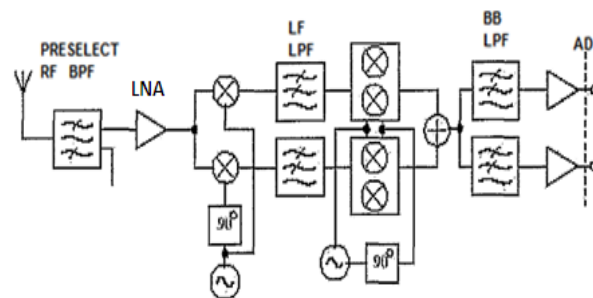
**3. BROADBAND STRUCTURE**

In figure 2, system structure of a broadband receiver to provide wireless communication standards features such as GSM is shown. In Table 1 bandwidth and accuracy required for each of the standards is specified. For signals with relatively average bandwidth, for example, the GSM standard, with considering average

over sampling rate (OSR) and an appropriate design can be achieved to desired components of mentioned Standard. For achieving to the desired accuracy, we can increase the number of differentiator bits or raise the order or increase the oversampling rate [7].

**Table 1.** Comparing of bandwidth and accuracy for different proposed standards [1]

Standard	GSM	WCDMA	WLAN	BLUETOOTH
Bandwidth	200KHZ	2 MHZ	10 MHZ	1 MHZ
Resolution	13 bit	9 bit	7 bit	11 bit



**Fig 2.** Broadband receiver [4]

**4. THE PROPOSED STRUCTURE**

In this work a second – order structure with feed forward structure in order to cover bandwidth correspond to GSM telecommunication standards is designed and simulated, that is specified in Figure 3. In which a single – bit differentiator and two integrators, one of them with delay and the other one without delay are used, for this work, low distortion structure is used, because it is very appropriate for broadband applications. Output swing of an amplifier used in the integrator, is limited by power supply that in practice this amount is caused by decreasing of amount of voltage on the output transistors which is located in the saturation region, is less than the ideal amount. In this structure, because the input signal is not entered directly to the modulator loop, the output swing of direct path integrator from the output of first integrator to the input of the stable differentiator of this modulator is such a way that differentiator follows the input signal after one delay unit. Another advantage of this structure is that sensitivity reduced to mismatches.

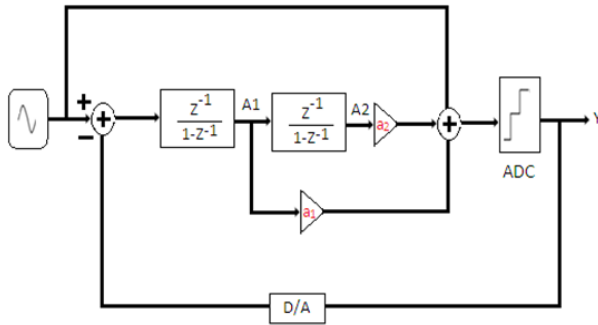


Fig 3. Structure of GSM

This modulator has a main feedback path that just needs a DAC in the feedback path. For used modulator, signal transfer function (STF) and noise transfer function (NTF) are as the numbers (2) and (3) relations:  $STF=1$  (2)

$$NTF=(1-Z^{-1})^{-2} \quad (3)$$

And also signal to noise ratio (SNR) is as the number (4) relation:  $SNR = 6.02N + 1.76 - 12.9 + 50Log(OSR)$  (4)

In which OR is the over sampling rate and N is the number of output bits of modulator. According to the relation (4) is obvious that by doubling the OSR, SNR increase to 15 dB and thereby the accuracy improves to 5.2 bits.

5. SIMULATION RESULTS

Figure 4 shows the output spectrum of modulator in the ideal mode for GSM standard in which input frequency is 200 KHZ, bandwidth is 100 KHZ and also sampling frequency is 48 KHZ. However, non – ideal effects such as sampling jitter or diversion from the ideal sampling, sampling noise or KT/C that it is caused by sampling capacitor of modulator and non – ideal effects of OP – AMP include limited gain, limited bandwidth, rotation speed and OP – AMP noise could have negative effects on the modulator performance, Figure 5 shows the corresponding output by applying non – ideal effect of jitter, In which it is determined that whatever jitter or diversion is lower, output is closer to the ideal state. Table 2 shows the Simulation results by applying all of the non-ideal effects. Figure 7 also shows the switch Scheme of simulated structure for GSM standard. And in Figure 6, used clocks scheduling are specified.

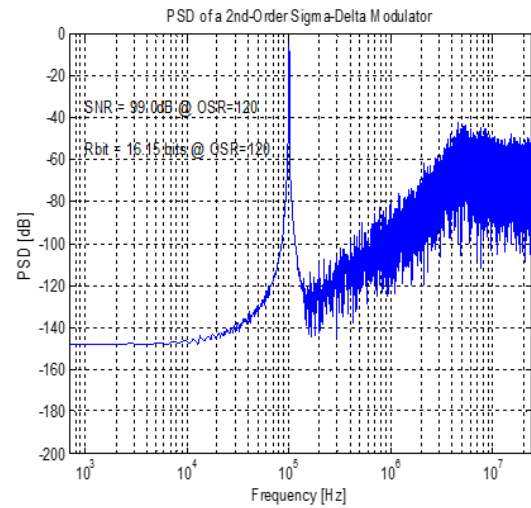
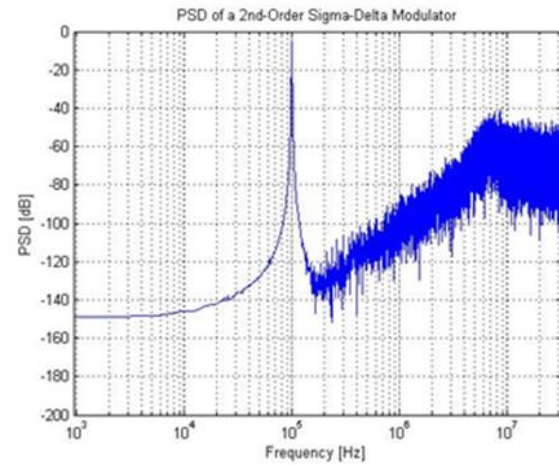
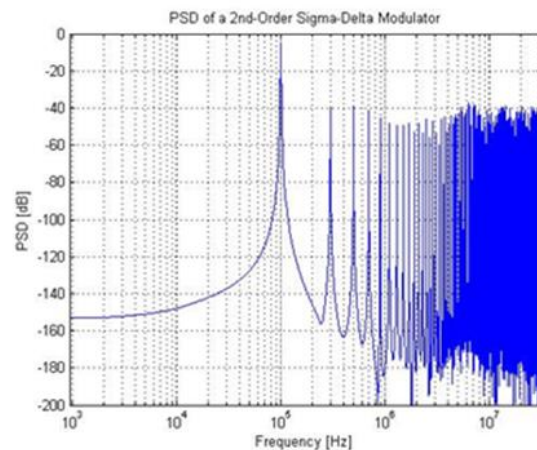


Fig 4. Modulator output for GSM standard



a



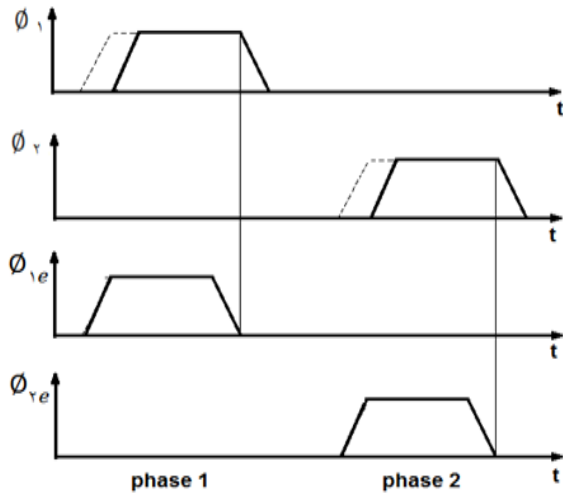
b

Fig 5. The jitter clock effect on the modulator  
a) Diversion of 12 ps b) Diversion of 12 μs

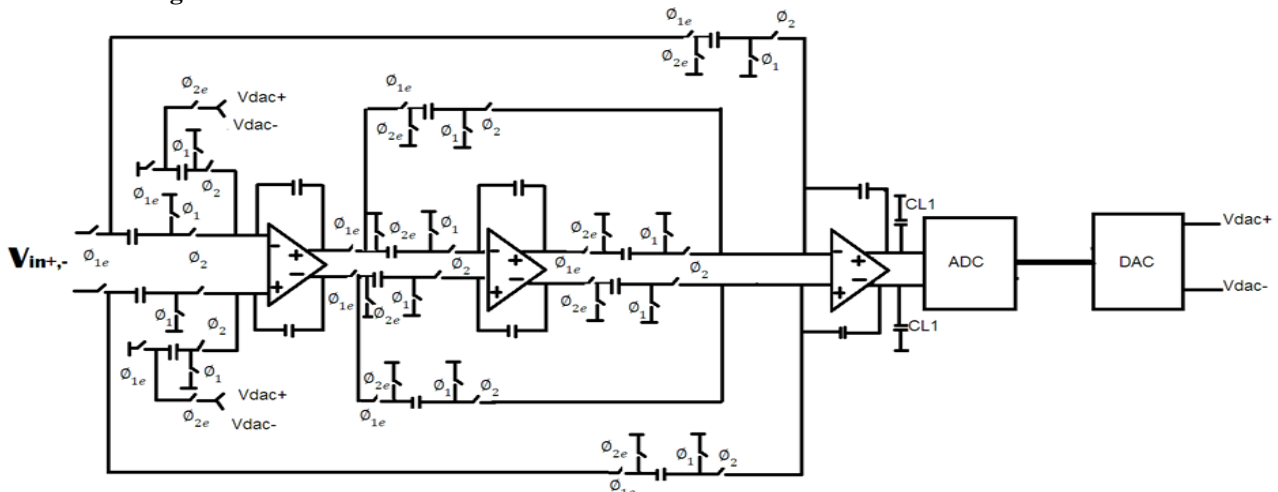
**Table 2.** Results of system simulation

GSM	Standard
200 KHZ	Bandwidth
120	Sampling Rate
48 MHZ	Sampling frequency
100 KHZ	Input Frequency
98 db	Signal to Noise Ratio
15.5	Accuracy

Table (3) compares the results of our work with those of similar works and demonstrates that the proposed design can compete and even outperform similar designs.



**Fig 6.** Used clocks schedulin



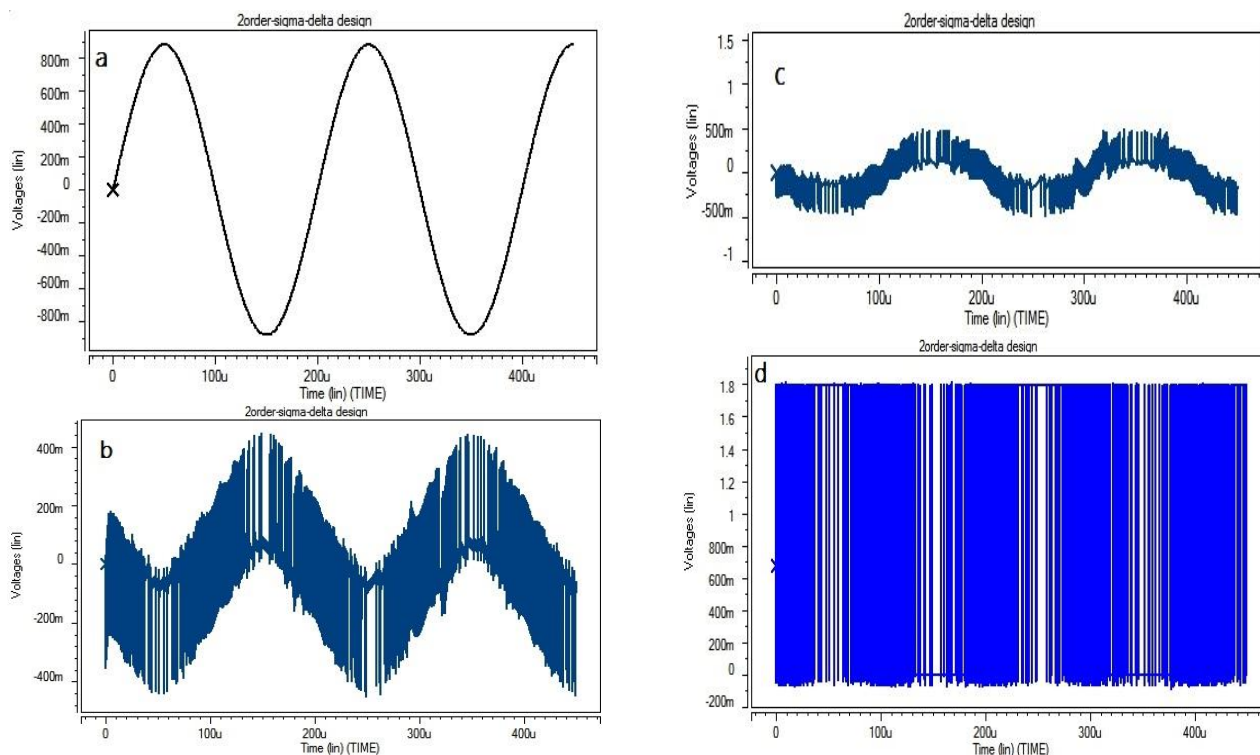
**Fig 7.** The switch Scheme of simulated structure for GSM standard

**6. CIRCUIT SIMULATION RESULTS**

The proposed sigma–delta modulator shown in Fig 3 has been realized by a fully-differential switched-capacitor circuit displayed in Fig 7 The modulator is controlled by two phase, non-overlapping clocks:  $\phi_1$  and  $\phi_2$  for the sampling and integrating phase, respectively, and delayed clocks ( $\phi_{1e}$  and  $\phi_{2e}$ ) are used to reduce the effects of charge injection. Figure 8 shows the input signal with the output of the first integrator and the second integrator and also total output of second – order modulator. According to the figure 8 (b) and (c) it is determined that integrators output relative to input signal causes the waste frequency is removed and it had 90 degrees phase difference compared to it, because integration operation in a phase and sampling operation in other phase is carried out.

**Table 3.** comparison of the results of this work with similar works

REFERENCE	4 ORDER [18]	3 ORDER [2]	2 ORDER [16]	2 ORDER This Work
Oversampling rate	128	160	64	120
Signal bandwidth	100 KHZ	100KHZ	100 KHZ	100 KHZ
standard	GSM	GSM	GSM	GSM
SNR(db)	100.2	94	88	98
Enobe	*	*	*	15.5



**Fig 8.** a) Input signal, b) The output of the first integrator, c) the output of the second integrator, d) total output of modulator

**7. CONCLUSION**

This paper was mainly concerned with analysis, modeling and design of  $\Sigma\Delta$  modulator, whose characteristics could be adjusted to the requirements imposed by GSM wireless standard, being so suitable for use in Wideband receivers. In this work a second – order with feed forward structure in order to cover bandwidth correspond to GSM telecommunication standards is designed and simulated is used that by applying the oversampling rate of 120 and bandwidth of 200 KHZ, SNR about 98 dB and accuracy about 15.5 bit can be achieved. Also its circuit structure by using capacitance

switch method with 0.13 micron technology and 1.8 volt power supply has been implemented. The results demonstrate that the usage of a Sigma-Delta modulator allows very weak analog signals to be converted to an extremely high resolution digital output.

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