A New Analysis, Design and Fabrication of DVB-T/T2 LDMOS UHF Broadband Amplifier

Farbod Setoudeh[1*], Mohsen Pooya[2]
1- Department of Electrical Engineering, Arak University of Technology, Arak, Iran.
Email: f.setoudeh@arakut.ac.ir (Corresponding author)
2- Department of Electrical Engineering, Arak Branch, Islamic Azad University, Arak, Iran.

Received: March 2020 Revised: May 2020 Accepted: June 2020

ABSTRACT:
In this paper we want to design linear amplifiers for the Multi Frequency Network (MFN) or Single Frequency Network (SFN) digital terrestrial applications for Digital Video Broadcasting-Terrestrial (DVB-T/T2) transmitters with frequencies of 400 to 900 MHz, so to achieve this aim, we have used Laterally Diffused Metal Oxide Semiconductor (LDMOS) transistor technology has been used. The RF input signal reaches the divider ballun, and then the input of both LDMOS transistors is given and the output of two transistors by the collector balloon reaches the output of the amplifier. We have simulated this design by using the Agilent Design System (ADS) software simulator with a gain more than 24 dB, the (Inter Modulation Distortion (IMD) signal has been attenuated from -29 to -52.5dBc and Power Added Effeciency (PAE) from 48 to 66% with 4-stage matching network consisting of capacitors and microstrips with a drain bias voltage of 28 volts and gate bias voltage of 2.86 volts in the frequency range 400 to 900 MHz. Eventually all of the circuit is designed on a printed circuit board.

KEYWORDS: Memcapacitor, Emulator, Electronic Device, Advance Design System.

1. INTRODUCTION

In classical circuit theory, there are three fundamental elements including resistor, capacitor, and inductor. These three elements represent the relationship between current and voltage, charge and voltage, and current and flux, respectively. They are passive and two-terminal elements, and the substructures of modern electronic, and are also used in all kinds of circuits. Besides these elements cannot save data, and they will lose their new data after passing a little time, if the power supply is interrupted [1].

Today, new memory elements called memelement have been identified and discovered.

Memelements are befitted for constructing self-organizing systems. These elements comprise the memristive devices (including memristor), memreactive devices (including memcapacitor and meminductor) [2].

Chua proposed another element as the fourth electronic element, and called “memristor” with memory defined the relationship between charge and flux [3]. Recently, these circuit elements save data without presence of power supply and are also used for low power calculations [4].

Moreover, for data which are attached together, the analog calculations could be replaced with available digital type. These concepts can be the base of brain function and perhaps in many other mechanisms in life organisms, which cause better learning, and better realization of adaptive behavior. In electronic designing, there is a lot of emphasis on using small and nanoscale elements while considering Moore`s law with other abilities [4]. Therefore, development of nanoscale memory cells in nonvolatile memory is necessary [5]. Chua proposed new elements by analysis of mathematical terms and called them “memristive elements” [6]. In these elements, resistance varies according to applied voltage, through atomic defect displacement which is due to lack of oxygen atoms in special positions in the film [7, 8].

In this case, while the power supply is off, the vacancy position of oxygen cannot go back to primary position easily and system remains in new resistance. The resistance of the memristor can vary from the minimum to maximum values. Recently, a lot of research have been done on the implementation and simulation of memristor in nanoscale [1-6].

These years, other devices from memristive family such as memcapacitors and meminductors are introduced and implemented. There is a growing interest in using these elements in different applications like biological systems. The devices are implemented in nanoscale and their behavior is simulated by electronic circuits easily. The memristive devices are nonlinear and usually have Chaos behavior in the electronic circuits

[9]. The memcapacitors can be categorized in two categories including voltage and charge controlled memcapacitor [10]. Ventra et al. developed memristive systems using other elements like memcapacitor and meminductor [11]. Ochs et al., used an energetic definition for modelling of memcapacitor and meminductor [2]. Memcapacitor can be used in many applications such as logical and memristive networks like artificial neural networks [12]. Recently, many researchers have been working on physical model implementation of memelements [13-17]. But the main problem is that there is no memelement commercially available, so it is preferred to design emulator circuits to study on these elements. A lot of research has been done on the design and implementation of the memristor emulator. Babacan et al., designed and implemented memristor emulator based on multi outputs operational transconductance amplifier (MO-OTA) [18]. Sánchez-López et al., designed and implemented grounded memristor emulator that operates from 16 Hz to 860 kHz [19]. Kanyal et al., designed and implemented memristor emulator based on OTA that operates for a frequency range up to 8 MHz for grounded emulator and up to 400 kHz for floating emulator [20]. Very few literatures are apply for the design of Memcapacitor [9-11, 21-29]. One common way to model the behavior of a memcapacitor is to use a mutator circuit to convert the memristor to memcapacitor. Recently, research has been conducted on the design of mutator circuits and its application in the design of grounded memcapacitors [21, 22]. In [21], SPICE modeling of memcapacitor along with mathematical definitions is proposed. Floating memcapacitors [23] and universal mutators in order to convert between memory, memcapacitors and meminductors [24].

In [25], a charge controlled Memcapacitor emulator without using memristor is designed [25] but operational frequency range is narrow. Sah et al. simulated a memcapacitor offered to work under 25Hz condition [26]. Yu et al. designed a memcapacitor with new characteristics operating up to 50Hz [27]. Wang et al. designed and implemented a memcapacitor based on a memristor that operates up to f=10Hz [22]. Using mathematical analysis, a model of memcapacitor was designed for using in other research. In this model, the frequencies of input signal are ω=0.2, 2, 10 [28]. Biolek et al. designed a memcapcitor from memristor, which works with f=1Hz of input sinusoidal voltage [29]. Pershin et al. proposed circuits with memristor to convert memristors into memcapacitors and meminductors [9]. It incited further inquiry on memcapacitor emulator circuits that operates up to f=50Hz and as a result, anumber of novel memcapacitors have been emerged in last few years [9, 11, 22, 26-29]. Venta et al. proposed a charge-controlled memcapacitor emulator that operates in 1Hz [11]. Wang et al. proposed a circuit of memcapacitor without fairly simple structure while using LDR [22].. Vista et al. used the Differential Voltage Current Conveyor Transconductance Amplifier (DVCCTA) to design memcapacitor emulator. This circuit is simulated by usong spice software based on 0.18μm TSMC CMOS technology [30].

Biolek et al., used the piecewise-linear constitutive relations between time-domain integrals of voltage andcharge to diesign memcapactor emulator based on switch capacitor technique [31]. This circuit is simulated by using spice software. So designing a memcapacitor simulator is an opportunity to discover real-world applications. Therefore, authors proposed a new design of a Memcapacitor emulator using analog active blocks. In this paper, for the first time, a new structure for a memory capacitor has been designed and implemented which can operate at frequencies greater than 260 Hz. The practical results of the designed circuit are the subject of this article. In this paper, the physical structure of the memory capacitor is examined and simulated. Then, the memory capacitor emulator is designed, analyzed, and finally implemented.

2. MEMCAPACITOR STRUCTURE

The memcapacitor is a memory device, and its capacitance varies according to voltage and charge. For systems with active and passive states, two conditions are considered. It starts from a full depletion mode in the passive systems, in which the capacitance is less than the amount of the added energy and cannot be more than it. Thus, the equation is given by [11, 16]:

$$U_C = \int_{t_0}^{t} v(\tau) i(\tau) d\tau \geq 0 \quad (1)$$

Where $i(\tau)$ is the current passing through the capacitor.

The relationship between charge and voltage of a memcapacitor is given by:

$$q(t) = C(q, v, t)v(t) \quad (2)$$

Where $q(t)$ is the charge, $v(t)$ is the voltage of memcapacitor, and $C(q, v, t)$ is memcapacitance. Careful scrutiny of this element determines that a variation in capacitance can occur because of two phenomena that are: a) an alteration in the structure of the system such as some MEMS capacitors or b) in the quantum-mechanical characteristics of the carriers and bound charges of the materials composing the capacitor or both. The capacitance of a voltage-controlled capacitor varies linearly or nonlinearly according to the applied voltage to the device, and varies between the minimum and maximum value in line. The nonlinear memcapacitance could be calculated by the following equation [16]:

$$\mathrm{C(v)} = \mathrm{C_{max}} - (\mathrm{C_{max}} - \mathrm{C_{min}})\mathrm{e}^{-|\beta \mathrm{v(t)}|} \quad (3)$$

Where $\mathrm{C_{max}}$ is the maximum capacitance of the memcapacitor while the applied voltage goes to maximum, and $\mathrm{C_{min}}$ is the minimum capacitance while the applied voltage goes to zero. The derivation of charge to time, is the current passing through a voltage-controlled capacitor:

$$i(t) = \frac{\mathrm{dq}}{\mathrm{dt}} = \mathrm{C(v)}\frac{\mathrm{dv}}{\mathrm{dt}} + \mathrm{v}\frac{\mathrm{dC(v)}}{\mathrm{dt}} \quad (4)$$

and:

$$\frac{\mathrm{dC(v)}}{\mathrm{dt}} = \mathrm{sign(v)}\beta(\mathrm{C_{max}} - \mathrm{C_{min}})\mathrm{e}^{-|\beta \mathrm{v}|}.\frac{\mathrm{dv}}{\mathrm{dt}} \quad (5)$$

By applying the external voltage to the two ends of the capacitor (voltage-controlled memcapacitor), the capacitance of this element will be changed. These dissipative processes result in an energy in the form of heat which warms the structure of the capacitor [11, 16]. Charge-controlled memcapacitor is given by:

$$\begin{cases} \mathrm{v(t)} = D_M(x(t), q(t), t) \\ \dot{x(t)} = \frac{dx(t)}{dt} = \mathrm{f}_q(x(t), q(t), t) \end{cases} \quad (6)$$

Where $q(t)$ and $\mathrm{v(t)}$ are the memcapacitor charge and voltage, respectively; $D_M = \frac{1}{C_M}$ is the inverse of memcapacitance; C_M is the memcapacitance and $x(t)$ is an internal state variable of the memcapacitor; charge-controlled memcapacitor is a special type in which the capacity varies according to quantities mentioned in Equation (3) and is called, time-varying capacitor. Then, the charge could be calculated by the current passing through the memcapacitor according to the following equation:

$$q(t) = q(0) + \int_0^{\mathrm{t}} i(\xi)\mathrm{d}\xi \quad (7)$$

The relationship between voltage and charge in the capacitor can be given by $q(t) = C_M(\mathrm{t})\mathrm{v(t)}$.

Using Eq. 6 and Eq. 7, we have:

$$\mathrm{v(t)} = \mathrm{D_M(t)}\left[\mathrm{C_M}(0)\mathrm{v}(0) + \int_0^{\mathrm{t}} i(\xi)\mathrm{d}\xi\right] = \frac{\left[\mathrm{C_M}(0)\mathrm{v}(0) + \int_0^{\mathrm{t}} i(\xi)\mathrm{d}\xi\right]}{\mathrm{C_M(t)}} \quad (8)$$

In this equation, $\mathrm{v(t)}$ is the voltage at the two ends of the capacitor and $\mathrm{v}(0)$ is the initial voltage.
Figure 1 shows the memcapacitor block diagram. In the proposed model, capacitor with state $x(t)$ and charge-controlled capacity is based on a nonlinear function$\mathrm{D_M}$. In this model, charge is time integral of the current ($q(t) = \int i(t)d(t)$. A design of the memcapacitor is shown in Figure 2, in which the capacitance can be regulated by dielectric width.

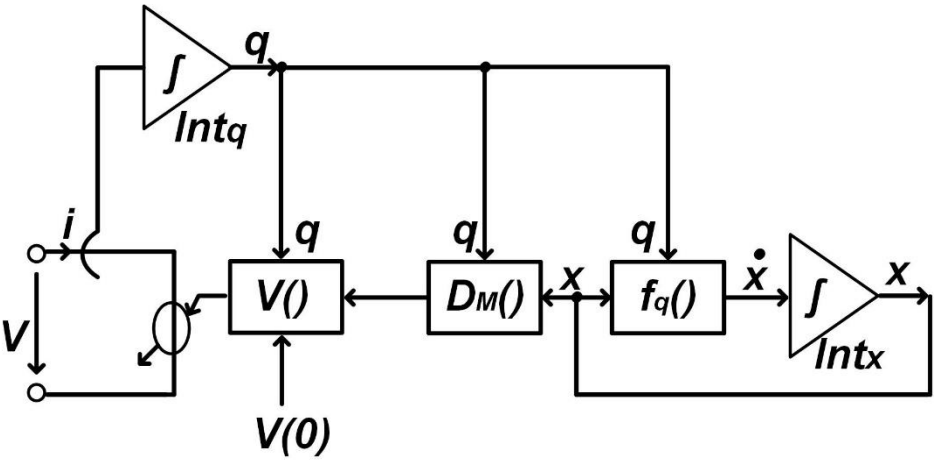

Fig. 1. The block diagram of memcapacitor model.

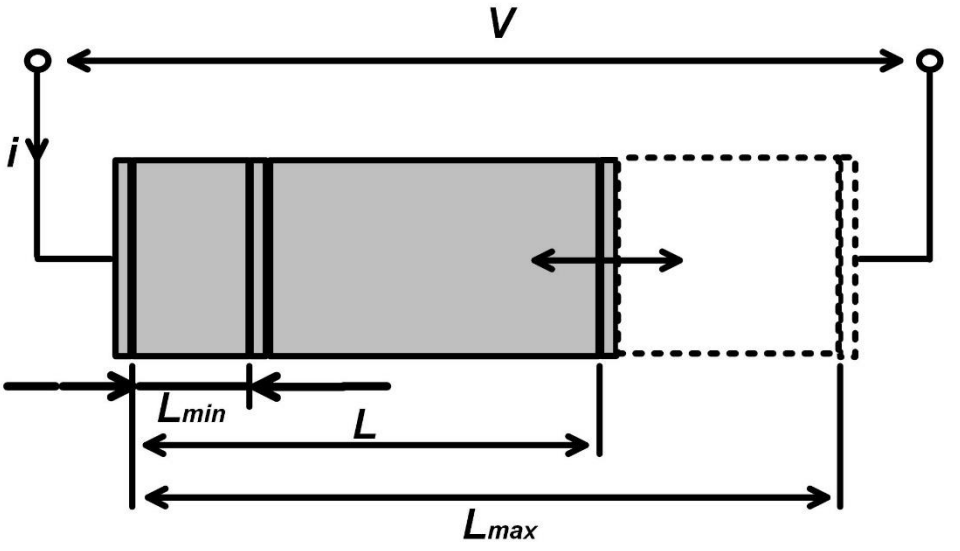

Fig. 2. A layout of the memcapacitor.

As shown in Figure 1, the blocks V, D, and f represents the voltage at the two ends of the memcapacitor, and the inverse of memcapacitance respectively.

Dielectric width (L(t)), varies between L_{min} andL_{max}; thus, the capacitance can change between C_{min} and C_{max}. The variable state x(t) is given as follows [10, 15]:

$$x(t) = \frac{L(t)-L_{min}}{L_{max}-L_{min}} \in [0,1] \quad (9)$$

So, the memcapacitance can be calculated as follows [16]:

$$C_M = \frac{1}{\frac{1}{C_{max}}+\left[\frac{1}{C_{max}}-\frac{1}{C_{min}}\right]x(t)} \quad (10)$$

So,

$$\dot{x(t)} = \frac{dx(t)}{dt} = kq(t)[1-(2x(t)-1)^{2p}] \quad (11)$$

Figure 3 shows the implementation of memcapacitor based on physical model in Advance Design System software (ADS). Transient analysis of memcapacitor is shown in Figure 4.

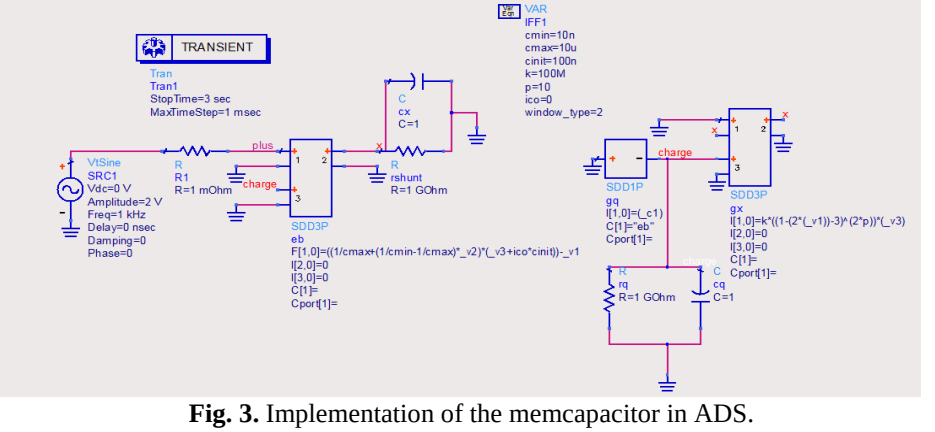

Fig. 3. Implementation of the memcapacitor in ADS.

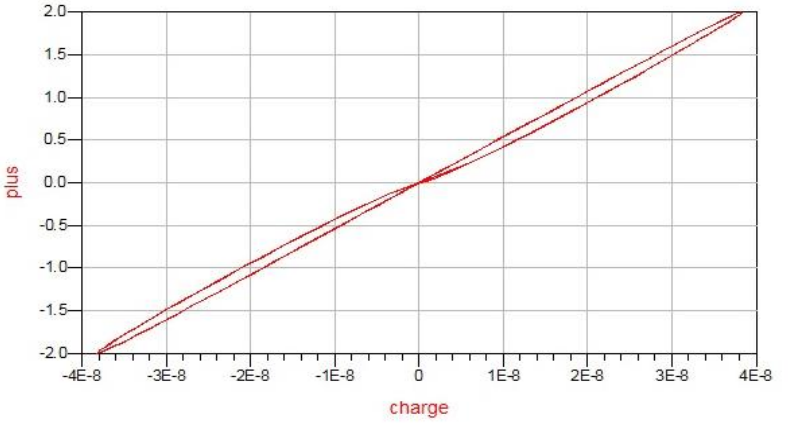

Fig. 4. Transient analysis of memcapacitor.

3. MEMCAPACITOR EMULATOR

Physical model of a memcapacitor is categorized in two ways: a) the capacitance of the memcapacitor varies according to the applied voltage to the ends of the device in form of nonlinear change. b) The capacitance of the memcapacitor varies according to the charge and is nonlinear.

In Figure 5, a circuit of the charge-controlled memcapacitor emulator with available electronic devices is illustrated.

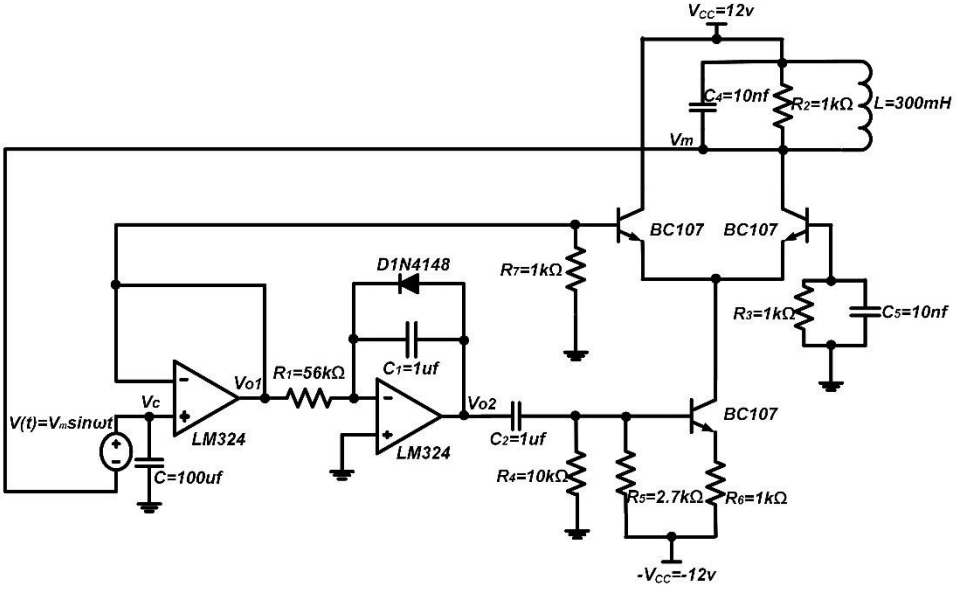

Fig. 5. Circuit of the memcapacitor emulator.

From circuit, V_{in} is given by:

$$V_{in} = V_c - V_m \tag{12}$$

Where, V_{in}, V_m and V_c are input voltage, output voltage of the multiplier and capacitor voltage (the voltage of $C = 100\mu$), respectively.
So:

$$V_c = V_{o1} = \frac{1}{c}\int i(t)dt = \frac{q(t)}{C} \tag{13}$$

Where, V_{o1} is output of the buffer circuit, $i(t)$ is current passing through the capacitance and $q(t)$ is stored charge in the capacitance.

Current passing through the R_1 is:

$$i_{R_1} = \frac{V_{o1}}{R_1} \quad (14)$$

From equation (13):

$$i_{R_1} = \frac{q(t)}{R_1 C} \quad (15)$$

Thus, the output voltage of integrator circuit can be calculated by:

$$V_{o2} = -\frac{1}{C_1}\int i_{R_1} dt \quad (16)$$

Using (15), (16) we have:

$$V_{o2} = -\frac{\int q(t)dt}{R_1 C_1 C} \quad (17)$$

For analog multiplier:

$$I_k = I_{k_0} + G_1 V_{o2} \quad (18)$$

Where $\boldsymbol{I_k}$ is ac-dc current passing through the Q_3 transistor, $\boldsymbol{I_{k_0}}$ is the transistor (Q_3) current in the operation point and is given as follow:

$$\boldsymbol{I_{k_0} = I_{E_3} = 1.9}$$

Where, $\boldsymbol{I_{E_3}}$ is the dc-current passing through the emitter of Q_3.

Also:

$G_1 \approx \frac{\mathbf{1}}{\boldsymbol{R_6}}$, $i_{c1}+i_{c2}=I_k$

$$\boldsymbol{i_{C_1} = I_s e^{\frac{v_{BE_1}}{V_T}}} \quad \boldsymbol{i_{C_2} = I_s e^{\frac{v_{BE_2}}{V_T}}} \quad (19)$$

Where $\boldsymbol{i_{C_1}, i_{C_2}}$ are current passing through $\boldsymbol{Q_1, Q_2}$ respectively in $\boldsymbol{ac}$ mode.

Therefore:

$$\boldsymbol{\frac{i_{C_1}}{i_{C_2}} = e^{\frac{v_{BE_1} - v_{BE_2}}{V_T}} = e^{\frac{V_{o1}}{V_T}}} \quad (20)$$

$\boldsymbol{i_{C_1}}$ is defined by the following equation:

$$i_{C_1} = \frac{I_k}{1+e^{Vo1/VT}} = \frac{I_k}{2}[1 - tanh\frac{V_{o1}}{V_{o2}}] \quad (21)$$

From (18),(21) and Maclaurin Series of $\boldsymbol{tanh\frac{V_{o1}}{V_{o2}}}$, $\boldsymbol{i_{C_1}}$ is defined as:

$$i_{C_1} = \left[I_{k_0} + \frac{V_{o2}}{R_6}\right][1 - \frac{V_{o1}}{2V_T} + \frac{1}{3} * \left(\frac{V_{o1}}{2V_T}\right)^3 - \frac{2}{15} * \left(\frac{V_{o1}}{2V_T}\right)^5 + \cdots] \quad (22)$$

By selecting proper parameters of RLC filter in the analog multiplier, $\boldsymbol{V_{o1}V_{o2}}$ will be in the output of the multiplier thus:

$$i_{C_1} \approx -\frac{V_{o1}V_{o2}}{2R_6 V_T} \quad (23)$$

Therefor:

$$V_m = -R_2 i_{C_1} = R_2 \frac{V_{o1}V_{o2}}{2R_6 V_T} \quad (24)$$

From Eq. (12),(24):

$$V_{in} = V_c - V_m = \frac{q(t)}{c} + \frac{q(t)R_2 \int q(t)dt}{2R_6 V_T R_1 C_1 C^2} \quad (25)$$

Therefore the relationship between charge and voltage of a memcapacitor is given by:

$$\mathbf{V_{in} = q(t)[\frac{1}{C} + \frac{R_2 \int q(t)dt}{2R_6 V_T R_1 C_1 C^2}]} \quad (26)$$

From Eq. 13, the inverse equation of memcapacitance of memcapacitor is:

$$C_M^{-1} = \frac{1}{C} + \frac{R_2 \int q(t)dt}{2R_6 V_T R_1 C_1 C^2} \quad (27)$$

4. RESULTS AND DISCUSSION

In order to verify the accuracy of the proposed emulator, the Advance Design System (ADS) software is used. Simulation analysis of the floating type is shown in Figure 6. The input voltage amplitude is $V_m = 1V$ and the voltage frequency is equal to the 50Hz, and 260Hz . Sine wave is used to run the simulator. The characteristic curve of the memcapacitor is shown in Figure 6.

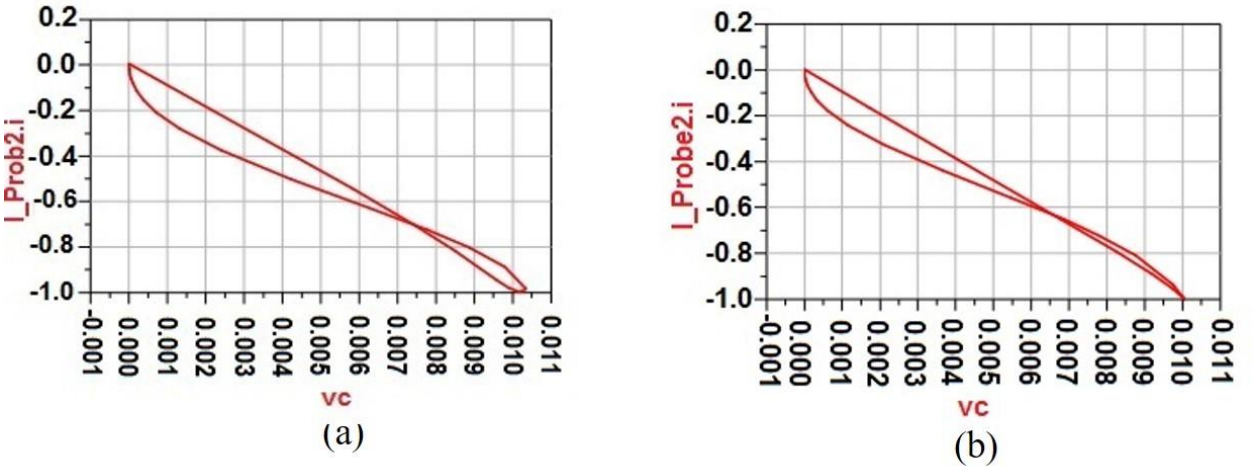

Fig. 6. ADS simulation results: Waveforms of the memcapacitor emulator for input voltage V_{in}= A sin (2πft.), with amplitude A=1 V and (a) frequency f=5oHz, (b) Waveform with frequency f= 260Hz.

5. EXPERIMENTAL RESULTS

The proposed circuit of the floating memcapacitor emulator with available electronic devices has been implemented on the breadboard. For this circuit, an input sinusoidal voltage at 1V and $\pm 12\, v$ power supply is used. This is depicted in Figure 7. Oscilloscope trace of the pinched hysteresis loop of hardware memcapacitor emulator at 10 Hz up to 260Hz is also shown in Figure 8.

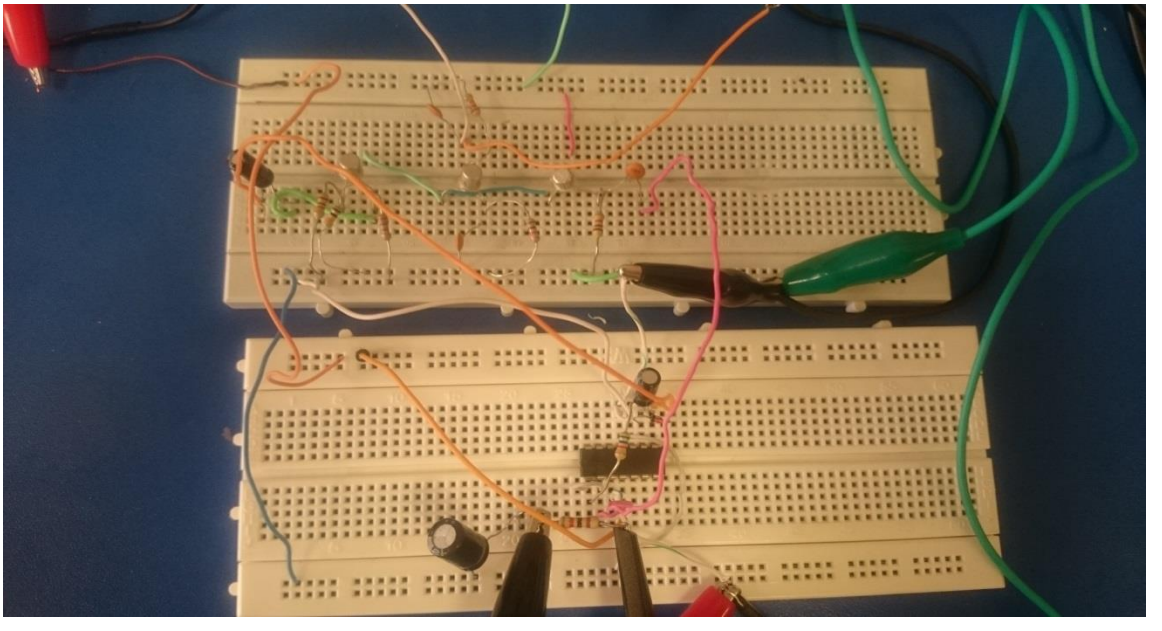

Fig. 7. The experimental memcapacitor emulator.

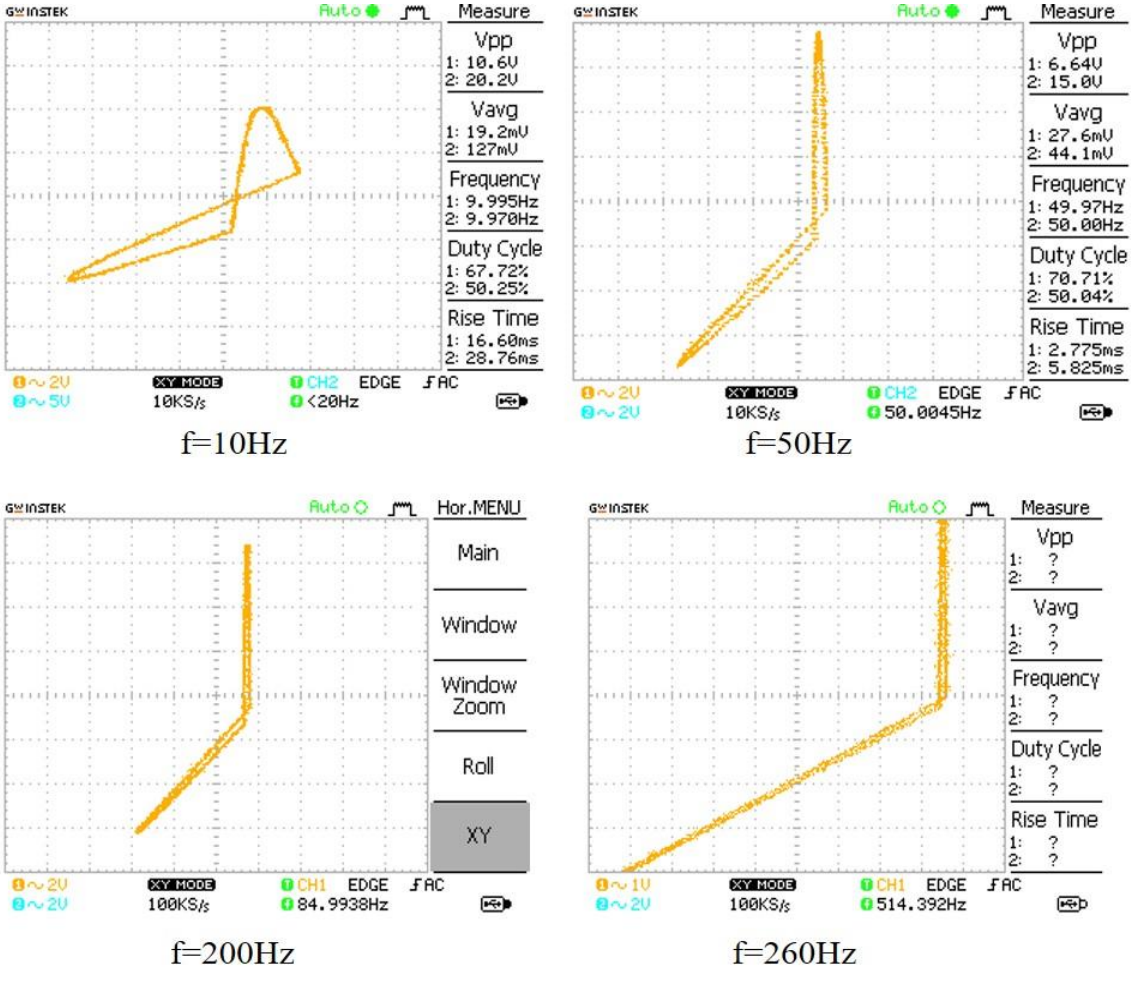

Fig. 8. The results of the physical implementation of the memcapacitor emulator.

6. CONCLUSION

In this paper, for the first time, a new structure for a memory capacitor which can operate at frequencies greater than 260 Hz has been designed and implemented. Moreover the physical model of memcapacitor can be realized by ordinary active devices. Based on the physical model of memcapacitor emulator, the researcher designed a floating-type memcapacitor emulator. The simulation results are in agreement with the theoretical results of this circuit. Using theoretical, experimental, and simulation results (ADS and physical implementation results), the operation of this circuit has been proven. This circuit can be used in other applications such as designing a complicated memcapacitor circuit. Because of its non-grounding limitation, the potential application of the floating-type of memristor is more extensive.

In this paper, we have proposed a good way to verify the two essential characteristics of the memcapacitor:

1. The memcapacitance varies according to the frequency of input signals, showing a helical shape of hysteresis loop.
2. The nonlinearity decreases with the increment of the input signal frequency. When the frequency reaches a large value, the memcapacitor becomes a linear capacitor.

The proposed Memcapacitor emulator has the following advantages:

- Simple and robust design
- Requires few number of active and passive elements
- Suitable for IC fabrication
- Consumes low power (in mW range)

REFERENCES

[1] L. Chua, **"Memristor-the missing circuit element,"** *IEEE Transactions on circuit theory*, Vol. 18, No. 5, pp. 507-519, 1971.

[2] K. Ochs and E. Solan, **"Energetically consistent modeling of passive memelements,"** *AEU-International Journal of Electronics and Communications*, Vol. 93, pp. 19-25, 2018.

[3] X. Wang, Y. Chen, H. Xi, H. Li, and D. Dimitrov, "**Spintronic memristor through spin-torque-induced magnetization motion,**" *IEEE electron device letters*, Vol. 30, No. 3, pp. 294-297, 2009.

[4] C. Yakopcic, E. Shin, T. M. Taha, G. Subramanyam, P. T. Murray, and S. Rogers, "**Fabrication and testing of memristive devices,**" in *The 2010 International Joint Conference on Neural Networks (IJCNN)*, 2010: IEEE, pp. 1-4.

[5] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "**The missing memristor found,**" *nature*, Vol. 453, No. 7191, p. 80, 2008.

[6] B. Bao, Z. Liu, and J. Xu, "**Steady periodic memristor oscillator with transient chaotic behaviours,**" *Electronics letters*, Vol. 46, No. 3, pp. 237-238, 2010.

[7] B. Muthuswamy, "**Implementing memristor based chaotic circuits,**" *International Journal of Bifurcation and Chaos*, Vol. 20, No. 05, pp. 1335-1350, 2010.

[8] S. P. Adhikari, H. Kim, B.-S. Kong, and L. O. Chua, "**Memristance drift avoidance with charge bouncing for memristor-based nonvolatile memories,**" *Journal of the Korean Physical Society*, Vol. 61, No. 9, pp. 1418-1421, 2012.

[9] Y. V. Pershin and M. Di Ventra, "**Memristive circuits simulate memcapacitors and meminductors,**" *Electronics Letters*, Vol. 46, No. 7, pp. 517-518, 2010.

[10] J. J. Yang, D. B. Strukov, and D. R. Stewart, "**Memristive devices for computing,**" *Nature nanotechnology*, Vol. 8, No. 1, p. 13, 2013.

[11] M. Di Ventra, Y. V. Pershin, and L. O. Chua, "**Circuit elements with memory: memristors, memcapacitors, and meminductors,**" *Proceedings of the IEEE*, Vol. 97, No. 10, pp. 1717-1724, 2009.

[12] J. Flak and J. K. Poikonen, "**Solid-state memcapacitors and their applications,**" in *Memristor Networks*: Springer, 201**4, pp. 585-601.**

[13] Y. V. Pershin and M. Di Ventra, "Spin memristive systems: Spin memory effects in semiconductor spintronics," *Physical Review B*, Vol. 78, No. 11, p. 113309, 2008.

[14] V. Mladenov and S. Kirilov, "**Syntheses of a PSpice Model of a Titanium-dioxide Memristor and Wien Memristor generator,**" in *2013 European Conference on Circuit Theory and Design (ECCTD)*, 2013: IEEE, pp. 1-4.

[15] Y. Ho, G. M. Huang, and P. Li, "**Dynamical properties and design analysis for nonvolatile memristor memories,**" *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 58, No. 4, pp. 724-736, 2010.

[16] M. Mohamed, H. Kim, and T.-W. Cho, "**Modeling of memristive and memcapacitive behaviors in metal-oxide junctions,**" *The Scientific World Journal*, Vol. 2015, 2015.

[17] Z. Yin, H. Tian, G. Chen, and L. O. Chua, "**What are memristor, memcapacitor, and meminductor?,**" *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 62, No. 4, pp. 402-406, 2015.

[18] Y. Babacan, A. Yesil, and F. Kacar, "**Memristor emulator with tunable characteristic and its experimental results,**" *AEU-International Journal of Electronics and Communications*, Vol. 81, pp. 99-104, 2017.

[19] C. Sánchez-López and L. Aguila-Cuapio, "**A 860 kHz grounded memristor emulator circuit,**" *AEU-International Journal of Electronics and Communications*, Vol. 73, pp. 23-33, 2017.

[20] G. Kanyal, P. Kumar, S. K. Paul, and A. Kumar, "**OTA based high frequency tunable resistorless grounded and floating memristor emulators,**" *AEU-International Journal of Electronics and Communications*, Vol. 92, pp. 124-145, 2018.

[21] D. Biolek, Z. Biolek, and V. Biolkova, "**SPICE modelling of memcapacitor,**" *Electronics letters*, Vol. 46, No. 7, pp. 520-522, 2010.

[22] X. Wang, A. Fitch, H. Iu, and W. Qi, "**Design of a memcapacitor emulator based on a memristor,**" *Physics Letters A*, Vol. 376, No. 4, pp. 394-399, 2012.

[23] Y. V. Pershin and M. Di Ventra, "**Emulation of floating memcapacitors and meminductors using current conveyors,**" *Electronics Letters*, Vol. 47, No. 4, pp. 243-244, 2011.

[24] D. Yu, Y. Liang, H. H. Iu, and L. O. Chua, "**A universal mutator for transformations among memristor, memcapacitor, and meminductor,**" *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 61, No. 10, pp. 758-762, 2014.

[25] M. Fouda and A. Radwan, "**Charge controlled memristor-less memcapacitor emulator,**" *Electronics letters*, Vol. 48, No. 23, pp. 1454-1455, 2012.

[26] M. Sah, C. Yang, R. Budhathoki, H. Kim, and H. Yoo, "**Implementation of a memcapacitor emulator with off-the-shelf devices,**" *Elektronika ir elektrotechnika*, Vol. 19, No. 8, pp. 54-58, 2013.

[27] D. Yu, Y. Liang, H. Chen, and H. H. Iu, "**Design of a practical memcapacitor emulator without grounded restriction,**" *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 60, No. 4, pp. 207-211, 2013.

[28] W. Wang, H. Xu, Y. W. Hou, and H. J. Liu, "**A circuit model of the memcapacitor,**" in *Applied Mechanics and Materials*, 2014, Vol. 644, Trans Tech Publ, pp. 3426-3429.

[29] D. Biolek and V. Biolkova, "**Mutator for transforming memristor into memcapacitor,**" *Electronics Letters*, Vol. 46, No. 21, pp. 1428-1429, 2010.

[30] J. Vista and A. Ranjan, "**Design of Memcapacitor Emulator using DVCCTA,**" in *Journal of Physics: Conference Series*, 2019, Vol. 1172, No. 1, IOP Publishing, p. 012104.

[31] D. Biolek, V. Biolková, Z. Kolka, and J. Dobeš, "**Analog emulator of genuinely floating memcapacitor with piecewise-linear constitutive relation,**" *Circuits, Systems, and Signal Processing*, Vol. 35, No. 1, pp. 43-62, 2016.