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Research Article

Efficient Design of Parity-Preserving Reversible Non-Restoring Divider

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Abstract

One of the basic challenges in high-density integrated circuits is loss of power consumption, which is caused by presence of transistors in circuits and causes the temperature of the circuit to increase. The design of digital circuits in a reversible way can be used as one of efficient approaches to solve this challenge. In addition, the design of parity-preserving reversible circuits can be very effective in detecting faults in circuits. Dividers are used as one of the most widely used circuits in digital computing systems. Divider circuits include an adder, a multiplexer and two sequential register and parallel-in to parallel-out left shift register circuits. This paper is presented a new and efficient design of a parity-preserving reversible non-restoring divider. For this purpose, first, a parity-preserving reversible D-latch is proposed. second, a parity-preserving reversible n-bit register is presented using the proposed reversible D-latch. Third, a parity-preserving reversible (n+1) bit shift register using the proposed reversible D-latch and other reversible gates is proposed. Finally, a parity-preserving reversible n bit divider is developed based on the non-restoring algorithm. The results of comparisons show that the proposed circuit is superior in terms of evaluation criteria of reversible circuits such as quantum cost, number of constant inputs and number of garbage outputs compared to previous works.

Keywords: Divider, non-restoring algorithm, Parity-preserving reversible circuit, Quantum computing, Reversible logic.

Highlights

- Proposing a reversible D-latch memory with parity preserving ability.
- Introducing a reversible register with parity preserving ability.
- Providing a parity preserving reversible left-shift register with parallel load capability (PIPO).
- Development of an efficient parity preserving reversible non-restoring divider using the proposed circuits.

Citation: [in Persian].