JACET Journal of Advances in Computer Engineering and Technology, 2(1) 2016

Novel Defect Terminolgy Beside Evaluation And Design Fault Tolerant Logic Gates In Quantum-Dot Cellular Automata

Mehrdad Poorhosseini

Received (2015-11-07)
Revised (2015-12-26)
Accepted (2016-01-02)

Abstract **- Quantum dot Cellular Automata (QCA) is one of the important nano-level technologies for implementation of both combinational and sequential systems. QCA have the potential to achieve low power dissipation and operate high speed at THZ frequencies. However large probability of occurrence fabrication defects in QCA, is a fundamental challenge to use this emerging technology. Because of these various defects, it is necessary to obtain exhaustive recognition about these defects. In this paper a complete survey of different QCA faults are presented first. Then some techniques to improve fault tolerance in QCA circuits explained. The effects of missing cell as an important fault on XOR gate that is one of important basic building block in QCA technology is then discussed by exhaustive simulations. Improvement technique is then applied to these XOR structures and then structures are resimulated to measure their fault tolerance improvement due to using these fault tolerance technique. The result show that different QCA XOR gates have different sensitivity against this fault. After using improvement technique, the tolerance of XOR gates have been increased, furthermore in terms of sensitivity against this defect XORs show similar behavior that indicate the effectiveness of improvement have been made.**

Keywords **- Quantum dot Cellular Automata (QCA); fault-tolerant gate; XOR; Defect terminology**

1- Faculty of Computer and Information Technology Engineering, Qazvin Branch, Islamic Azad University, Qazvin, Iran(m.poorhosseini@qiau.ac.ir)

I. INTRODUCTION

With the advancement of CMOS technology and increasing operating frequency at nano scale, nonideal behaviors like leakage power consumption and short channel effects cause serious restrictions for maintain scalability based on Moore's Law [1]-[5]. QCA has capability to implement both sequential and combinational circuits like full adders [6] and Flip Flops [7] [8]. Due to having positive properties such as greater speed, low power consumption and smaller feature size, QCA is one of the important candidates for replacement of CMOS transistors. Recent achievement in QCA focuses on molecular and magnetic implementations that give higher speed and also can be operational in room temperature [8]-[11]. Very small scale and nano fabrication limits impose a hurdle to design of QCA devices and necessitate fault tolerant analysis in this technology. Because of happening inevitable faults reliable computation in QCA systems faces problems. In modern nanotechnologies like QCA with large degree of doubt in performance due to quantum phenomena that lead to large number of defects to occur, it is obvious that appropriate framework must be prepared [10]. This paper after illustration some of techniques for fault tolerant designs present a new exhaustive classification of different kind of QCA defect. Then by use of optimized technique with minimum redundancy the action of robustness were implemented to XOR gates.

The rest of this paper is organized as follows. In section 2, a review of QCA is presented. In section 3, a survey from most of defects in new classification is discussed. In section 4, fault tolerant analysis in QCA XOR gates is presented. Then by use of robust majority gate as a fault

tolerant technique the circuits were improved and fault tolerant analysis performed again to measure the fault tolerance improvement.

II. PRELIMINARIES

1. *QCA Review*

In fig 1 a QCA cell and three basic logic elements shown. As shown in fig1 (a) each cell contains four quantum dots that two mobile electron tunnel between dots by columbic interactions. The Columbic interactions between two neighboring cells that determine the polarization of a cell (i and j) computed using following equation so-called kink energy E_k [10]:

$$E_j^i = \frac{1}{4\pi\varepsilon_0\varepsilon_r}\sum_{n=1}^{4}\sum_{m=1}^{4}\frac{q_n^i\, q_m^j}{|r_n^i - r_m^j|} \quad (1)$$

Binary wire, inverter and majority voter are basic elements in QCA that any circuit can be built using them (Fig 1.b, 1.c and 1.d). Majority voter is the most important logic gate in QCA. The logic function of majority voter based on the following:

$$M(A, B, C) = AB+BC+AC \quad (2)$$

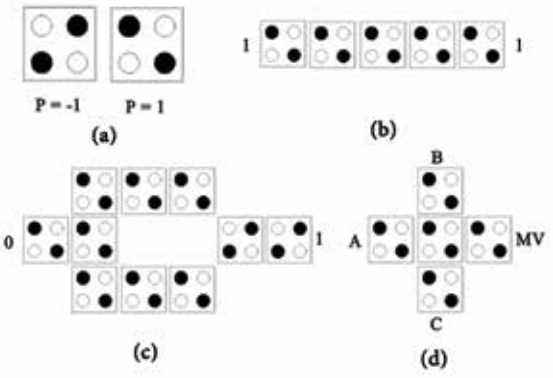

Fig.1. Basic QCA Elements: (a) QCA cell, (b) Binary Wire, (c) Inverter, (d) Majority Gate

2. *QCA Clocking*

Clocking is one of the important subjects in QCA circuit design. As shown in Fig. 2 each clock cycle divided into four phases: switch, hold, release and relax. During switch phase inter-dot barrier gradually raised and under effect of neighboring cells a cell switches into one of the stable polarizations. During hold phase a clock attains a high level to maintain the current polarization of the cell. The polarization start to reduce through the release phase and at last become unpolarized during relax phase to change the state of the QCA cell by the effect of neighboring cells [4] [12].

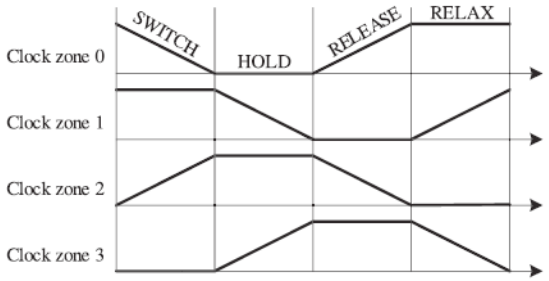

Fig.2. QCA Clocking scheme

III. NOVEL DEFECT TERMINOLOGY

Due to the possibility of occurrence various defects in nano devices and the importance of fault tolerant design in QCA, know and categorize all kind of defects is necessary. This section present the exhaustive collection of faults as a defect terminology that have been reported in several papers. According to this terminology, defects of QCA basically can be divided into two general categories: intra-cell and extra-cell. Each category fully described in the following.

1. *Intra-Cell Defects*

Intra-cell defects are said defects that be occurrence at inner position of the cell and more affected by dots and electrons. Examples of the most important intra-cell defects are as follows:

1) *Cell with extra dot*

This defect means that there are five quantum dots instead of four quantum dots in the cell[13]. Additional dot cause to create a non-ideal cell with the possibility of placing an electron in a central point (Fig 3-a).

2) *Cell with extra dot and electron*

In this defect, in addition to an extra dot in the cell, an additional electron as the third electron is trapped within the cell that because of the low distance between electrons strong repulsion occur and cause problems for cell polarization[13] (Fig 3-b).

3) *single electron fault*

In normal state, it should be exist two electrons in any cell but in the face of this defect, there is only one electron in the cell that is said “single electron fault”. Figure 3-c shows these

defect. In [14] the effects of this defect simulated in the inverter and in [15] simulated in binary wire.

4) dot misalignment

In normal mode, QCA cells are accordant to Fig 1-a. If the dots in the cells are not in this case and are not in the corners of cells, the electrons that are within these dots are put in non-ideal distance from each other and require more energy [13]. However, probability of occurrence of this fault appears very low (Fig 3-d).

5) stray charge defect

According to figure 3-e, this defect occurs when the cell polarization weakened due to fabrication and manufacturing defects. It means that instead of polarization 0.8, cell have polarization 0.02. As fully explained in [16], in some cases, the defects can cause a malfunction in a binary wire. The weakening of the polarization in order to occurrence stray charge defect increases the risk of noise susceptibility in the circuit. On the other hand, in the case of this fault occurrence in the transmission cycle to the output, it looks if neighboring cells are slightly displaced by the fabrication defects, the circuit sensitivity value increases to different defects.

2. Extra-Cell Defects

Extra-cell is said to the defects that related to the interactions between cells and mainly are from fabrication defects and manufacturing phase. These defects are more common than intra-cell defects and occurrence of them is more likely in different circuits. However, most research has focused on the extra-cell defects. In continue paid to investigate a number of these defects:

1) Cell displacement

This defect occurs when the cell digress a few nanometers from its original location. In fact the distance between cells is more than it should be. Increasing distance causes to attenuation the signal transmission process and even may interrupt the signal. The occurrence of this fault in the circuit can deteriorate the output. In this case, displaced cell impact on their neighbors and the impact cause to error in the proper functioning of the circuit and change the normal signal transmission to the output [2][10][12][17]-[20]. Fig 4-a show how to create this defects.

2) Cell misalignment

This defect containing displacement cell defect and can be generated when a defective cell is deviated from the right direction. In addition to the distance between the cells is more than normal cells, defective cell deviated from its axis. In fact, in displacement cell, the cells are in proper direction with incorrect distances, but in misalignment, the defective cell in addition to displacement, is not in proper direction of other cells. Here both the value of displacement and also the value of deviate from right direction are important. This defect also called offset [2][10]. Fig 4-b illustrates this fault.

3) missing cell

In this defect, there are one or more cells in a circuit that are not in specified place. As in stray charge defect case polarization transfer faces to problem, In the event of missing cell it can also be occur. This fault will be more likely to happen because in the event of missing cell a gap is created in the size of a cell. Although in some cases, the lack of a cell in the circuit with simpler architectures and shorter wire length may not cause serious problem but in most cases, especially in complex architectures, the occurrence of this defect causes to create problem in the signal transmission into the output. Furthermore this defect is one of the important fault [2][10][12] [17]-[21]. Fig 4-c illustrates this fault.

4) additional cell

In the basic blocks that there is blank space between or beside the cells, there may be placed an additional cell at the edges of cell in blank space by mistake. As in [21] simulated, this defect can also cause error in the output of circuit. For example, in the presence of occurrence of this defect in larger circuits, in the blank spaces that have been deliberately placed no cell, the cell is placed, and may be achieved the result in the opposite of what should be. Fig 4-d shows this defect at the majority gate.

5) cell rotation

This defect occurs when a cell rotate in its place. In a quantum block, such a problem can be impact on adjacent cells and thus the circuit output. Figure 4-e illustrates this defect. According to simulation results in [22] that checked assessment of occurrence of this defect on different basic modules, including binary wire, majority gate, L-shaped wire and etc. different tolerance levels against cell rotation considering the different rotation angles. The results show, the inverter is the weakest structure while the straight wire is the most reliable structure in the event of this defect [22].

6) Stuck-at 0/1

Occurrence of this defect means that the QCA cells in polarization -1 or 1 be fixed [23]. In other words, electrons cannot do correctly tunnel operations within the QCA cells.

7) random clock shifts

This defect occurs when cells in a QCA circuit is not in clock phase that must be within it. In fact, the clock signal is not entering to circuit in the right time and for example by shifting a few degrees, clock signal enters. The results of simulations carried out in [24] show that by increasing the amount of random phase shift of clock in the circuit, the correct answer in the circuit is reduced and this can be different according to the type of simulation vector and structure of each module.

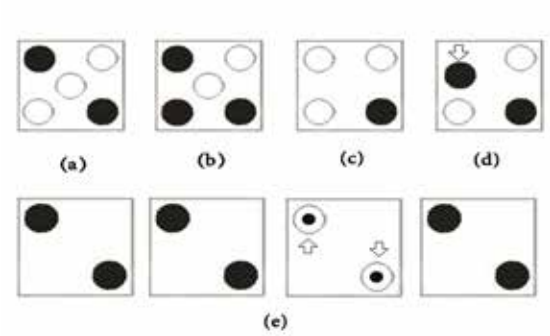

Fig.3. Intra-Cell Defects: (a) Cell with extra dot, (b) Cell with extra dot and electron, (c) Single electron fault, (d) Dot misalignment, (e) Stray charge defect

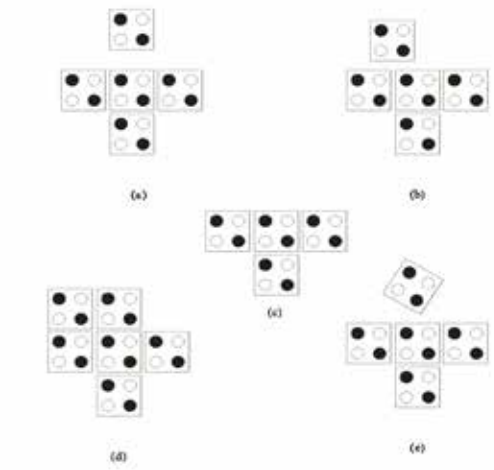

Fig.4. Extra-CellDefects: (a)Displacement, (b) Misalignment, (c) Missing, (d) Additional cell, (e) Rotation

IV. FAULT TOLERANT DESIGN METHODS IN QCA CIRCUITS

Redundancy is one of the most common techniques used in the context of fault tolerance. In QCA also use redundancy to reduce the effect of defects. In this section two different techniques that use redundancy to increase defects tolerance will be discussed. Tile structures and robust majority gate can be employed in circuits to raise the level of defect tolerance. Another fault tolerant technique in QCA is the operational implementation of circuit in one layer. This means that firstly, Due to the problems of operate circuits with crossover or multi-layer such as increase sensitivity against physical parameters like dimension and temperature in QCA [25][26], this is better that basic blocks simulated in small size and in one layer without crossover. Secondly circuits should have accessible inputs and outputs because when they were surrounded by their own cells, implementation of circuit in a layer practically is not possible and to access to them needed an additional layer. What said in above increases the risks of tolerance of the circuit and it looks that is impressive in increasing of faults in manufacturing phase. In [27] the effects of the multi-layer implementation on fault tolerant designs and how to efficient implement by taking risks of multi-layers were discussed.

1. Tile Structure [18]

Tile structure is introduced as a model to create redundancy in QCA basic blocks. In general, tile structure presented as square set of QCA cells as N × N that are added to the circuit. For example as 3 × 3 (Figure 5-a). What is important in Tile structures is that the risk of signal attenuation get the minimum value by creating the redundancy, and the signal is going into output, in addition to logical stability have high level of polarization. According to simulation results output will be in strong polarization, but the problem is that there is a lot of redundancy.

2. Robust Majority Gate Structure [4]

Another technique used in QCA circuit design is using robust majority gate structure. In [4] the majority gate structures has been described in different modes. As shown in Fig. 5-b, to make a correct voting structure, all input signals should enter simultaneously to specific clock phase. When they arrive to central cell in Majority gates and the next phase of the clock is central cell of

Majority gate, then to avoid output noising, the cells that forward output signal should be in the next phase of clock. Fig 5-b is shown the most appropriate structure of majority gate. According to the simulation results was carried out in this paper and defect tolerance of circuits before and after the injection of robust majority gate evaluated, The if in a circuit all of the majority structures be used in this case, fault tolerance level of the circuit will increase significantly.

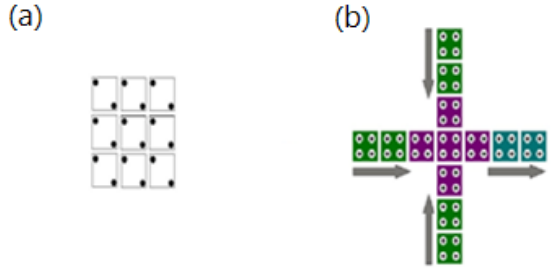

Fig.5. Some of fault tolerant structures: (a) Tile, (b) Robust Majority Gate

V. SIMULATION RESULTS OF FAULT TOLERANT DETERMINATION IN QCA XOR GATES

XOR gate is one of the most useful basic block in QCA that it can be used to create modules such as adders and parity generators. In this section, several XOR gates shown. All of them are made based on majority gate except one case. All simulations were performed by QCA Designer 2.0.3 [28] and based on the default software parameters.

1. Introduction of XOR gates

XOR gates provided by Shah et al [29], Suresh et al[30], Roohi et al[31], Mustafa et al [32], and two gate provided by Mahdiani et al [33], all are optimized gates with the minimum possible cell, occupying less space and high speed. Table 1 includes brief specifications of some existing XOR gates. Layout and waveform of these gates are displayed in Fig 6. In continue fault tolerant investigations of each gate against one of extra-cell defects will be described.

Table 1. Summery of xor gates properties

#	DESIGN NAME	Area(um^2)	Delay(Clk)	I/O Accessibility
1	Shah [29]	0.0283	1	Yes-No
2	Roohi [31]	0.0316	1	No-Yes
3	Suresh[30]	0.0388	0.75	No-Yes
4	Mustafa [32]	0.0431	1	No-Yes
5	Mahdiani 1 [33]	0.0518	1	Yes-Yes
6	Mahdiani 2 [33]	0.0352	1	Yes-Yes

2. Fault sensitivity evaluation of XOR gates against missing cell

In this section, the sensitivity of XOR gates against missing cell is tested by fault injection to each cells of each gate. In case of occurrence of this fault polarization transfer function of the circuit is compromised and this often causes problems in the main functioning of the circuit. To determine the resistance of circuits in the presence of missing each cell, after simulation the output value calculated. The simulation results have shown in Fig 7. The percentages in Fig 7 show the cells of circuit that do not change the correct output by removal them. The simulation results show that Mahdiani 2 gate is the most resistant gate against this defect. Mahdiani 1 seems weak, but with regard as operational implementation of circuit in one layer, this gates due to the accessibility of inputs and outputs can be implemented as single layer, It looks that its simulation will be better operated with what is occur in real. But by looking at other gates this result is achieved that due to the inaccessibility of their input or output, they should be implemented in additional layer, so they are not single layer. As mentioned in previous Section, it seems that additional layer increases the risk of fault tolerance in a circuit. Thus, according to all of indicators mentioned above Mahdiani 1 and 2 gates are more reliable and fault tolerant and operational in one layer. As is clear, XOR gates have high sensitivity against missing cell defect.

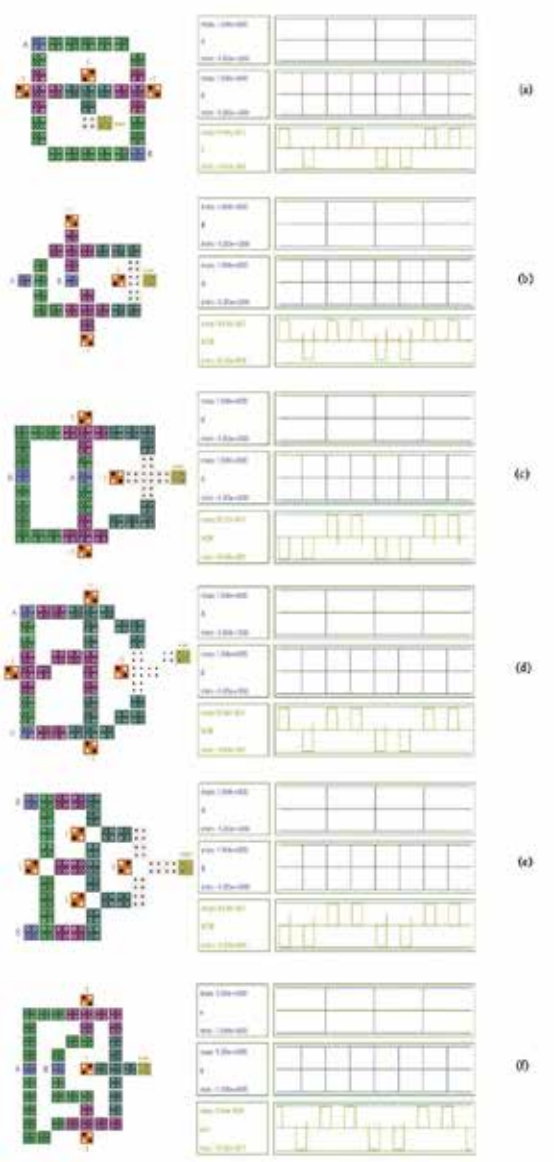

Fig.6. Layouts and waveforms of some existing XOR gates: (a) Shah[30], (b) Roohi[31], (c) Suresh[32], (c) Mahdiani 1[34], (d) Mahdiani 2[34], (e) Mustafa[33]

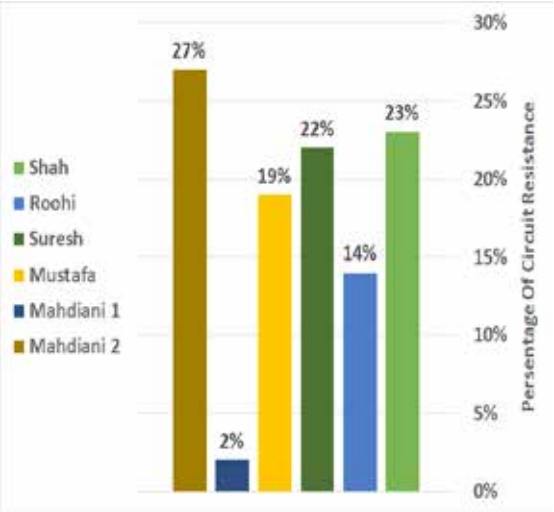

Fig.7. Simulation results of sensitivity of XOR gates against Missing cell

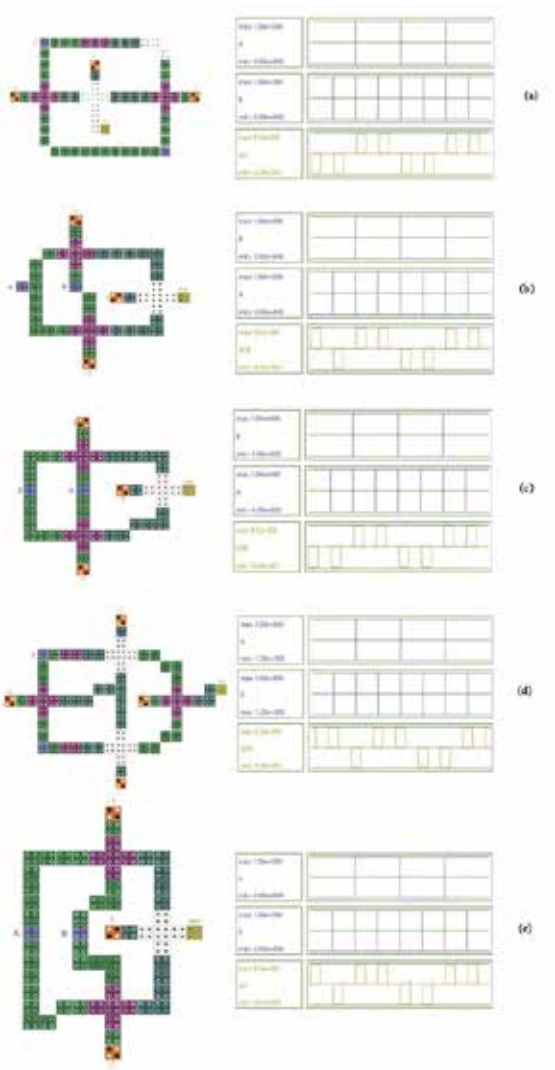

Fig.8. Layouts and waveforms of improved gates: (a) Shah, (b) Roohi, (c) Mustafa, (d) Mahdiani, (e) Suresh.

VI. IMPROVING THE SIMULATED GATES USING ROBUST MAJORITY GATE UTILIZATION

In the previous section several XOR gates were introduced and after fault injection the resistance of each gate was calculated. In this section, at first all of these gates except one gate that was not simulated with majority gate were strengthened using Robust Majority Gate. If tile structures were used for improving fault tolerant level of the circuits then a lot of redundancy were appear and wiring will be very thick and voluminous, so the use of the Robust Majority Gate has the advantage that with less redundancy the circuit fault tolerance come up. In these five gates, using the Robust Majority Gate has been applied and improved them. In this section, majority gate modules in all of the introduced XORs in the previous section is removed and the tolerant majority gate has been replaced them and again and clocking operation is injected to XOR gate cells. Then, fault injection to the improved gates were done again to calculate the resistance of each gate. Simulation results show that improved gates were much stronger than before. Table 2 includes features of improved gates and their comparison with their situations before improvement. In this table additional redundancy is calculated as follows:

$$Persentage\ Of\ Redundancy = \frac{\#\ Redundant\ Cells}{\#\ Cells\ Before\ Robustness}$$

Fig 8 also shows layout and waveforms of improved gates. In Fig 9, the value of obtained improvement of any gate is compared with its previous state to determine the level of improvement that each gate achieved.

Fig 9 shows simulation results of each gate before and after injecting fault tolerant technique. Blue color indicates circuit resistance prior robustness and red color indicates the circuit resistance after using the robust majority gate. Mahdiani gate have the greatest improvement among the simulated gates. one of the most important factors that lead to fault tolerance in QCA is using robust majority gate as well as the use of appropriate clocking allocation in a circuit. When this structure is used in QCA, it seems causes to increase distance between adjacent wires in a module and this cause less impact of wires to each other and consequently growing the range of fault tolerance in QCA circuits.

in previous section was observed that gates have different sensitivity against defects but after using fault tolerant basic blocks in QCA circuits in addition to improving reliability of all gates against defects, fault sensitivity come very close and any gate in comparison of other gate don't has obvious advantage (Fig 9). In previous section, this result was obtained that Mahdiani et al gate has better resistance and was the most fault tolerant gate with accessible inputs and output. However, with improvement that be done on all gates, not only this gate but also other gates show less sensitivity that it also causes to closing the gate sensitivity against defect to each other.

Table 2. Summery of Improved xor gates properties

#	DESIGN NAME	# Of Cells Before Robustness	# Of Cells After Robustness	Persentege Of Redundancy Of Cells	Area Before Robustness (um^2)	Area After Robustness (um^2)	Delay Before Robustness (Clk)	Delay After Robustness (Clk)	I/O Accessibility
1	Shah [29]	35	66	60%	0.02	0.09	1	1	Yes-No
2	Roohi [31]	29	49	68%	0.03	0.09	1	1	No-Yes
3	Suresh [30]	45	60	33%	0.03	0.10	0.75	1	No-Yes
4	Mustafa [32]	41	50	22%	0.04	0.08	1	1	No-Yes
5	Mahdiani 1 [33]	45	68	51%	0.05	0.15	1	1.75	Yes-Yes

According to table 2, it is clear that when using this technique to improve the defect tolerability in circuits we face to some redundancy in the number of cells and in the clock phases, but this redundancy is worth to increase fault tolerance that created. On the other hand, according to these tables and also approaching the fault tolerance level of circuits to each others, they don't have significant differences in sensitivity. the Mahdiani gate due to the accessibility of inputs and output has higher fault tolerance level than other gates because the implementation of other's gate is single-layer in appearance and multilayer in practical, but the Mahdiani gate, despite the made improvements has the higher delay than the other gates but practically is a single layer, because the inputs and output are not restricted and can be said that by improving be done and according to parameters presented have the higher level of fault tolerance.

The level of fault tolerance against missing cell have been evaluated. After the improvements made in the circuits, it can be seen that the circuit resistance to this defect has also increased. Simulation results show that using robust majority gate made circuit more resistance against this defect.

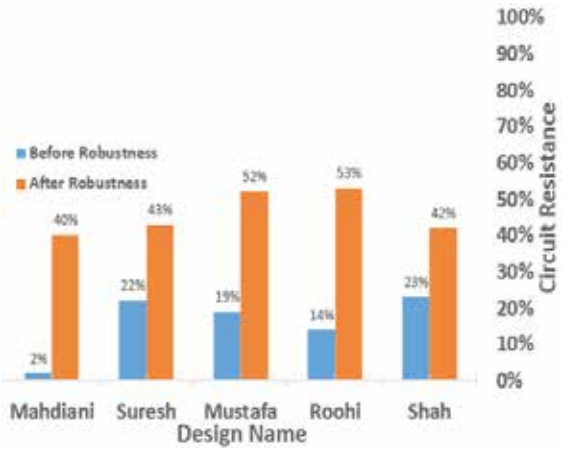

Fig.9. Fault sensitivity evaluation of improved XOR gates in comparison of each other

VII. CONCLUSION

A new defect terminology and some of fault tolerant techniques is introduced in the paper. Then XOR gate as an important basic building block were tested in front of a common defect in QCA and one of fault tolerant techniques were applied to them to design fault tolerant logic gates. Simulation results show that using Robust Majority Gate and design of single layer circuits in QCA can create fault tolerant circuits like XOR gates that examined in this paper.

ACKNOWLEDGMENT

The author would like to thank Dr. Hamid Reza Mahdiani for his kind advice throughout this research.

REFERENCES

[1] G. E. Moore, "Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp. 114 ff."Solid-State Circuits Newsletter, IEEE 11.5 (2006): 33-35.

[2] Mehdi Baradaran Tahoori, Mariam Momenzadeh, Jing Huang, Fabrizio Lombardi, "Defects and Faults in Quantum Cellular Automata at Nano Scale", Department of Electrical and Computer Engineering, Northeastern University, Boston, MA, 02115, Proceedings of the 22nd IEEE VLSI Test Symposium (VTS 2004)

[3] Craig S Lent, P Douglas Tougaw, Wolfgang Porod and Gary H Bernstein, "Quantum cellular automata", Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556, USA, Received 1 August 1992, accepted for publication 24 December 1992

[4] Kyosun KIM, Member, Kaijie WU, and Ramesh KARRI, "Quantum-Dot Cellular Automata Design Guideline", 2006 The Institute of Electronics, Information and Communication Engineers, IEICE TRANS. FUNDAMENTALS, VOL.E89–A, NO.6 JUNE 2006

[5] Weiqiang Liu, Liang Lu and M´aire O'Neill Earl E. Swartzlander Jr, "Design Rules for Quantum-dot Cellular Automata", 2011 IEEE

[6] K. Navi, S.Sayedsalehi, R.Farazkish, M.Rahimi Azghadi, Five-input majority gate, a new device for quantum-dot cellular automata ,J. Comput. Theor. Nanosci. 7(2010)1546–1553.

[7] X.Yang,L.Cai,X.Zhaho,N.Zhang, Design and simulation of sequential circuits in quantum-dot cellular automata: falling edge-triggered flip-flop and counter study, Microelectron.J.41(2010)56–63 (Elsevier).

[8] M. Lieberman, S. Chellamma, B. Varughese, Y. Wang, C.S. Lent, G.H. Bernstein, G. Snider and F. Peiris, "Quantum-Dot Cellular Automata at a Molecular Scale", Annals of the New York Academy of Sciences, vol. 960, pp. 225-239, 2002.

[9] MICHAEL CROCKER, MICHAEL NIEMIER, X. SHARON HU, and MARYA LIEBERMAN, "Molecular QCA Design with Chemically Reasonable Constraints", ACMJournal on EmergingTechnologies in Computing Systems,Vol. 4, No. 2,Article 9, Publication date: April 2008

[10] JIANWEI DAI and LEI WANG University of Connecticut and FABRIZIO LOMBARDI Northeastern University, "An Information-Theoretic Analysis of Quantum-Dot Cellular Automata for Defect Tolerance", ACM Journal on Emerging Technologies in Computing Systems, Vol. 6, No. 3, Article 9, Pub. date: August 2010.

[11] A. Orlov, A. Imre, G. Csaba, L. Ji, W. Porod, and G. H. Bernstein, "Magnetic Quantum-Dot Cellular Automata: Recent Developments and Prospects," Journal of Nanoelectronics and Optoelectronics Vol.3, 1–14, 2008

[12] V. Vankamamidi, M.Ottavi, F.Lombardi,Two-dimensional schemes for clocking/timing of QCA circuits, IEEE Trans. Comput.Aided Des. Integr.Circuits Syst. 27(2008)34–44.

[13] Kunal Das, Debashis De, "QCA Defect and Fault Analysis of Diverse Nanostructure for Implementing Logic Gate", International J. of Recent Trends in Engineering and Technology, Vol. 3, No. 1, May 2010

[14] Mojdeh Mahdavi, Mohammad Amin Amiri, Sattar Mirzakuchaki, and Mohammad Naser Moghaddasi, "Single Electron Fault Modeling in QCA Inverter Gate", Canadian Journal on electrical & Electronics Engineering Vol. 1, No. 1, February 2010

[15] M. Mahdavi, S. Mirzakuchaki, M.N. Moghaddasi, M.A. Amiri, "Single electron fault modelling in quantum binary wire," Micro & Nano Letters, 2011, Vol. 6, Iss. 2, pp. 75–77

[16] P. D. Tougaw and C. S. Lent, "Effect of stray charge on quantum cellular automata," Jpn. J. Appl. Phys., vol. 34, pp. 4373–4375, 1995.

[17] Mehdi Askari and Maryam Taghizadeh and Khossro Fardad, "Digital Design Using Quantum-Dot Cellular automata (A Nanotechnology Method)", 1Department of computer and Electrical Engineering, Islamic Azad University, Omeidyeh, Iran 2Department of computer, Islamic Azad University, Behbahan, Iran, Proceedings of the International Conference on Computer and Communication Engineering 2008

[18] J. Huang, M.Momenzadeh, L. Schiano and F. Lombardi, "Simulation-based Design of Modular QCA Circuits", Proc. IEEE Conference on Nanotechnology, PaperWE-P7-1, IEEE CD-ROM 05TH8816C, Nagoya, 2005.

[19] T. Cole, J.C. Lusth, "Review Quantum-dot cellular automata, Department of Mathematics and Computer Science", Boise State University, Boise ID 83725, USA, 2001 Elsevier Science Ltd

[20] Razieh Farazkish, "A new quantum-dot cellular automata fault tolerant five-input majority gate", J Nanopart Res (2014)

[21] J. Huang, M. Momenzadeh, F. Lombardi, " Analysis of missing and additional cell defects in sequential quantum-dot cellular automata," INTEGRATION, the VLSI journal 40 (2007) 503–515.

[22] Xiaokuo Yang, Li Cai, Shuzhao Wang, Zhuo Wang, and Chaowen Feng, "Reliability and Performance Evaluation of QCA Devices With Rotation Cell Defect", IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 11, NO. 5, SEPTEMBER 2012

[23] Mariam Momenzadeh, Jing Huang, Mehdi B. Tahoori, and Fabrizio Lombardi, "Characterization, Test, and Logic Synthesis of And-Or-Inverter (AOI) Gate Design for QCA Implementation", IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, VOL. 24, NO. 12, DECEMBER 2005

[24] Faizal Karim, Marco Ottavi, Hamidreza Hashempour, Vamsi Vankamamidi, Konard Walus, Andre ivanov, Fabrizio Lombardi, "Modeling and Evaluating Errors Due to Random Clock Shifts in Quantum-Dot Cellular Automata Circuits," Journal of Electronic Testing, February 2009, Volume 25, Issue 1

[25] M. Janez, P. Pecar, and M. Mraz, "Layout design of manufacturable quantum-dot cellular automata,"

Microelectronics Journal, vol. 43, pp. 501–513, 2012.

[26] S. Perri, and P. Corsonello, “New Methodology for the Design of Efficient Binary Addition Circuits in QCA,” Nanotechnology, IEEE Transactions on, 11(6), 1192-1200. 2012.

[27] Arman Roohi, RonaldF.DeMara, Navid Khoshavi, “Design and evaluation of an ultra area-efficient fault-tolerant QCA full adder,” Microelectronics Journal 46 (2015) 531–542.

[28] K. Walus, T. Dysart, G. Jullien, and R. Budiman, “QCADesigner: A rapid design and simulation tool for quantum-dot cellular automata,” IEEE Trans. Nanotechnol., vol. 3, pp. 26–31, 2004.

[29] N. Shah, F. Khanday, andJ. Iqbal,“Quantum-dot cellular automata (qca) design of multi-function reversible logic gate,” Communications in Information Science and Management Engineering,2012.

[30] K. Suresh, and G.Bahniman “Ripple Carry Adder Using Two XOR Gates in QCA.” Applied Mechanics and Materials 467, 531-535. 2014.

[31] A. Roohi, H. Khademolhosseini,S. Sayedsalehi, and K.Navi, “A Novel Architecture for Quantum-Dot Cellular Automata Multiplexer.” IJCSI International Journal of Computer Science Issues 8.6: 55-60. 2011.

[32] M. Mustafa, and M. Beigh, “Design and implementation of quantum cellular automata based novel parity generator and checker circuits with minimum complexity and cell count.” Indian Journal of Pure & Applied Physics 51 60-66, 2013.

[33] H. R. Mahdiani, A. R. Hejazi, M. Poorhoseini “ A Fault-Tolerant and Efficient XOR Structure for Modular Design of Complex QCA Circuits” submitted to internatonal journal of circuit theory and applications.