



# Effects on selective epitaxial growth of strained-SiGe p-MOSFETs on various (001) Si recess structures

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## Abstract

Influences of source and drain recess structures on SiGe epitaxy growth, SiGe step height, facet formation,  $I_{D,sat}$  and resistance performance are investigated. Growth rate of SiGe height increases with decreased recess width at a fixed depth of 62 nm. Under a fixed recess width of 96.3 nm, the deeper the recess, the higher the growth rate of SiGe height. An increase in the depth/width ratio of the recessed Si geometry may promote SiGe {001} growth. Upon the recess, SiGe step height is influenced by the initial SiGe orientation. A longer {001} facet of SiGe initial orientation causes a higher growth rate of SiGe step height. Higher  $I_{D,sat}$  and lower resistance can be achieved by increasing SiGe volume with wider recess width, deeper recess depth, and higher SiGe step height.

**Keywords** SiGe · Recess · Facet · SEG

## Introduction

In order to enhance the performance of device speed, selective epitaxial growth (SEG) of SiGe was implanted in the recessed source and drain to provide lateral compressive strain and to increase carrier mobility [2]. The lateral compressive strain is due to the lattice mismatch between silicon and germanium atoms, which provides an approximately 2 GPa compressive stress near the interface when germanium content is about 20% [2]. Compressive strain increases with increasing SiGe volume by silicon recess depth, width, and SiGe step height. Higher SiGe volume results in higher strain fields, and thus higher drive current [3–5]. A major challenge to the embedded source and drain SiGe stressor is the pattern dependent deposition [6–8]. According to the kinetic gas model, different recess environment or structures may lead to dramatic influence that species are attracted by dangling bonds and cause different

SEG growth rate [8]. The SiGe volume is influenced by the facets driven by growth rate anisotropy in different orientations and sidewall material [9]. The relationship between the growth rates of different SiGe facets and sidewall material are  $R_{001} > R_{112} > R_{119} > R_{018} > R_{113} > R_{110} > R_{111}$  and  $R_{Si} > R_{nitride} > R_{oxide}$ , respectively [10–12].

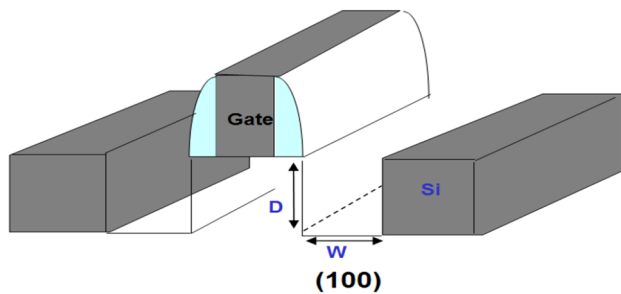
In this paper, the effects of silicon recess geometry and SiGe step height on SiGe epitaxy growth, SiGe facet formation and device performance in a SiGe process-induced strained silicon device are investigated. This result indicates that different depth/width ( $D/W$ ) ratio in U-sharp recess can result in different levels of influence in device performance. This paper could provide useful information when embedded SiGe in recessed source and drain area is used for enhancing MOSFET performance.

## Experiment

A commercially available reduced-pressure chemical vapor deposition tool was used for the selective epitaxial growth (SEG) of  $Si_{80}Ge_{20}$  on the U-shape Si recessed source and drain regions prepared by using reactive-ion etching (RIE) with (100) silicon wafers. As shown in Fig. 1, various recess width and depth samples are prepared for this study.

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**Fig. 1** Cross-section of recessed source/drain regions for SiGe growth in a MOS transistor

The reactor system has upper and lower lamp-heating modules with optical pyrometer temperature sensors.  $\text{SiCl}_2\text{H}_2$  and diluted  $\text{GeH}_4$  (20%) are the source gases for the SiGe epitaxial growth and  $\text{H}_2$  is used as the carrier gas. The deposition temperature ranges from 600 to 800 °C at a deposition pressure of 10–20 Torr using 20 sccm  $\text{SiCl}_2\text{H}_2$ , 10 sccm  $\text{GeH}_4$ , and 300 sccm  $\text{H}_2$  flow.

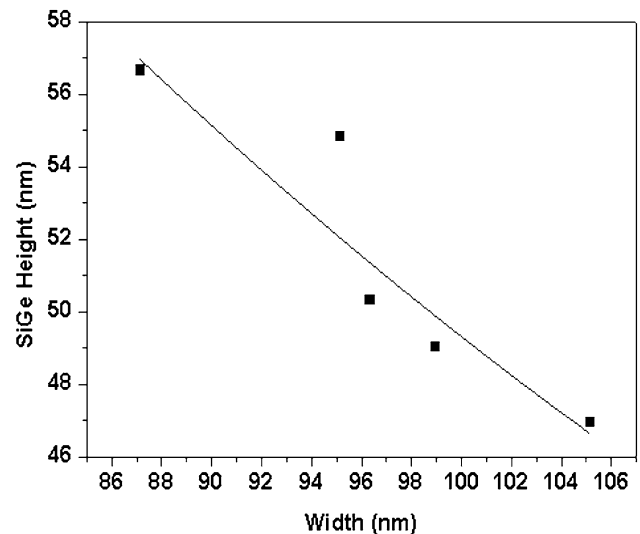
In order to observe the facet formation, a 3-s silicon marker deposition is inserted after a 27-s SiGe deposition. Under the above described deposition conditions, thickness (or height) of the SiGe layer is measured from the cross-sectional image taken from a transmission electron microscopy (TEM). Secondary ion mass spectrometry and high resolution X-ray diffractometer (HRXRD) are used to measure the germanium atomic content while the stain of SiGe layer is measured using nanobeam electron diffraction (NBD) technique. Finally, the device parameters are tested to analyze the electrical response of the different conditions.

## Results and discussion

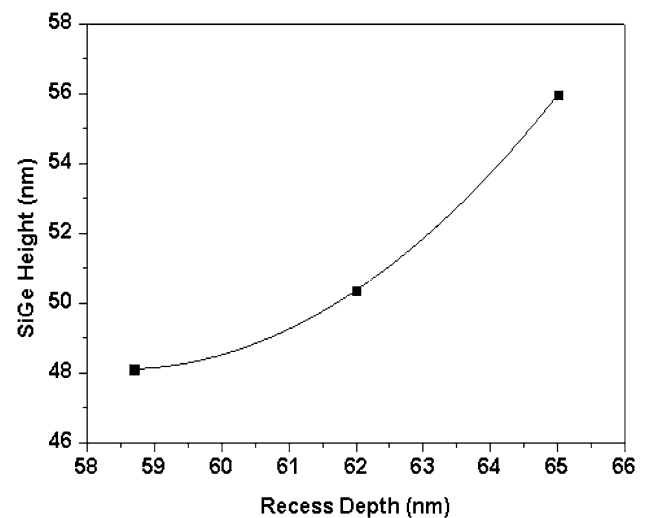
Under a fixed depth of 62 nm, smaller width leads to decreased volume of the recess region. Figure 2 shows that SiGe height (measured after four deposition cycles) increases with decreased recess width. And the deeper the recess, the higher the SiGe height for a fixed recess width of 96.3 nm as is shown in Fig. 3.

For better understanding, SiGe height is plotted against the recess depth/width ( $D/W$ ) ratio as shown in Fig. 4. It indicates that SiGe height increases with recess  $D/W$  ratio. The growth rate ( $R$ ) of SiGe height at different geometry can be explained by the facet. Figure 5 shows the cross-sectional TEM images of the morphology of the SiGe layers deposited in between Si sidewalls with various recess  $D/W$  ratios. The relationship between SiGe growth rates on different Si facets is  $R_{111} < R_{113} < R_{001}$ .

In Fig. 5a, the  $D/W$  ratio is 0.61 and SiGe height is 48.1 nm, the length of the {111} and {113} facets are 20.5



**Fig. 2** SiGe height versus recess width at a fixed depth of 62 nm



**Fig. 3** SiGe height versus recess depth under a fixed width of 96.3 nm

and 20.5 nm, respectively. In Fig. 5b, the  $D/W$  ratio is 0.64 and SiGe height is 50.4 nm, the length of the {111} and {113} facets are 15.8 and 15.4 nm, respectively. As a result, a high  $D/W$  ratio has lower influence on {111} and {113} facets, which is beneficial to the SiGe height {001} facet growth.

Unlike silicon sidewalls, the top sidewalls of the recess are nitride films which cannot grow SiGe film. The growth rate of SiGe step height is influenced by initial {001} SiGe facet length (measured the fifth Si marker). In Fig. 6, the step height of cycle five to six (above the recess) increases with longer initial {001} SiGe facet length. Figure 7 shows the cross-sectional TEM images of the morphology of the SiGe step height deposited in between nitride sidewalls with long and short initial {001} SiGe facet length. In

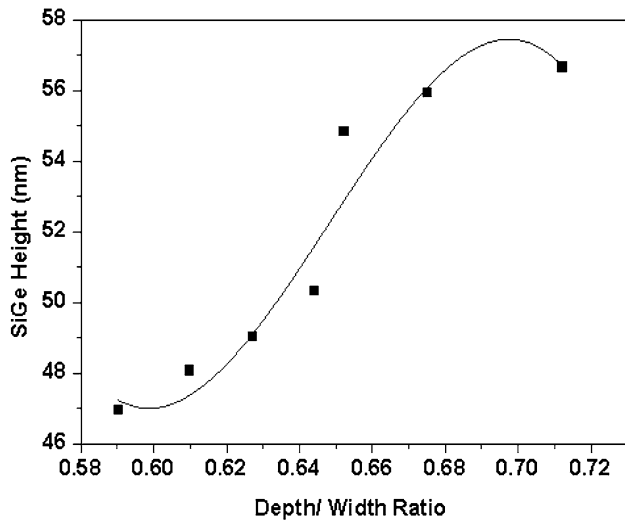


Fig. 4 SiGe height versus the recess depth/width ratio

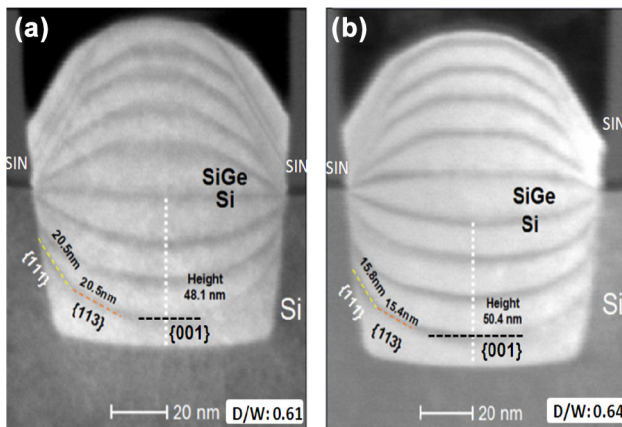


Fig. 5 a  $D/W$  ratio 0.61,  $\{111\}$  20.5 nm and  $\{113\}$  20.5 nm. b  $D/W$  ratio 0.64,  $\{111\}$  15.8 nm and  $\{113\}$  15.4 nm

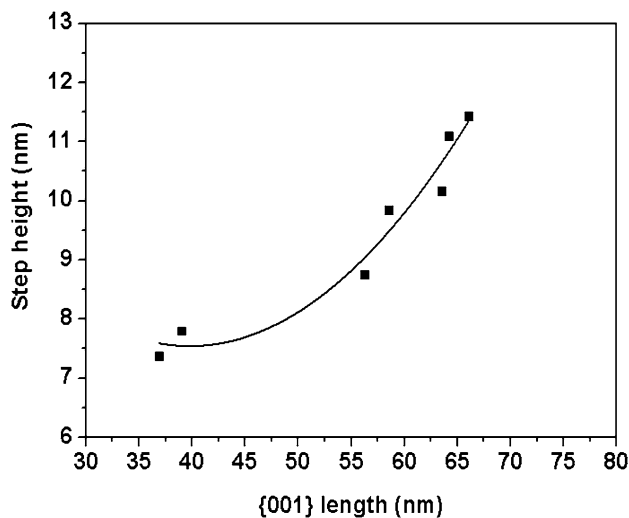


Fig. 6 SiGe step height versus  $\{001\}$  length (measured from cycle 5 to cycle 6)

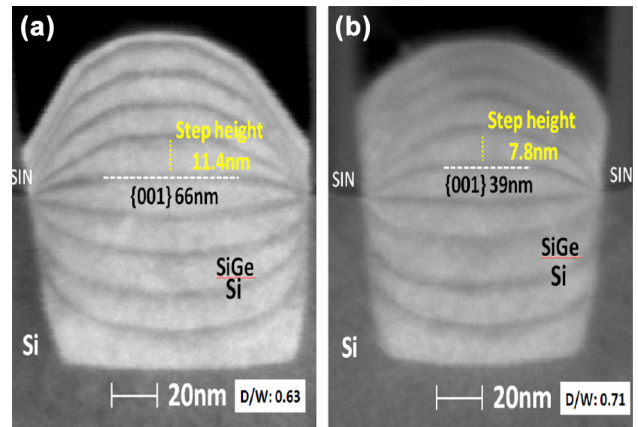


Fig. 7 TEM cross-sectional images of the fabricated recess with  $D/W$  ratio of a 0.63 and b 0.71

Fig. 7a, the initial  $\{001\}$  SiGe facet length is 66 nm and the step height of cycle 5 to cycle 6 is 11.4 nm. In Fig. 7b, the initial  $\{001\}$  SiGe facet length is 39 nm and the step height of cycle 5 to cycle 6 is 7.8 nm. The initial  $\{001\}$  SiGe facet length influence the growth rate of step height.

Figure 8 shows the TEM image of SiGe film grown on a blanket wafer without a faceting effect. The one cycle SiGe step height is 12.3 nm, which is higher than the recessed source and drain regions.

The strain, measured by NBD technique, on silicon walls caused by the SiGe film deposited in the recess region ( $D/W$  ratio 0.63) is shown in Fig. 9. The strain on silicon walls is  $-0.5\%$  while the average strain of the SiGe film itself is  $+1.0\%$ . It indicates that the SiGe film provides 1.5% compress strain to the silicon channel.

The impacts of the recess width and recess depth on the drive current and resistance are given in Figs. 10, 11, 12, 13. In Figs. 10 and 11, a wider recess width has a higher

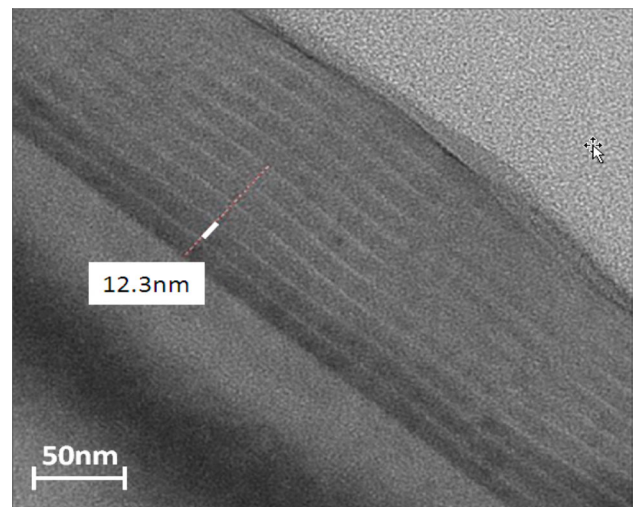
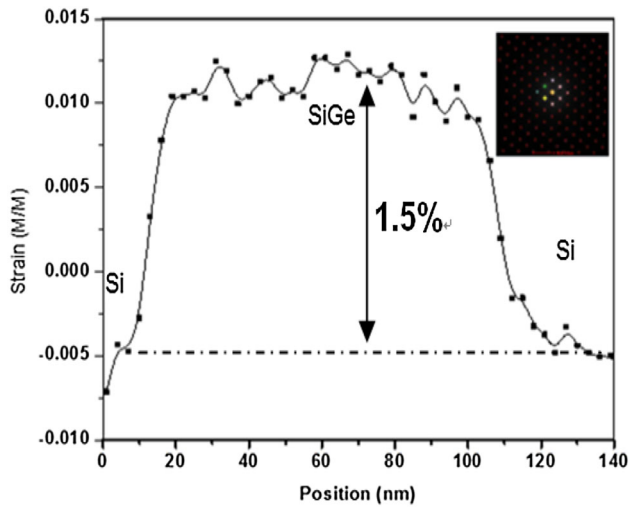
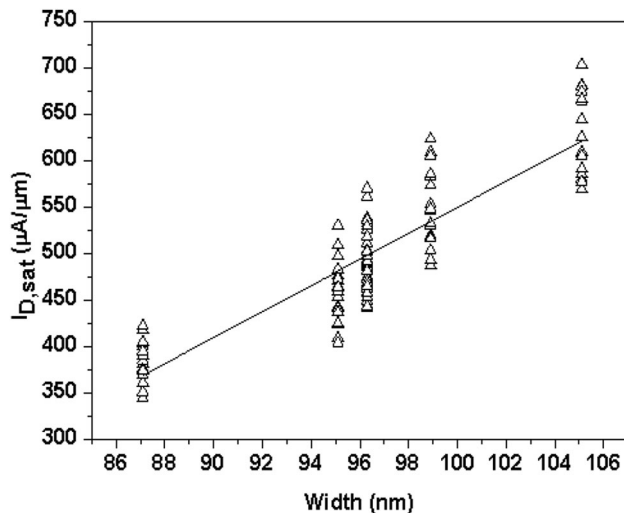


Fig. 8 Cross-section of SiGe growth in blanket wafer

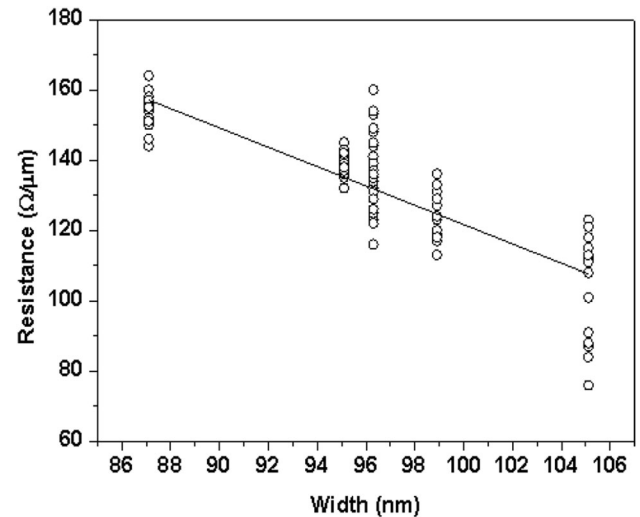


**Fig. 9** Compress strain to Si by the SiGe layer deposited in the Si recess, the strain was measured by NBD. ( $D/W$  ratio 0.63)

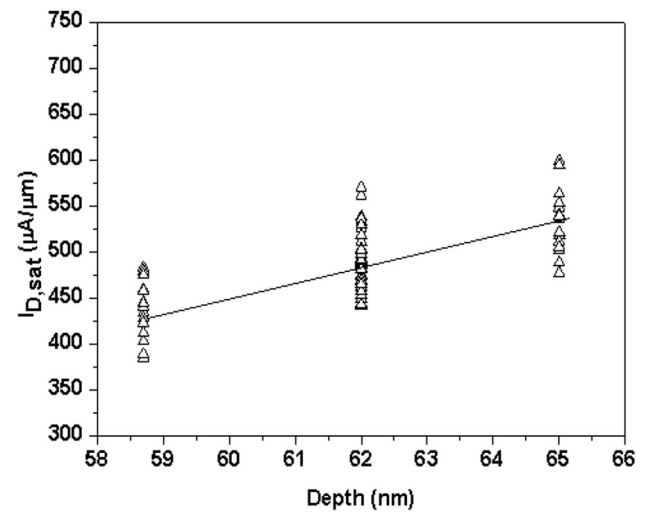


**Fig. 10** SiGe  $I_{D,sat}$  versus recess width at a fixed depth of 62 nm

drive current and lower resistance under a fixed depth of 62 nm. According to the result of strain simulation about advanced sigma-shape recessed structures, there are two key structure factors affect device's performance. One is the distance between the sigma-shape recess and its channel region; another is tip depth [13]. In simple U-shape recess structure, only the distance between the U-sharp recess and its channel region is significant in structure's influence. Larger SiGe volume (wider U-sharp recess width) and shorter channel to recess distance both lead to higher strain in the channel region and better device performance. In Figs. 12 and 13, a deeper recess has a higher drive current and lower resistance under a fixed recess width of 96.3 nm. They suggest that larger SiGe volume in the recessed source and drain regions could provide higher



**Fig. 11** SiGe resistance versus recess width at a fixed depth of 62 nm



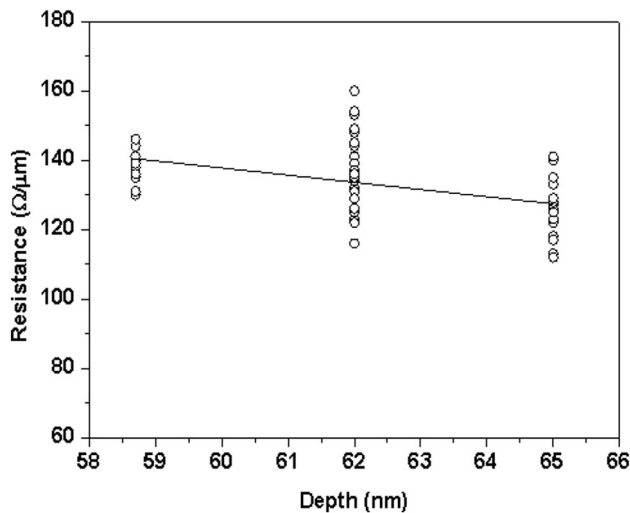
**Fig. 12** SiGe  $I_{D,sat}$  versus recess depth under a fixed width of 96.3 nm

compressive stress and lower resistance to the transistor channel and result in higher  $I_{D,sat}$ .

## Conclusions

The influences of recess width, recess depth, and orientation effects on the step height of SiGe epitaxy are investigated. Based on these results, recess depth/width ( $D/W$ ) ratio plays an important role in facet formation. It also influences the SiGe growth in the silicon recessed region. Higher  $D/W$  ratio has a higher SiGe step height. SiGe step height depends on the initial {001} SiGe facet length above the recess, in which a longer initial length has a higher SiGe step height. SiGe epitaxy in the recessed source and drain regions provides higher compressive strain to the channel





**Fig. 13** SiGe resistance versus recess depth under a fixed width of 96.3 nm

and increases the carrier mobility for enhancing transistor performance. Hence drive current increases and resistance decreases with increased recess width, recess depth, and SiGe step height.

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