A QCA Fault-Tolerant Reversible Full Adder

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Abstract

Today, the use of CMOS (Completely Metal-Oxide Semiconductor) technology for manufacturing electronic ICs has faced many limitations. Many alternatives to CMOS technology are offered and made every day. Quantum-dot cellular automata (QCA) is one of the most widely used. QCA gates and circuits have many advantages including small size, low power consumption, and high speed. On the other hand, using special digital gates called reversible gates, a series of reversible circuits can be built that have their advantages and applications in digital design. QCA gates can implement reversible circuits. One of the most important reversible gates implemented by QCA gates is the QCA1 gate. In this paper, we proposed a reversible full adder using QCA1 gates with a fault-tolerant structure. Fault tolerance is an important factor in QCA structures. This structure has better indexes such as area and latency than similar ones. Reversible circuits are a kind of intelligent system; because the output values can distinguish the possible system error. The proposed reversible full adder has 350 gates and 2 clock cycles which is much less latency than previous works.

Keywords: Reversible gate, QCA1 gate, Intelligent system, Fault-tolerant
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1. Introduction

Gordon Moore from Intel Company predicted that the number of transistors on chips doubles approximately every two years. This prediction surprisingly has been accurate for more than 40 years and it is known as Moor's law. The number of transistors in CMOS technology follows Moor's law. To achieve a circuit with higher speed and lower power consumption, the size of the transistor should be decreased. However, as this technology moves below sub-micron levels, many problems arise. Some physical limitations like quantum effect, unpredictable behavior in low currents, and some limitations which are related to this technology such as power consumption, design, and lithography complexity prevent the development of micro-electronic systems that follow Moor's law. Therefore, there is a need for a new technology to code the binary information. For developing new and practical technologies for designing Nano-scale circuits, some new solutions should be considered. Technologies such as single-electron transistors, Nano Carbon tubes, molecular switches, etc. are some of the possible solutions. Also, in recent years many researchers have been investigating to design of Nano-scale circuits using Quantum Cellular Automata (QCA) technology, and scientists and designers of the digital circuit hope that CMOS will be replaced with this novel technology. So, in this technology, we have basic digital gates, and using these gates, any digital circuit could be designed.

The most commonly used QCA gates and how they work are described in [1] (such as NOT, OR, and AND gates). Small and basic QCA structures such as majority gate [2], inverter [3], and comparator [4] are designed and proposed on many papers in different ways. More complex circuits such as BCD adder [5], ALU [6], SRAM [7], and cryptographic elements [8] are implemented by QCA gates in previous papers too.

Full adder is one of the most popular combinational logic circuits that is widely used in digital circuits and many complex circuits using this. So, designing optimal circuits for full adder is of particular importance. QCA full adders' structure are so various. D. Kumar and D. Bravo in [9] have proposed one QCA structure for full adder that is implemented by fault-tolerant majority gate. A five-input majority gate is proposed in [10] and used for

implementing a full adder. M. Mohammadi and S. Gorgin in [11] designed a QCA full adder and a 16-bit ripple carry adder is proposed using that. An adder/subtractor is proposed in [12].

A lot of defects may occur during the manufacturing of QCA ICs. The most important defects are cell displacement, cell misalignment, and cell missing [13]. More types of defects are also presented today, such as rotation cell defects [14] and single electron defects [15]. Extra cell deposition and double cell missing are two defects that have been addressed recently in some articles [3].

Reversible computing is a new solution at the logic level. Reversible gates use quantum concepts to create reversible circuits. The basis of this circuit is a one-to-one mapping between inputs and outputs. Basic reversible gates such as NOT, CNOT, CCNOT, and a few more reversible gates are introduced in [16] and their truth table has been expressed. Reversible gates and circuits are just one concept that can be implemented with any technology. One way is to use QCA structures. D. Banik, J. Mathew, and H. Rahaman [17] have designed a D flip-flop with the Friedkin reversible gate and then implemented the structure with QCA cells, which yielded good simulation results. In [18], a 2*2 crossbar switch based on reversible circuits is proposed and then implemented with QCA cells. At the rest of [18], two structures for reversible multiplexer and demultiplexer based on this switch have been described and their possible QCA defects analysis has been performed. QCA1 and QCA2 are two very important reversible structures that are presented in [19]. These gates are used as the main gate in many reversible circuits. For example, a reversible decoder is implemented in [20] using a QCA1 gate.

A reversible gate named NRG is proposed in [21] and a reversible full adder is proposed using this gate. B. Sen and M. Dutta have introduced a reversible multiplexer in [22] and a reversible full adder is designed in the rest of their paper. A reversible full adder is proposed in [23] too.

One of the most important digital circuits in the construction of digital circuits and computers is the full adder. Because defect is an important factor in the correct operating of QCA circuits, in this paper, we are trying to introduce a QCA full adder that, unlike the previous articles, is also focused on being fault tolerant. Due to the advantages of reversibility of digital circuits that are explained in the rest of the paper, we have considered this full adder as reversible. This aspect of QCA circuits has not been investigated recently.

This paper is organized as follows. Section 2 includes the basic concepts of QCA, popular QCA gates, QCA defects, clocking, and reversible gates. We proposed our reversible full adder in section 3. In the rest of this section, we upgrade the proposed reversible full adder to a fault-tolerant one. Finally, the conclusion is in section 4.

2. Background

A QCA cell consists of four quantum dots positioned at the corners of a square and contains two free electrons. The two free electrons can quantum-mechanically tunnel among the dots and settle either at polarization P=-1 or in P=+1 as shown in **Fig.1**. A QCA cell with polarization P=-1 denotes the logic 0 state and with polarization P=+1 denotes the logic 1 state of the cell. In all figures, rectangles denote a QCA cell and the circles inside denote the electrons (or place of electrons) in that cell.

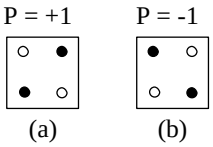


Fig. 1. QCA cell (a) logic 1 state (b) logic 0 state

In Fig. 2, two common QCA wire structures are shown. Two possible wire-crossing are also can be seen in Fig. 3. A majority gate and its truth table are shown in Fig. 4. Fig. 5 shows a specific structure of several possible structures of QCA NOT, AND, and OR gates achieved by fixing one of the inputs of the majority gate at 0 or 1 [9].

Fig. 2. (a) QCA binary wire (b) QCA inverted wire

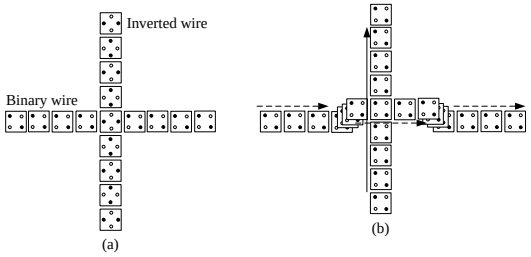
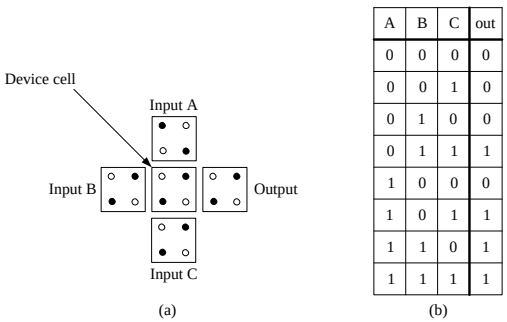


Fig. 3. Wire-crossing in QCA (a) coplanar (b) multilayer



A	B	C	out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Fig. 4. a) The three-input majority gate (b) truth table of gate

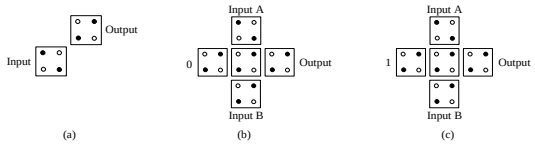


Fig. 5. A few examples for QCA gates (a) NOT gate (b) AND gate (c) OR gate

Many defects can occur during the process of making QCA circuits. Because the dimensions are in nanometers, the probability of defect goes even higher. These defects generally occur at the chemical and deposition stages. Defects mainly can be categorized as cell displacement, cell misalignment, and cell missing. Cell displacement is a defect in which the defective cell is displaced from its original direction. Fig. 6(b) shows this type of cell displacement in a majority gate. In cell misalignment, the direction of the defective cell is misplaced. Fig. 6(c) shows this type of defect in a majority gate. Cell missing is a defect in which a particular cell is missing, as compared to a defect-free arrangement. Fig. 6(d) shows a cell missing defect [13]. A fault-tolerant majority gate is shown in Fig. 7 [24].

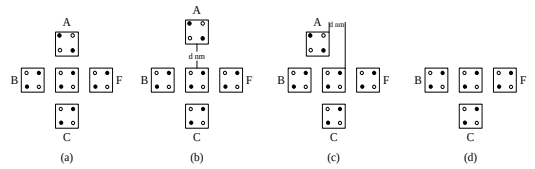


Fig. 6. Defects of QCA structures (a) Fault free (b) cell displacement (c) cell misalignment (d) cell missing [13]

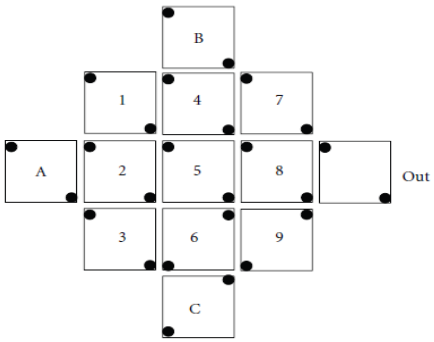


Fig. 7. Fault-tolerant majority gate [24]

A very important issue to consider in the construction of QCA circuits is the concept of timing. At any point in time, each QCA cell can be switched to one of four consecutive phases: switch, hold, release, and relax which are 90º phase differences. Those four phases are shown in Fig. 8 and a color is assigned to each phase [4].

The clock changes phase when the potential barriers that affect a group of QCA cells (referred to as a clocking zone) are raised or lowered or remain raised or lowered. During the switch phase, the inter-dot barrier is gradually raised, and the QCA cell settles down to one of the two ground polarization states as influenced by its neighbors. During the hold phase, the inter-dot barrier is held high, suppressing electron tunneling and maintaining the current ground

polarization state of the QCA cell. During the release and relax phases, the inter-dot barriers are lowered, and the excess electrons gain mobility. In these two phases, a QCA cell remains unpolarized. Overall, the polarization of a QCA cell is determined when it is in its switch phase by the polarizations of its neighbors that are in switch and hold phases. The unpolarized neighbors in the release and relax phases do not affect determining the state of the QCA cell. The clock signals (through an induced electric field) can be generated by CMOS wires embedded below the QCA plane.

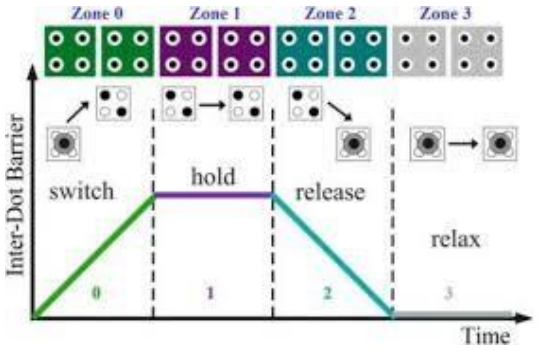
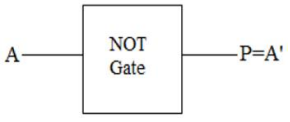


Fig. 8. Clocking in QCA has four phases.

Reversible gates and circuits are new concepts in quantum. Each reversible gate must have two properties. At first, the number of inputs and outputs should be equal. Another property is if the gate is repeated two or more times, the output should equal to input. It means this is possible to determine from the output of each gate or a reversible circuit what the input was. So, the truth table of each gate is unique in each row. There are several types of reversible gates, but we are considering some of them here.

Fig. 9 shows the reversible NOT gate and its truth table. The gate has one input and one output. The reversible CNOT gate and its truth table have been seen in Fig. 10. Sometimes, there are one or more direct outputs without changing the input in reversible gates called garbage. This output is only due to the requirement of an equal number of inputs and outputs. Fig. 11 shows the reversible CCNOT (Toffoli) gate and its truth table [16].

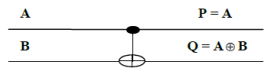


(a)

Input	Output
A	A'
1	0
0	1

(b)

Fig. 9. (a) Reversible NOT gate (b) truth table

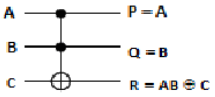


(a)

Input		Output	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

(b)

Fig. 10. (a) Reversible CNOT gate (b) truth table



(a)

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

(b)

Fig. 11. (a) Reversible CCNOT gate (b) truth table

The combination of reversible gates can make reversible circuits. In Fig. 12, we see schematically several reversible gates that are aligned to form a reversible circuit. Their advantage is the ability to detect the fault in the output of each block or the final output of the circuit based on the unique property of the correct table of each reversible gate in each row. By comparing the output of each block with the next block input and comparing it with the inputs and outputs of the before and after blocks, we can detect the fault at each step.

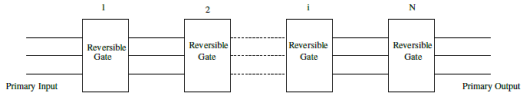


Fig. 12. Schematic of a reversible circuit

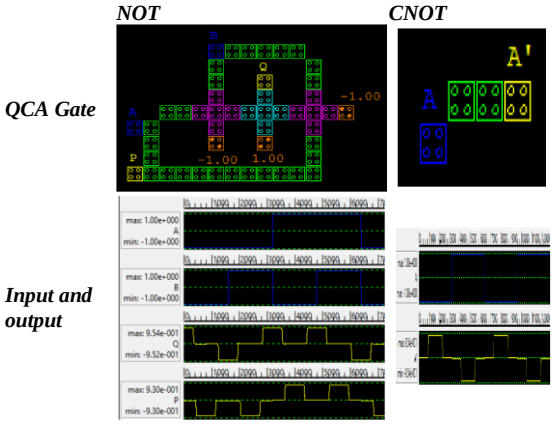


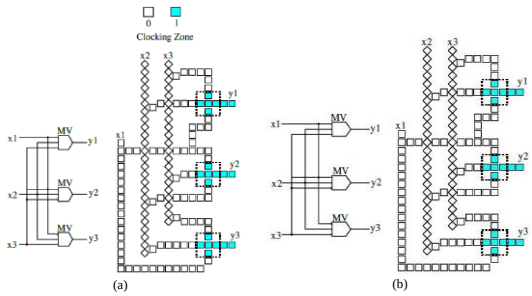
Fig. 13. Two reversible gates implemented by QCA and their simulation in QCADesigner

All reversible gates and circuits can be implemented in the QCA platform. Simulation of two NOT and CNOT gates with their outputs in QCADesigner software are shown in Fig. 13. As a result, all issues related to QCA circuits, including faults, can also be investigated in reversible circuits.

Two common structures in reversible gates are QCA1 and QCA2. Fig. 14 shows these gates. These two structures are widely used in the manufacture of reversible circuits. The input and output relationship of QCA1 and QCA2 gates are according to Eq. (1) and Eq. (2), respectively. The "M" notation in these equations means the majority of inputs [19].

$$\begin{cases} y1 = M(x1,x2,x3) = x1x2 + x2x3 + x1x3 \\ y2 = M(x1,x2,\overline{x3}) = x1x2 + x2\overline{x3} + x1\overline{x3} \\ y3 = M(\overline{x1},x2,x3) = \overline{x1}x2 + x2x3 + \overline{x1}x3 \end{cases} \quad (1)$$

$$\begin{cases} y1 = M(x1,x2,x3) = x1x2 + x2x3 + x1x3 \\ y2 = M(x1,x2,\overline{x3}) = x1x2 + x2\overline{x3} + x1\overline{x3} \\ y3 = M(\overline{x1},x2,\overline{x3}) = \overline{x1}x2 + x2\overline{x3} + \overline{x1}\overline{x3} \end{cases} \quad (2)$$



(a) (b)

Fig. 14. Schematic and layout of (a) QCA1 gate (b) QCA2 gate

3. Proposed fault-tolerant reversible full adder

Based on the QCA1 reversible gate shown in Fig. 14, the description of the reversible circuits described in the previous section, and the input and output relationships of this gate described in Eq.(1), schematic of a reversible full adder can be obtained according to Fig. 15 by two QCA1 series gates. The truth table is shown in Table 1. The advantage of a reversible full adder based on a truth table is the main property of the reversible circuits (each row of the truth table is unique). So, this will be very helpful in detecting an output error, especially for larger multi-bit full adders. After repeating the proposed full adder twice, the output will be equal to the input. This property will help to easily identify possible output errors.

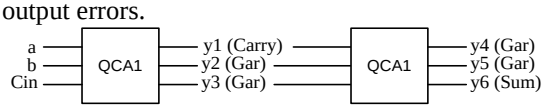


Fig. 15. Schematic of a reversible full adder (Gar in figure means garbage output)

Table.1.
The truth table of a reversible full adder

a	b	Cin	y1(Carry)	y2	y3	y4	y5	y6(Sum)
0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	0	1
0	1	0	0	1	1	1	0	1
0	1	1	1	0	1	1	0	0
1	0	0	0	1	0	0	1	1
1	0	1	1	0	0	0	1	0
1	1	0	1	1	0	1	1	0
1	1	1	1	1	1	1	1	1

This reversible full adder can be implemented with QCA technology. The QCA1 gate is manufactured from a combination of three majority gates and two NOT gates, as shown in Fig. 14 and Eq(1). So any QCA structure for the majority and NOT gates can be used to construct the QCA1 gate and eventually the entire reversible full adder. Here we have used the fault-tolerant majority gate structure shown in Fig. 7 to make our proposed fault-tolerant reversible full adder (Fig. 16) against cell displacement, cell misalignment, and cell missing defects. In Fig. 16, the fault-tolerant is done by placing the fault-resistant majority gate.

The simulation of all QCA designs is done in the QCADesigner software. The proposed reversible full adder was simulated in the QCADesigner V2.0.3 simulation tool. For accuracy, the coherence vector engine was employed. This is a quantum mechanical engine using the Jacobi algorithm to calculate the values/vectors of the Hamilton matrix. Fig. 17 shows the simulation results. All cells in the simulation have 18*18nm cell size and the distance between neighboring cells is 2nm.

Table 2 shows a comparison of QCA reversible full adders. It is seen that our proposed fault-tolerant full adder is superior to similar works in terms of different parameters. Our proposed reversible full adder has 350 gates which is less than [22] and [23]. But it has more gates than [21]. Instead, our reversible full adder has 2 clock cycles which is much less latency than [21], [22], and [23]. We know latency is very important in QCA circuits.

Wire-crossing is the coplanar mode in our proposed reversible full adder, so the structure has only one layer. This is a very important issue in manufacturing. Multilayer wire-crossing can't be manufactured in QCA technology. According to Table 2, in terms of area, our proposed fault-tolerant full adder is properly compared with similar works.

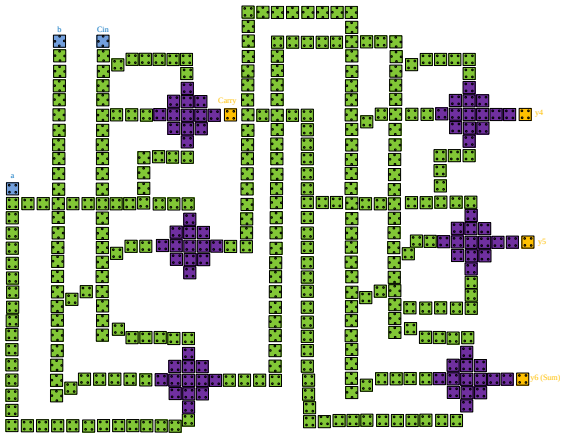


Fig. 16. QCA layout for proposed fault-tolerant reversible full adder (by NOT gate, majority gate, and wiring)

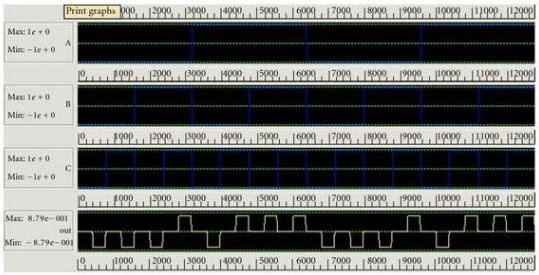


Fig. 17. Simulation results of the proposed fault-tolerant reversible full adder by QCADesigner

Table.2.
A comparison of QCA reversible full adders

Full adder	*Cells*	*Layers*	*Area (μm^2)*	*Latency (clock cycles)*	*Constant inputs*	*Garbage outputs*
[21]	221	1	0.38	5.00	0	2
[22]	612	1	0.96	4.00	3	3
[23]	355	2	0.42	3.40	0	3
Proposed	350	1	0.35	2.00	0	2

The number of constant inputs and garbage outputs are two important issues in reversible circuits. Their large numbers can increase the complexity of the circuit in construction .According to Table 2, we have seen our proposed reversible full adder has less constant input and garbage output than similar works.

Our proposed reversible full adder is fault-tolerant, while others are not. The only major gate used in our proposed structure must be the majority gate. So, the manufacturing process will be easier, whereas in other full adders that are made of different gates, the fault-tolerant process and manufacturing process will be more complex. QCAPro [25] is an energy estimator tool that evaluates the leakage, switching, and total energy dissipations of the QCA circuits. Table 3 represents the energy dissipation analysis of our proposed fault-tolerant reversible full adder and similar works listed in Table 2. The simulations are performed in three distinct tunneling energy levels (0.5, 1, and 1.5 Ek) considering 2 K as the operational temperature.

By using this full adder, multi-bit adders and finally, more complex digital circuits can be made. With the help of the reversibility of this full adder, the fault can be found and corrected at any stage of the logical process.

Table.3.
The energy dissipation analysis

	Av. Leakage energy dissipation (eV)			*Av. switching energy dissipation (eV)*			*Total energy consumption (eV)*		
	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k
[21]	0.085	0.235	0.452	0.342	0.285	0.259	0.427	0.520	0.711
[22]	0.093	0.241	0.475	0.348	0.301	0.292	0.441	0.542	0.767
[23]	0.094	0.271	0.486	0.354	0.309	0.275	0.448	0.579	0.761
Our work	0.068	0.209	0.376	0.269	0.236	0.203	0.337	0.445	0.579

According to Table 3, it can be easily perceived that our design has much less leakage and switching energy dissipation in different tunneling energy levels in comparison to similar works. In an objective comparison of total energy dissipation (overall vector pairs) to the previously reported reversible QCA full adders listed in Table 2, our proposed design dissipates on average 28%, 28%, and 30% less energy in 0.5Ek, 1Ek, and 1.5Ek tunneling energy levels, respectively.

4. Conclusion

This paper proposed a fault-tolerant reversible full adder using a QCA1 gate that has more advantages in comparison with similar works in terms of indicators such as area, latency, constant inputs, and garbage outputs. More-bit reversible full adders can be made by this proposed fault-tolerant reversible full adder. By reversible full adder, we can recognize the probable fault by comparing inputs and outputs (the truth table of each gate is unique in each row). Since full adders are one of the most important elements in the manufacturing of processors, ideas like this article, in which full adders with higher speed, less area, and reversibility are introduced, more powerful processors can be manufactured.

Power analysis shows our proposed fault-tolerant reversible full adder has less energy consumption than similar works. Because of defects in the QCA layout in the manufacturing process, the outputs may be at fault and thus face major reliability-related problems. So, the majority gate of the proposed reversible full adder is a fault-tolerant majority gate. More fault-tolerant majority gates can be used on the proposed fault-tolerant reversible full adder in the future. There are more defects in the manufacturing process that are not reviewed in this paper. Suggesting circuits that are resistant to more defects can be an idea for future works and improve reliability.

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