Reliability Computation for Single Event Transient on Various Encoder Structures of Flash ADCs

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Abstract

The importance of reliability of digital circuits and the impact of cosmic radiation and single event transient (SET) on circuits, with reducing the technology scaling and operating voltage, is increasing dramatically. In this paper, the reliability of different encoder structures that used in the flash analog to digital converters, were calculated and compared in term of single event transient. The impacts of masking (logic and electrical) and crosstalk effects between interconnects on reliability are considered when evaluating the reliability of SET in this circuits. The results indicate that reliability for SET on Encoder Rom structure is more than other structures. The masking and crosstalk effects will improve the reliability of this circuits by more than 42%.

Keywords: Reliability, Single Event Transient, Encoder, Flash ADC

1. Introduction

In terms of reliability, application of systems divided into two types named critical and non-critical. Obviously, in critical applications, reliability is essential requirement. Today, advances in technology have made the Reliability for non-critical applications is also considered important. The reason is that, the numerous incidence of errors in a system causes the loss of credibility manufacturer and market future products is at risk. Therefore, today the reliability for all applications, including critical and noncritical, is an important parameter [1], [2]. Failure of submicron technology-based circuits can be divided into two parts permanently failures and temporary failures. Among these, failures caused by the collision of energetic particles emitted by cosmic rays and alpha particles into sensitive areas of a semiconductors material, because of the density and distribution of energy, is of particular importance. When a high-energy particles strike the sensitive part of a semiconductor material, a dense channel of electrons and holes is created. The presence of an electric field causes the current carriers moving in the circuit and if they can charge or discharge a capacitor in the hit node, transient voltage pulse is created. If the content of memory element impressed during this operation and its logic is changed, the so-called soft error has occurred. It is reported that in a favorable environment, 90% of failures in a computer system caused by transient failures [3]. For this reason, in assessing the reliability and system failure, transient failure are more important. In general, there is the possibility of collision of

energetic particles with different components of a digital circuit including logic, memory elements and the control signal lines. Figure 1 shows different parts of the circuit and different modes of influence of particle collisions. Particle collision to a logic gates produce and inject charge that after passing through the logic circuits, Cause transient voltage ripple occurs at the output of the combination part that named single event transient(SET). These SETs during transmission and spread, Can be masked by logical and electrical structure or latch sampling period and Prevent to be further transmission and spread. These three factors are somewhat reduce probability of soft error. But still a large number of transient wave with a sufficient period of time to be reach the storage elements and Leading to the occurrence of breakdowns and software errors. Particle collisions can directly affect the internal nodes of the memory circuits and leading to the change of status of circuit. This phenomenon is called single event upset (SEU) [4]. Particle collisions with controlling circuits, such as clock pulse circuits could enable control signals faulty and thus save the unwanted data [5].

The effect of SETs on the reliability of digital systems under radiation should be considered by designers who exploit deep submicron technologies [6], [11]. Available, accurate methods for calculating the impact of SET on IC designs are thus needed [6]. However, there are few related works for calculating the reliability of SETs in logic circuits.

Baojun Liu et al. proposed an algorithm for evaluating the reliability of single event transients on digital ICs. The algorithm is based on defined multi-state systems, and signal probability. The impacts of masking (logic and electrical) and crosstalk effects between interconnects on reliability are considered when evaluating the reliability of SET in logic circuits [7].

This paper gives the importance of digital system reliability, calculate and compare the reliability of different encoder structures that are used in the flash analog to digital converters, in terms of single event transient. The rest of the paper is organized as follows. In Section II, conventional method for reliability evaluation is presented. In Section III, reliability evaluation for SETs on various encoder structures of flash ADCs are presented. Section IV presents analysis and simulation results. Section V concludes this paper.

2. The conventional method used to calculate the reliability of digital circuits

A. Reliability Evaluation Based on Universal Generating Function and Multi-State Model of SETs

In this paper, the proposed method in [7] is used to reliability analysis of various encoders. First, the multistate of SETs pulses were defined, as shown in Fig. 2 (table 1).

So any signal line may spread a multi-state signal, illustrated by the set S= {0, a, b,$\bar{a}, \bar{b}$, 1}. When a SET occurs at node $n_i$in a digital circuit, extracted are all on-path signals and gates from $n_i$to every reachable primary out put.This result can be achieved using the forward Depth-First-Search (DFS) algorithm [8].

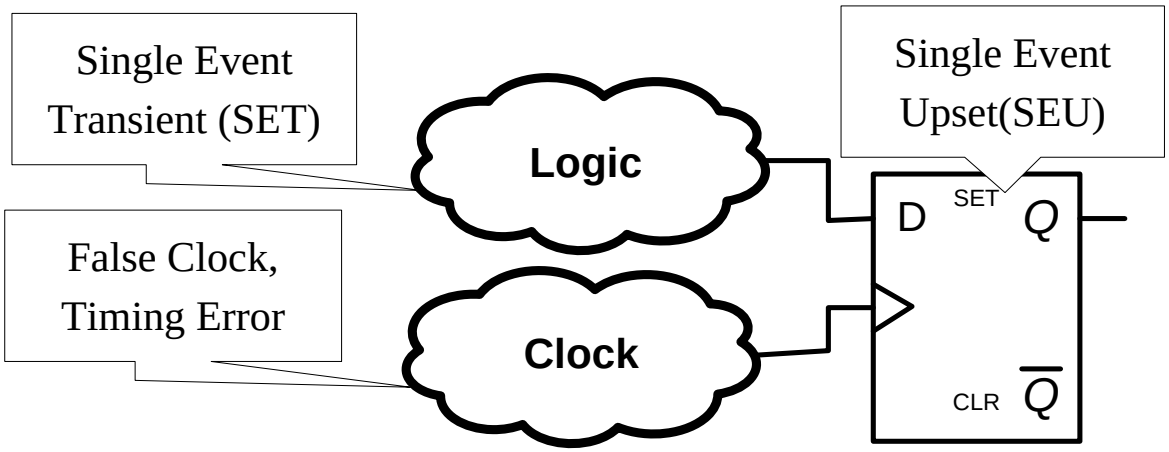

Fig. 1. The effect of particle collisions in different parts of the circuit

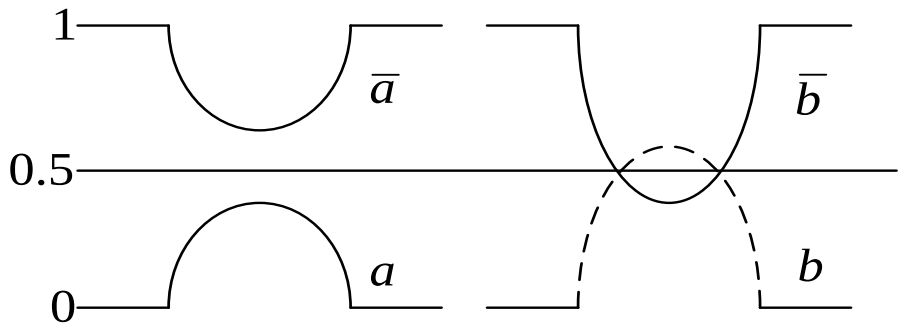

Fig. 2. Status of SETs signal

Table1-Definition of SETs signal

Signal Status	Quantity
0	No SET is propagated to this signal line, and it has an error-free value of 0.
1	No SET is propagated to this signal line, and it has an error-free value of 1.
a	Signal propagate a SET from logic 0, and the maximum value of it is less than 0.5 (V_{DD}*/2).
$\bar{a}$	Signal propagate a SET from logic 1, and the minimum value of it is more than 0.5.
b	Signal propagate a SET from logic 0, and the maximum value of it is more than 0.5.
$\bar{b}$	Signal propagate a SET from logic 1, and the minimum value of it is less than 0.5.

Table 2- Mapping function of main gates.

Gate	Defined Function f
AND	$minf(1,x^*)=x\,;minf(0,x)=0\,;minf(a,y^*)$ $=a\,;minf(\bar{b},y)$ $=y\,;minf(b,\bar{a})=a$
OR	$addf(1,x)=1\,;addf(0,x)=x\,;addf(\bar{a},y)$ $=\bar{a}\,;addf(a,b)$ $=b\,;\ addf(a,\bar{b})$ $=\bar{a}\,;addf(b,\bar{b})=\bar{a}$
NOT	$notf(1)=0\,;notf(0)=1\,;notf(a)$ $=\bar{a}\,;notf(\bar{a})=a\,;\ notf(b)$ $=\bar{b}\,;\ notf(\bar{b})=b$
XOR	$xorf(1,\bar{a})=a\,;xorf(1,a)=\bar{a};xorf(0,a)$ $=a\,;\ addf(0,\bar{a})$ $=\bar{a}\,;xorf(\bar{b},1)=b\,;\ldots$

$*\ x\in S=\{0,a,b,\bar{a},\bar{b},1\}\,,y\in S-\{0,1\}.$

The reliability of SET in the primary output can be expressed as [9].

$$R(\theta)=E[\pi(W,\theta)]=\sum_{i=1}^{6}q_i\pi(w_i,\theta) \quad (1)$$

Where $q_i$is the probability mass function of primary outputs and $\pi(W,\theta)$ is an acceptability function which represents the desired relation between the primary output W and some limit values named acceptable range (π(W,θ)=1 if primary output is acceptable and π(W,θ)=0 otherwise). The reliability for SETs from noden_i on digital circuits with k outputs are calculated as.

$$R_{all}=\prod_{j=1}^{k}R_j(\theta) \quad (2)$$

The universal generating function (u-function), representing the probability mass function of signals, can be defined as [9].

$$u_j(z)=q_i\ =\sum_{h=1}^{6}p_{jh}z^{s_h} \quad (3)$$

To obtain the u-function representing the probability mass function of the gate, which consists of signal inputs of $V_1,V_2,\ldots,V_n$, the following defined operator (9) is used [7].

$$\begin{aligned}U(z)&=\underset{f}{\otimes}\big(u_1(z),u_2(z),\ldots,u_n(z)\big)\\&=\underset{f}{\otimes}\left(\sum_{h=1}^{6}p_{1h}z^{s_h},\sum_{h=1}^{6}p_{2h}z^{s_h},\ldots,\sum_{h=1}^{6}p_{nh}z^{s_h}\right)\\&=\sum_{h=1}^{6}\sum_{h=1}^{6}\ldots\sum_{h=1}^{6}\left(\prod_{i=1}^{n}p_{ih}z^{f(s_h,s_h,\ldots,s_h)}\right)\end{aligned} \quad (4)$$

From (9), we can find that the key of the u-function calculation is the mapping function. By considering logic masking, we define the mapping function of main gates (including AND, OR, and NOT) under SETs, as shown in Table 2[7].

B. Reliability evaluation consideringeffects of masking and crosstalk

It was clear that, gate position and size

affection error propagation and logic masking [10]. When a noise disturbance inputs into a gate, the gate can filter and attenuate the disturbance [11]. This phenomenon is called electrical masking. This effect will attenuate the amplitude of the SET noise. Assume that the electrical masking ratio is$1-P_E$. If the original u-function of a gate without considering electrical masking is expressed as [7]

$$u(z)=p_0z^0+p_az^a+p_bz^b+p_{\bar{a}}z^{\bar{a}}+p_{\bar{b}}z^{\bar{b}}+p_1z^1 \quad (5)$$

Where

$$p_0+p_a+p_b+p_{\bar{a}}+p_{\bar{b}}+p_1=1 \quad (6)$$

Then the u-function of the gate considering electrical masking effects can be achieved by:

$$u(z)=(p_0+p_aP_E)z^0+(p_a(1-P_E)+p_bP_E)z^a+p_b(1-P_E)z^b+p_{\bar{b}}(1-P_E)z^{\bar{b}}+(p_{\bar{a}}(1-P_E)+p_{\bar{b}}P_E)z^{\bar{a}}+(p_1+p_{\bar{a}}P_E)z^1 \quad (7)$$

With advances in technology scaling, coupling effects among interconnects, called crosstalk effects, will significantly affect the SETs [9]. Here we only consider the crosstalk effects between interconnects of the inputs of the same gate. Assume that the crosstalk probability isp_c.For a gate with two inputs, the u-function for the signals of the input can be written as [7]

$$\begin{aligned}u_1(z)&=p_{11}z^0+p_{12}z^a+p_{13}z^b+p_{14}z^{\bar{b}}+p_{15}z^{\bar{a}}+p_{16}z^1u_2(z)\\&=p_{21}z^0+p_{22}z^a+p_{23}z^b+p_{24}z^{\bar{b}}+p_{25}z^{\bar{a}}+p_{26}z^1\end{aligned} \quad (8)$$

Where

$$\sum_{h=1}^{6}p_{mh}=1\,,(m=1,2) \quad (9)$$

For $u_1(z)$, because of the crosstalk effects, the probability mass function of it is modified by (16)

$$\begin{aligned}&\acute{u_1}(z)=p'_{11}z^0+p'_{12}z^a+p'_{13}z^b+p'_{14}z^{\bar{b}}+p'_{15}z^{\bar{a}}+p'_{16}z^1\\&p_{t1}=p_{22}+p_{23}+p_{24}+p_{25}\\&p'_{11}=p_{11}(1-p_cp_{t1})+p_{12}p_{25}p_c+p_{13}p_{24}p_c\\&p'_{12}=p_{12}(1-p_cp_{t1})+p_{11}p_{t1}p_c+p_{12}p_{24}p_c\\&p'_{13}=p_{13}(1-p_cp_{24})+p_{12}p_{23}p_c+p_{12}p_{22}p_c\\&p'_{14}=p_{14}(1-p_cp_{23})+p_{15}p_{24}p_c\\&p'_{15}=p_{11}(1-p_cp_{22}-p_cp_{24})+p_{16}p_{t1}p_c\\&p'_{16}=p_{16}(1-p_cp_{t1})+p_{14}p_{23}p_c+p_{15}p_{22}p_c\end{aligned} \quad (10)$$

Similarly, we can obtain the modified$u_2(z)$considering crosstalk effects.

Table 4. Truth Table of 3-bit Gray Code Encoder

B_1	B_2	B_3	G_1	G_2	G_3	T_1	T_2	T_3	T_4	T_5	T_6	T_7		
0	0	0	0	0	0	0	0	0	0	0	0	0	S_0	
1	0	0	1	0	0	1	0	0	0	0	0	0	S_1	
0	1	0	1	1	0	1	1	0	0	0	0	0	S_2	
1	1	0	0	1	0	1	1	1	0	0	0	0	S_3	
0	0	1	0	1	1	1	1	1	1	0	0	0	S_4	
1	0	1	1	1	1	1	1	1	1	1	0	0	S_5	
0	1	1	1	0	1	1	1	1	1	1	1	0	S_6	
1	1	1	0	0	1	1	1	1	1	1	1	1	S_7	

3. Reliability Evaluation for SETs on Various Encoder Structures of Flash ADCs

Fig. 3 shows the general structure of a 3-bit flash ADC. Which consists of a number of comparators which each compares the input signal with a reference signal. The output of comparators are connected to the inputs of an encoder that generates a binary output. In this section three different encoder structures that used in the flash ADCs are introduced and the reliability evolution of these encoders, in terms of single event transient is proposed. For reliability evolution of these circuits we use the algorithm presented in [7].

A. Gray Code Encoder

Figure 4. Shows structure of gray code encoder for 2 and 3-bit flash ADC. Assume that an SET occurs at intermediate node (G1). Without considering effects of error attenuation and crosstalk, we first constitute the truth table of the 2-bit encoder circuit, shown in Table 3. We next define an on-path gate as a gate on a path from the SET-occurred node to a reachable output. By using the DFS algorithm [8], extract all on-path gates from SET-occurred node (G1) to every reachable primary output.

The probability of status "a" is 0.3, and the probability of "b" is 0.7for the original status "0"; or else the probability of "$\bar{a}$" is 0.3, and the probability of "$\bar{b}$" is 0.7 for the status "1". For any combination S, determine the u-function of the signal of the primary output, and the u-function of the signal probability of other off-path SET signals, as follow. For combination S_0 and S_3 we have

$$u_{T_2}(z) = u_{G_2}(z) = u_{B_2}(z) = p_0 z^0 + p_1 z^1 = 0.5z^0 + 0.5z^1$$
$$u_{G_1}(z) = p_a z^a + p_b z^b = 0.3z^a + 0.7z^b$$
$$u_{B_1}(z) = u_{G_1}(z) \underset{xorf}{\otimes} u_{G_2}(z) = 0.15z^a + 0.35z^b + 0.15z^{\bar{a}} + 0.35z^{\bar{b}}$$

For combination S_1 and S_2

$$u_{T_2}(z) = u_{G_2}(z) = u_{B_2}(z) = 0.5z^0 + 0.5z^1$$
$$u_{G_1}(z) = 0.3z^{\bar{a}} + 0.7z^{\bar{b}}$$
$$u_{B_1}(z) = u_{G_1}(z) \underset{xorf}{\otimes} u_{G_2}(z) = 0.15z^{\bar{a}} + 0.35z^{\bar{b}} + 0.15z^a + 0.35z^b$$

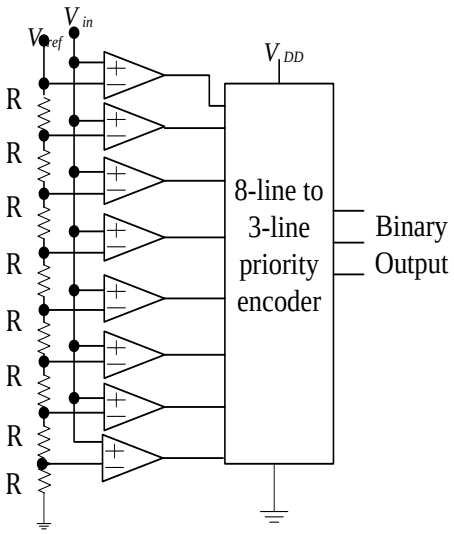

Fig. 3. General structure of a 3-bit flash ADC.

Table 3 -Truth Table of 2-bit Gray Code Encoder

B_1	B_2	G_1	G_2	T_1	T_2	T_3	
0	0	0	0	0	0	0	S_0
1	0	1	0	1	0	0	S_1
0	1	1	1	1	1	0	S_2
1	1	0	1	1	1	1	S_3

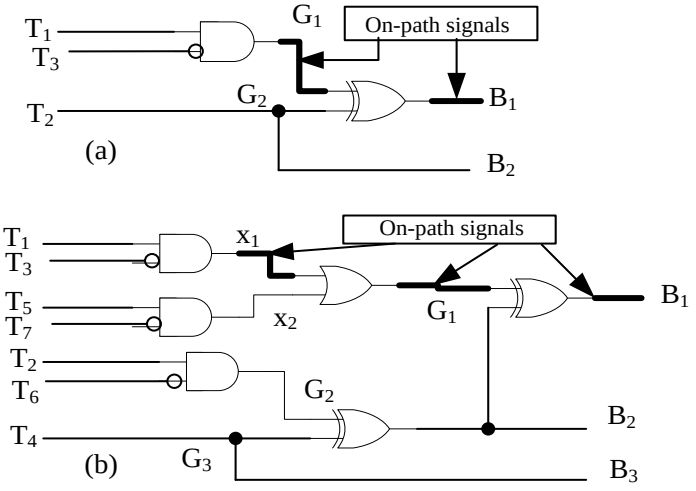

Fig. 4. Structure of gray code encoder for 2 (a) and 3-bit (b) flash ADC.

Table 4 . Truth table of 3-bit gray code encoder

B_1	B_2	B_3	G_1	G_2	G_3	T_1	T_2	T_3	T_4	T_5	T_6	T_7	
0	0	0	0	0	0	0	0	0	0	0	0	0	S_0
1	0	0	1	0	0	1	0	0	0	0	0	0	S_1
0	1	0	1	1	0	1	1	0	0	0	0	0	S_2
1	1	0	0	1	0	1	1	1	0	0	0	0	S_3
0	0	1	0	1	1	1	1	1	1	0	0	0	S_4
1	0	1	1	1	1	1	1	1	1	1	0	0	S_5
0	1	1	1	0	1	1	1	1	1	1	1	0	S_6
1	1	1	0	0	1	1	1	1	1	1	1	1	S_7

The acceptability function can be defined as

$$\pi(w_i,\theta)=\begin{cases}1(w_i>0.5)\\0(w_i<0.5),\end{cases}\quad for\ F=1$$
$$\pi(w_i,\theta)=\begin{cases}0(w_i>0.5)\\1(w_i<0.5),\end{cases}\quad for\ F=0 \tag{11}$$

Assume that the probability Qs of the combination of inputs is$\frac{1}{2^2}$. The reliability for SET can be achieved as

$$\begin{aligned}R=\sum_{s=0}^{2^m-1}Q_sR_s=\frac{1}{2^2}\sum_{S_0}^{S_3}\sum_{i=1}^{6}u_{B_1}(z)\,\pi(w_i,\theta)=\frac{1}{4}[u_{B_1,S_0}(z)\pi(w_i<0.5,\theta)+u_{B_1,S_1}(z)\pi(w_i\\>0.5,\theta)+u_{B_1,S_2}(z)\pi(w_i<0.5,\theta)+u_{B_1,S_3}(z)\pi(w_i>0.5,\theta)]\\=\frac{1}{4}[0.15Z^a+0.15Z^{\bar a}+0.15Z^a+0.15Z^{\bar a}]=\frac{1}{4}[0.3Z^a+0.3Z^{\bar a}]=0.15\end{aligned} \tag{12}$$

For reliability evaluation on SET for 3-bit gray code encoder, assuming that an SET occurs at intermediate node (x_1).The truth table of the 3-bit gray code encoder circuit, shown in Table 4.

For any combination S, we calculate the u-function of primary output, and signal probability of off-path SET signals. For combination S_0.

$$\begin{aligned}&u_{x_2}(z)=u_{G_2}(z)=0.75z^0+0.25z^1\\&u_{x_1}(z)=0.3z^a+0.7z^b\\&u_{G_1}(z)=u_{x_1}(z)\underset{addf}{\otimes}u_{x_2}(z)=0.25z^1+0.225z^a+0.525z^b\\&u_{G_3}(z)=0.5z^0+0.5z^1\\&u_{B_2}(z)=u_{G_3}(z)\underset{xorf}{\otimes}u_{G_2}(z)=0.5z^0+0.5z^1\\&u_{B_1}(z)=u_{G_1}(z)\underset{xorf}{\otimes}u_{B_2}(z)\\&\qquad=0.125z^1+0.125z^0+0.1125z^a+0.2625z^b+0.1125z^{\bar a}\\&\qquad+0.2625z^{\bar b}\end{aligned} \tag{13}$$

According to truth table 4 equation 18 is also true for combinations S_3, S_4, S_5, $S_6$and S7. For combination S_1 and S_2 we have.

$$
\begin{aligned}
&u_{x_2}(z) = u_{G_2}(z) = 0.75z^0 + 0.25z^1 \\
&u_{x_1}(z) = 0.3z^{\bar{a}} + 0.7z^{\bar{b}} \\
&u_{G_1}(z) = u_{x_1}(z) \underset{addf}{\otimes} u_{x_2}(z) = 0.25z^1 + 0.225z^{\bar{a}} + 0.525z^{\bar{b}} \\
&u_{G_3}(z) = 0.5z^0 + 0.5z^1 \\
&u_{B_2}(z) = u_{G_3}(z) \underset{xorf}{\otimes} u_{G_2}(z) = 0.5z^0 + 0.5z^1 \\
&u_{B_1}(z) = u_{G_1}(z) \underset{xorf}{\otimes} u_{B_2}(z) \\
&\qquad = 0.125z^0 + 0.125z^1 + 0.1125z^a + 0.1125z^{\bar{a}} + 0.2625z^b + 0.2625
\end{aligned}
\tag{14}
$$

Assume that the probability Qs of the combination of inputs is$\frac{1}{2^3}$. The reliability for SET can be achieved as

$$
\begin{aligned}
R = \sum_{s=0}^{2^m-1} Q_s R_s = \frac{1}{2^3} \sum_{S_0}^{S_7} \sum_{i=1}^{6} u_{B_1}(z)\, \pi(w_i, \theta) = \frac{1}{8} [&u_{B_1,S_0}(z)\pi(w_i < 0.5, \theta) + u_{B_1,S_1}(z)\pi(w_i \\
&> 0.5, \theta) + u_{B_1,S_2}(z)\pi(w_i < 0.5, \theta) + u_{B_1,S_3}(z)\pi(w_i > 0.5, \theta) \\
&+ + u_{B_1,S_4}(z)\pi(w_i < 0.5, \theta) + u_{B_1,S_5}(z)\pi(w_i > 0.5, \theta) \\
&+ u_{B_1,S_6}(z)\pi(w_i < 0.5, \theta) + u_{B_1,S_5}(z)\pi(w_i > 0.5, \theta)] \\
&= \frac{1}{8} [(0.125Z^0 + 0.1125Z^a) + \cdots](15) = 0.2375
\end{aligned}
$$

B. *XOR Based Encoder*

Figure 5. Shows structure of XOR based encoder for 2 and 3-bit flash ADC.The truth table of the 2-bit XOR encoder circuit, shown in Table 5. With all previous assumptions, we calculate the reliability for SET for this type of encoder. The u-function for primary output (B_1) for combinations S_0, S_2 and S_3 is calculated as follows.

Table 5- Truth Table of 2-bit XOR BASED Encoder

	T_3	T_2	T_1	G_1	B_2	B_1
S_0	0	0	0	0	0	0
S_1	0	0	1	1	0	1
S_2	0	1	1	0	1	0
S_3	1	1	1	0	1	1

$$
\begin{aligned}
&u_{T_2}(z) = u_{T_3}(z) = u_{B_2}(z) = 0.5z^0 + 0.5z^1 \\
&u_{G_1}(z) = 0.3z^a + 0.7z^b \\
&u_{B_{1,S_0,S_2,S_3}}(z) = u_{G_1}(z) \underset{xorf}{\otimes} u_{T_3}(z) = 0.15z^a + 0.35z^b + 0.15z^{\bar{a}} + 0.35z^{\bar{b}}
\end{aligned}
\tag{15}
$$

And for combination S_1 we have

$$u_{T_2}(z) = u_{T_3}(z) = u_{B_2}(z) = 0.5z^0 + 0.5z^1$$

$$u_{G_1}(z) = 0.3z^{\bar{a}} + 0.7z^{\bar{b}}$$

$$u_{B_{1,S_0,S_2,S_3}}(z) = u_{G_1}(z) \underset{xorf}{\otimes} u_{T_3}(z) = 0.15z^{\bar{a}} + 0.35z^{\bar{b}} + 0.15z^{a} + 0.35z^{b}$$

The overall reliability is calculated as follows.

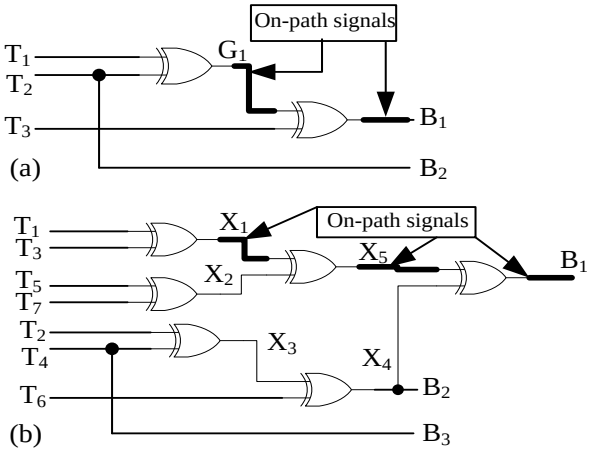

Fig. 5. Structure of XOR based encoder for 2 (a) and 3-bit (b) flash ADC.

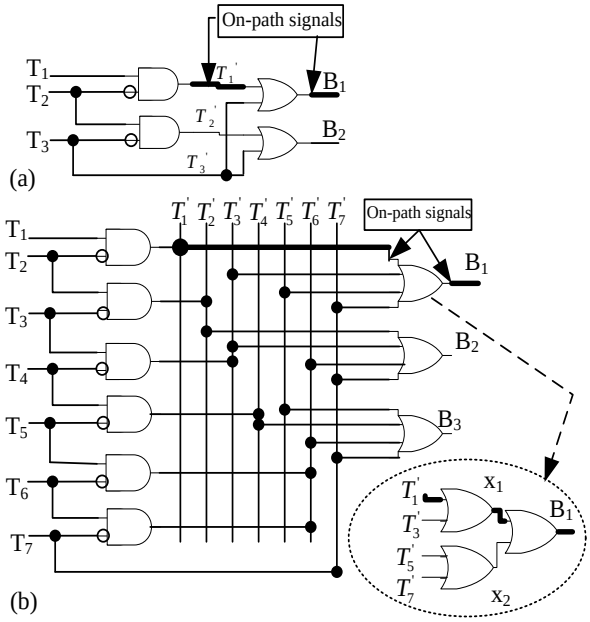

Fig. 6. Structure of encoder ROM for 2 (a) and 3-bit (b) flash ADC.

$$R = \sum_{s=0}^{2^m-1} Q_s R_s = \frac{1}{2^2} \sum_{S_0}^{S_3} \sum_{i=1}^{6} u_{B_1}(z)\,\pi(w_i,\theta) = \frac{1}{4}[u_{B_1,S_0}(z)\pi(w_i < 0.5,\theta) + u_{B_1,S_1}(z)\pi(w_i > 0.5,\theta) + u_{B_1,S_2}(z)\pi(w_i < 0.5,\theta) + u_{B_1,S_3}(z)\pi(w_i > 0.5,\theta)] = \frac{1}{4}[0.15Z^a + 0.15Z^{\bar{a}} + 0.15Z^a + 0.15Z^{\bar{a}}] = 0.15 \quad (16)$$

For reliability evaluation on SET for 3-bit XOR encoder, assuming that an SET occurs at intermediate node (x_1). The truth table of the 3-bit XOR encoder circuit, shown in Table 6. For any combination S, we calculate the u-function of primary output, and signal probability of off-path SET signals. For combination S_0.

Table 6- Truth Table of 3-bit XOR BASED Encoder

	T_7	T_6	T_5	T_4	T_3	T_2	T_1	B_3	B_2	B_1
S_0	0	0	0	0	0	0	0	0	0	0
S_1	0	0	0	0	0	0	1	0	0	1
S_2	0	0	0	0	0	1	1	0	1	0
S_3	0	0	0	0	1	1	1	0	1	1
S_4	0	0	0	1	1	1	1	1	0	0
S_5	0	0	1	1	1	1	1	1	0	1
S_6	0	1	1	1	1	1	1	1	1	0
S_7	1	1	1	1	1	1	1	1	1	1

Table 7 Truth Table of 2-bit Encoder ROM

	T_3	T_2	T_1	T_3'	T_2'	T_1'	B_2	B_1
S_0	0	0	0	0	0	0	0	0
S_1	0	0	1	0	0	1	0	1
S_2	0	1	1	0	1	0	1	0
S_3	1	1	1	1	0	0	1	1

$$u_{x_2}(z) = u_{x_3}(z) = u_{x_4}(z) = 0.5z^0 + 0.5z^1$$
$$u_{x_1}(z) = 0.3z^a + 0.7z^b$$
$$u_{x_5}(z) = u_{x_1}(z) \underset{xorf}{\otimes} u_{x_2}(z) = 0.15z^a + 0.35z^b + 0.15z^{\bar{a}} + 0.35z^{\bar{b}} \quad (17)$$
$$u_{B_1}(z) = u_{x_4}(z) \underset{xorf}{\otimes} u_{x_5}(z) = 0.15z^a + 0.35z^b + 0.15z^{\bar{a}} + 0.35z^{\bar{b}}$$

According to truth table 6 equation 22 is also true for combinations S_3, S_4, S_5, $S_6$and S7.For combination S_1 and S_2 we have

$$
\begin{aligned}
&u_{x_2}(z) = u_{x_3}(z) = u_{x_4}(z) = 0.5z^0 + 0.5z^1 \\
&u_{x_1}(z) = 0.3z^{\bar{a}} + 0.7z^{\bar{b}} \\
&u_{x_5}(z) = u_{x_1}(z) \underset{xorf}{\otimes} u_{x_2}(z) = 0.15z^{\bar{a}} + 0.35z^{\bar{b}} + 0.15z^{a} + 0.35z^{b} \\
&u_{B_1}(z) = u_{x_4}(z) \underset{xorf}{\otimes} u_{x_5}(z) = 0.15z^{\bar{a}} + 0.35z^{\bar{b}} + 0.15z^{a} + 0.35z^{b}
\end{aligned} \tag{18}
$$

Assume that the probability Qs of the combination of inputs is$\frac{1}{2^3}$. The reliability for SET can be achieved as

$$
\begin{aligned}
R = \sum_{s=0}^{2^m-1} Q_s R_s = \frac{1}{2^3} \sum_{S_0}^{S_7} \sum_{i=1}^{6} u_{B_1}(z)\, \pi(w_i, \theta) = \frac{1}{8} [u_{B_1,S_0}(z)\pi(w_i < 0.5, \theta) + u_{B_1,S_1}(z)\pi(w_i \\
> 0.5, \theta) + u_{B_1,S_2}(z)\pi(w_i < 0.5, \theta) + u_{B_1,S_3}(z)\pi(w_i > 0.5, \theta) \\
+ + u_{B_1,S_4}(z)\pi(w_i < 0.5, \theta) + u_{B_1,S_5}(z)\pi(w_i > 0.5, \theta) \\
+ u_{B_1,S_6}(z)\pi(w_i < 0.5, \theta) + u_{B_1,S_5}(z)\pi(w_i > 0.5, \theta)] \\
= \frac{1}{8} [(0.15Z^a) + (0.15Z^{\bar{a}}) + \cdots] = 0.15
\end{aligned} \tag{19}
$$

C. *Encoder ROM*

Figure 6. Shows structure of encoder ROM circuit for 2 and 3-bit flash ADC. The truth table of the 2-bit encoder ROM circuit, shown in Table 7.

Assume that an SET occurs at intermediate node (T'_1). With all previous assumptions, we calculate the reliability for SET for this type of encoder. The u-function for primary output (B_1) for S_0, S_2 and S_3 combinations is calculated as follows.

$$
\begin{aligned}
&u_{T_1}(z) = u_{T_2}(z) = u_{T_3}(z) = u_{T'_3}(z) = 0.5z^0 + 0.5z^1 \\
&u_{f_1}(z) = 0.3z^{a} + 0.7z^{b} \\
&u_{B_{1,S_0,S_2,S_3}}(z) = u_{f_1}(z) \underset{addf}{\otimes} u_{T_3}(z) = 0.15z^{a} + 0.35z^{b} + 0.15z^{1} + 0.35z^{1}
\end{aligned}
$$

For combination S_1 we have

Table 8 Truth Table of 3-bit Encoder ROM

	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T'_7	T'_6	T'_5	T'_4	T'_3	T'_2	T'_1	B_3	B_2	B_1
S_0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S_1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1
S_2	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0
S_3	0	0	0	0	1	1	1	0	0	0	0	1	0	0	0	1	1
S_4	0	0	0	1	1	1	1	0	0	0	1	0	0	0	1	0	0
S_5	0	0	1	1	1	1	1	0	0	1	0	0	0	0	1	0	1
S_6	0	1	1	1	1	1	1	0	1	0	0	0	0	0	1	1	0
S_7	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1

Table 9. Reliability of various Encoder Circuits

Encoder Structure	Reliability (no effect)	Reliability (only masking effect)	Reliability (masking and crosstalk effects)
2-Bit Gray Code Encoder	0.15	0.2265	0.2277
2-Bit XOR Encoder	0.15	0.2257	0.2272
2-bit Encoder ROM	0.3625	0.4748	0.4821
3-Bit Gray Code Encoder	0.2375	0.3372	0.3422
3-Bit XOR Encoder	0.15	0.2280	0.2304
3-bit Encoder ROM	0.3677	0.4798	0.4883

$$u_{T_1}(z) = u_{T_2}(z) = u_{T_3}(z) = u_{T'_3}(z) = 0.5z^0 + 0.5z^1$$
$$u_{T'_1}(z) = 0.3z^{\bar{a}} + 0.7z^{\bar{b}}$$
$$u_{B_{1,S_1}}(z) = u_{T'_1}(z) \underset{addf}{\otimes} u_{T_3}(z) = 0.15z^{\bar{a}} + 0.35z^{\bar{b}} + 0.15z^1 + 0.35z^1$$

The overall reliability is calculated as follows

$$R = \frac{1}{4}[0.15Z^a + 0.15Z^{\bar{a}} + 0.15Z^1 + 0.35z^1 + 0.15Z^a + 0.15Z^1 + 0.35z^1] \quad (20)$$
$$= 0.3625$$

For reliability evaluation on SET for 3-bit XOR encoder, assuming that an SET occurs at intermediate node (T'_1). The truth table of the 3-bit XOR encoder circuit, shown in

Table 8. For any combination S, we calculate the u-function of primary output, and signal probability of off-path SET signals. For combination S_0we have

$$
\begin{aligned}
&u_{\acute{T}_3}(z) = u_{\acute{T}_5}(z) = u_{\acute{T}_7}(z) = 0.75z^0 + 0.25z^1 \\
&u_{\acute{T}_1}(z) = 0.3z^a + 0.7z^b \\
&u_{x_1}(z) = u_{\acute{T}_1}(z) \underset{addf}{\otimes} u_{\acute{T}_3}(z) = 0.225z^a + 0.525z^b + 0.25z^1 \\
&u_{x_2}(z) = u_{\acute{T}_5}(z) \underset{addf}{\otimes} u_{\acute{T}_7}(z) = 0.5625z^0 + 0.4375z^1 \\
&u_{B_1}(z) = u_{x_1}(z) \underset{addf}{\otimes} u_{x_2}(z) = 0.1266z^a + 0.2953z^b + 0.5773z^1
\end{aligned}
\tag{21}
$$

According to truth table 8 equation 26 is also true for combinations S_2, S_3, S_4, S_5, S_6 and S_7. For combination S_1 we have

$$
\begin{aligned}
&u_{\acute{T}_3}(z) = u_{\acute{T}_5}(z) = u_{\acute{T}_7}(z) = 0.75z^0 + 0.25z^1 \\
&u_{\acute{T}_1}(z) = 0.3z^{\bar{a}} + 0.7z^{\bar{b}} \\
&u_{x_1}(z) = u_{\acute{T}_1}(z) \underset{addf}{\otimes} u_{\acute{T}_3}(z) = 0.225z^{\bar{a}} + 0.525z^{\bar{b}} + 0.25z^1 \\
&u_{x_2}(z) = u_{\acute{T}_5}(z) \underset{addf}{\otimes} u_{\acute{T}_7}(z) = 0.5625z^0 + 0.4375z^1 \\
&u_{B_1}(z) = u_{x_1}(z) \underset{addf}{\otimes} u_{x_2}(z) = 0.1266z^{\bar{a}} + 0.2953z^{\bar{b}} + 0.5773z^1
\end{aligned}
\tag{22}
$$

Assume that the probability Qs of the combination of inputs is $\frac{1}{2^3}$. The reliability for SET can be achieved as.

$$
\begin{aligned}
R = \sum_{s=0}^{2^m-1} Q_s R_s = \frac{1}{2^3} \sum_{S_0}^{S_7} \sum_{i=1}^{6} u_{B_1}(z)\, \pi(w_i, \theta) = \frac{1}{8}[(0.1266z^a) + (0.1266z^{\bar{a}} + \\
0.5773z^1) + (0.1266z^a) + (0.5773z^1) + (0.1266z^a) + (0.5773z^1) + (0.1266z^a) + \\
(0.5773z^1)] = 0.3677
\end{aligned}
\tag{23}
$$

4- SIMULATION AND ANALYSIS

Assume that probability of weak SET (a,$\bar{a}$) is 0.3, and the probability of strong SET (b,$\bar{b}$) is 0.7 at the SET-occur node, the reliabilities of SET in the various 2-bit and 3-bit encoder circuits are evaluated early without considering logic masking and crosstalk effect. Then, assuming an SET occur in the input of presented circuits and electrical masking ratio is 0.7; the crosstalk probability is 0.9; reliability is same again considering the effects of masking and crosstalk for 2 and 3-bit encoders are calculated in different structures. The results are shown in Table 9. From this table it can be resulted that the

reliability of Encoder Ram is approximately twice more than other structures. After considering the masking effects, reliability is improved strongly by an average 42.8%. Because of the masking effect alleviate the amplitude of the pulse disturbance. Also compared with the reliability without effect, crosstalk effect and error attenuation of the gates improves reliability on average about 44.5%.

5- CONCLUSION

With advances in fabrication technology and reducing the feature size, single event transients (SETs), is among the most important considerations in the design of digital circuits. Based on multistate model of single event transients and universal generating function, Reliability of three different 2 and 3-bit encoder structures that are used in flash ADCs, is calculated. The results shows that the reliability of Encoder Rom structure is higher than other structures. Also calculates the reliability for 2 and 3-bit encoders in the different structures with respect the logic masking and crosstalk effect indicates the reliability improving strongly. Therefor results of this paper can provide important suggestions for integrated circuits designers and researchers to use structures with high reliability.

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