Design of Current Starved Voltage Controlled Oscillator with Phase Locked Loop to Estimate the Process Corner Analysis

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ABSTRACT:
This paper consists of a performance comparison of Current Starved Voltage Controlled Oscillator (CSVCO) for Phase Locked Loop (PLL). The design of Current Starved VCO is implemented using sleepy stack low power leakage technique. This has been implemented in 45nm CMOS Technology with a supply voltage of 0.45V in Cadence Software. The parameters such as average power, oscillation frequency, and delay are calculated in different process corners showing the performance of improvement results of cadence simulation. After comparison of the various parameters of PLL implemented with Sleep Stack CSVCO and Basic CSVCO, the sleepy stack approach is particularly useful in low power applications, The recommended PLL has a much smaller chip than previous designs, much lower power consumption and significantly higher efficiency. The proposed design of the PLL with Sleep Stack Technique makes the circuit efficiently to reduce sub-threshold leakage current, and achieves Frequency of 2.759 GHz, Power 2.559µw, phase noise -63.8(dBc/Hz) and Delay(µs) 0.0006544, respectively.

KEYWORDS: VCO, PLL, Gain, Gale-or, Lector, Control Voltage, Current starved VCO, Oscillation Frequency, Sleepy Stack, Tuning Range.

1. INTRODUCTION

The Phase Locked Loop (PLL) is a control system used to generate the phase of output signal which is related to the phase of the input signal. The major blocks present in the PLL are Voltage controlled Oscillator and phase detector in a feedback loop. This paper depicts one of the major blocks called VCO. The main functionality of the VCOs is in the communication systems. Among the multiple types of VCOs, the ring oscillators and LC oscillators plays a major role in terms of high frequency, less noise, wide tuning range [1], and the area occupancy. The LC VCO which consists of an induct-or and capacitor occupies more area. The ring oscillators consist of the delay cells which have the same functionality similar to the buffer and these cells would occupy more area. In a ring oscillator, the last delay cell output is connected to the first delay cells input [2], which is called feedback. The delay cells can be either single ended or differential accordingly [4]. The increase in the number of delay cells give rise to consumption of area [6]. Because of the differences in the driving capability, the characteristics of the VCO become nonlinear which can be avoided by adding feedback circuit. By adding this feedback circuit, it further leads to the increase in cost of the circuit [7]. The current starved VCO technique was designed in order to overcome the disadvantages caused by the previous VCO's [7].

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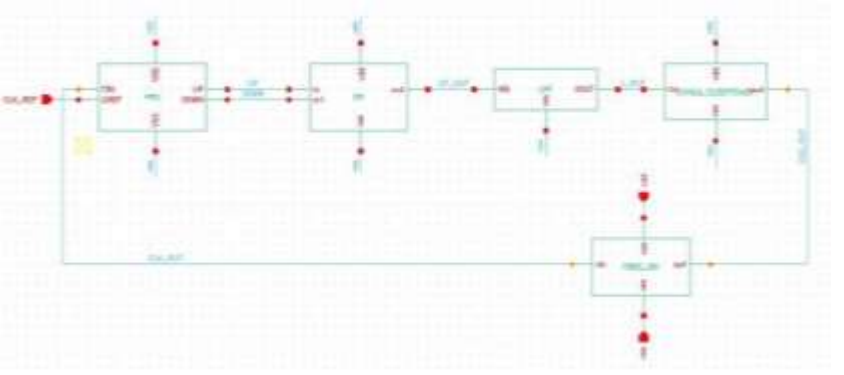


Fig. 1. Schematic diagram for PLL with Sleep Stack Current Starved VCO.

This paper is organized as follows. Section2 explains basic Current Starved VCO. Section 3 describes different leakage power reduction techniques in CMOS circuits. Section 4 defines simulation results and design comparisons. Finally, section 5 concludes this paper.

2. CURRENT STARVED RING VCO WITH SLEEP STACK & KEEPER TECHNIQUE

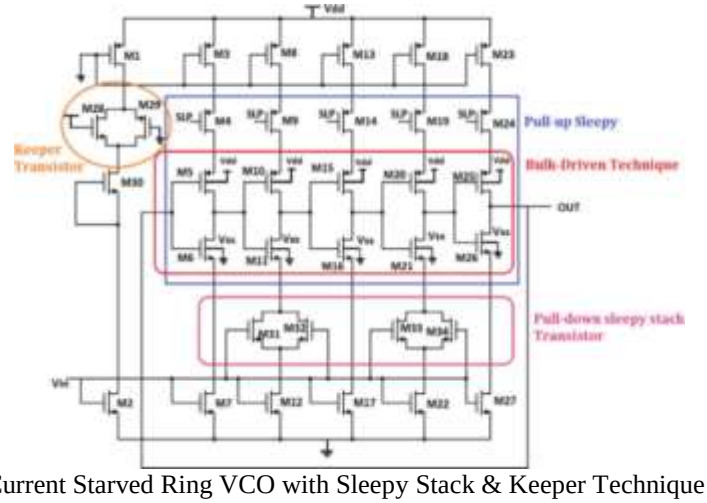


Fig. 2. Current Starved Ring VCO with Sleepy Stack & Keeper Technique Circuit.

The sleepy stack approach is particularly useful in low-power applications or when power efficiency is a critical design consideration. It helps to reduce power consumption without sacrificing the speed or performance of the circuit. The purpose of the alternative arrangement in the proposed circuit is to reduce the number of transistors and the area utilization. The alternative arrangement of the proposed design itself makes the circuit works efficiently to reduce sub-threshold leakage current, which in turn reduces power consumption. Therefore, not all the delay cells in the proposed design need to be connected with the sleepy stack approach.

3.CURRENT STARVED VCO PLL ARCHITECTURE WITH SLEEP STACK TECHNIQUE

Among the different types of VCO's, ring oscillator is the efficient in terms of frequency and driving capabilities. The ring VCO has been designed with delay stage. When these delay stages increased, lead to the non-linearity of the circuit. This non- linearity can be overcome by increasing the number of delay cells which has increased the complexity of the circuit and also increasing the power consumption [8]. The output frequencies of a basic VCO are controlled by the control voltage whereas the current is controlled by the current starved VCO [9]-[10]. The circuit consists of delay cells along with the current mirror which is used to limit the current to all the delay cells. The current starved VCO alone has also increased the leakages and power consumption [1]. These leakages can be further reduced by applying the low leakage techniques to the delay cells and by varying the aspect ratio of transistors which reduces the threshold voltage of basic current starved VCO [11].

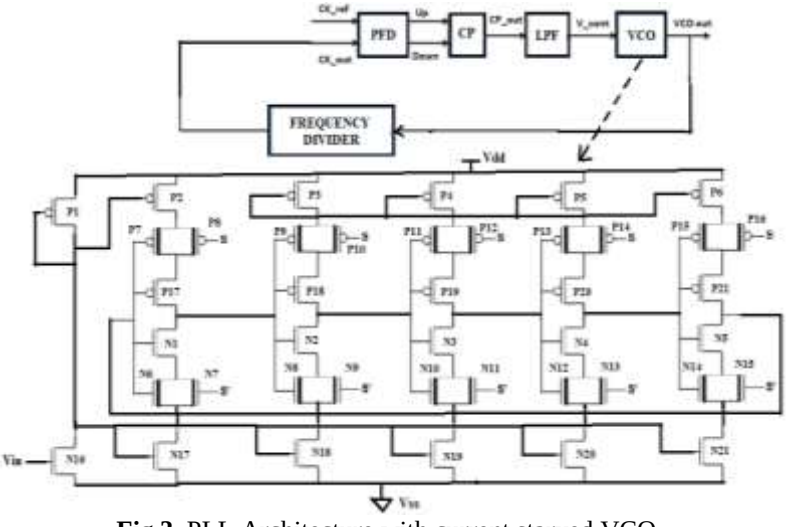


Fig.3. PLL Architecture with current starved VCO.

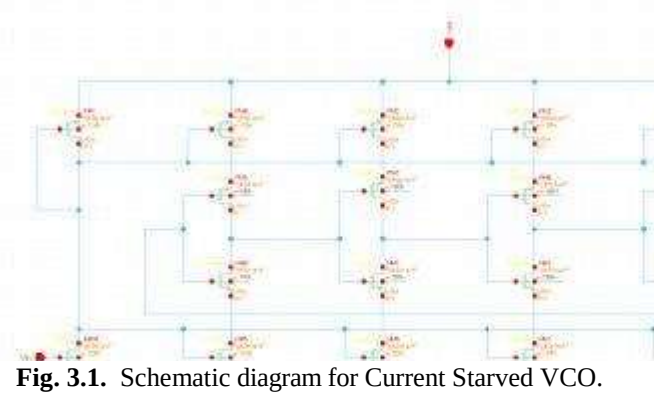


Fig. 3.1. Schematic diagram for Current Starved VCO.

In order to avoid this power consumption, a VCO named current starved was designed. The output frequencies of a basic VCO are controlled by the control voltage whereas the current is controlled by the current starved VCO [9]-[10]. The circuit consists of delay cells along with the current mirror which is used to limit the current to all the delay cells. The current starved VCO alone together has also increased the leakages and power consumption [1]. These leakages can be further reduced by applying the low leakage techniques to the delay cells and by varying the aspect ratio of transistors which reduces the threshold voltage [11].

4. LEAKAGE REDUCTION TECHNIQUES IMPLEMENTED IN VCO

The basic CSVCO, Current Starved Voltage Controlled Oscillator, is operated with the input voltage namely control voltage (Vctrl). As the Vctrl decreases, the current that is to be mirrored from the transistor M1 reduces when it is passed through the different PMOS in the delay stages. Because of the active mode of transistors in the CSVCO, the leakage power has been increased [1]. In this paper, the current starved VCO has been implemented with different low power leakagetechniques like Gale-or, Lector, Sleepy Keeper, Sleep Stack, and Sleepy Stack to observe the better performance of the circuit [12]. Performance analysis can be observed in terms of different parameters like frequency, delay, and average power is calculated in different process corners showing the improved performance Phase Locked Loop, For different applications

.4.1. Current Starved VCO with Sleep Stack Technique

The CSVCO circuit is implemented with Stack technique as shown in Figure 6, in which both the stack and sleep techniques are implemented above and below the pull -up and pull-down network, respectively. In normal mode, the sleep transistor would go to sleep mode, then the stack transistors reduce the leakages [24]-[26]. In case of the active mode, the sleep transistor becomesON and stack transistors are OFF, reducing the leakages in CSVCO circuit.

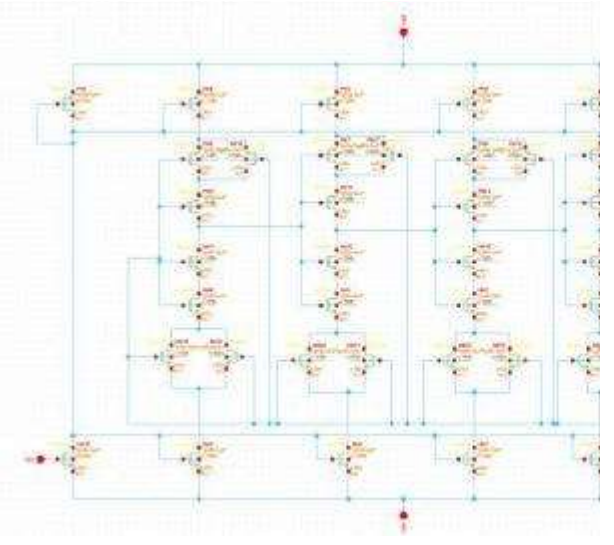


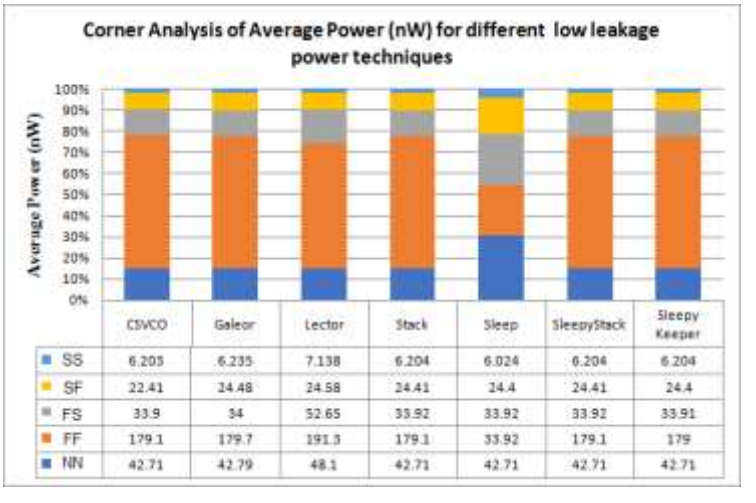
Fig. 4. CSVCO using Sleepy Stack Technique.

5. PROCESS CORNER ANALYSIS

Corner analysis provides a convenient way to measure circuit performance while simulating a circuit with sets of parameter values that represent the most extreme variations in a manufacturing process. All the proposed circuits with different low leakage techniques have their average power, oscillating frequency, and tuning range calculated in process corners like nominal, slow-fast, fast-slow, fast-fast and slow-slow conditions.

The mobility and the threshold voltage which in turn effect the device performance. If the threshold voltage is lowered, then there is more current and effectively the device is faster, however, if the threshold voltage is increased there is less current and the device could be slower. A lower supply voltage causes slower switching of the gates and results into an overall slower circuit, a high supply voltage drives faster switching of the larger gates which makes the circuits faster.

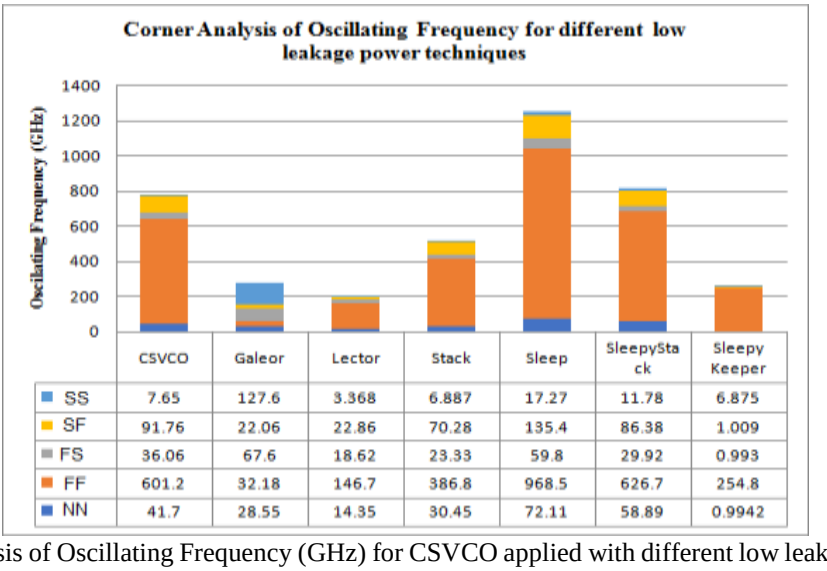
In addition to temperature and voltage analysis, the process corner analysis is carried out with the Cadence Virtuoso tool using the 45 NM generic process design kit (GPDK) technology file at 27℃ (fig.5).



	CSVCO	Galeor	Lector	Stack	Sleep	SleepyStack	Sleepy Keeper
SS	6.205	6.235	7.138	6.204	6.024	6.204	6.204
SF	22.41	24.48	24.58	24.41	24.4	24.41	24.4
FS	33.9	34	52.65	33.92	33.92	33.92	33.91
FF	179.1	179.7	191.3	179.1	33.92	179.1	179
NN	42.71	42.79	48.1	42.71	42.71	42.71	42.71

Fig. 5. Corner Analysis of P_{avg} for CSVCO applied with different low leakage techniques.

From the above plotted graph, it is observed that the average power in all the corners remained almost constant and in the Sleep Technique is always low in all the corners.

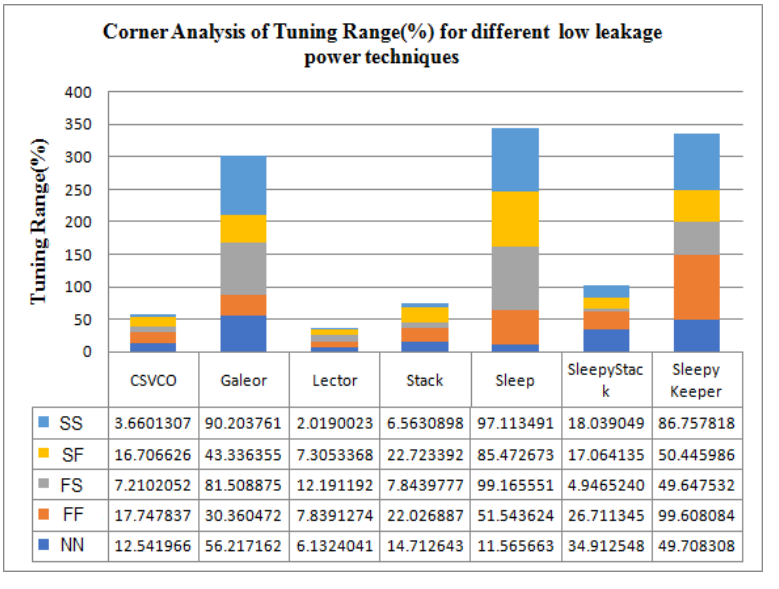


	CSVCO	Galeor	Lector	Stack	Sleep	SleepyStack	Sleepy Keeper
SS	7.65	127.6	3.368	6.887	17.27	11.78	6.875
SF	91.76	22.06	22.86	70.28	135.4	86.38	1.009
FS	36.06	67.6	18.62	23.33	59.8	29.92	0.993
FF	601.2	32.18	146.7	386.8	968.5	626.7	254.8
NN	41.7	28.55	14.35	30.45	72.11	58.89	0.9942

Fig. 5.1. Corner Analysis of Oscillating Frequency (GHz) for CSVCO applied with different low leakage techniques.

From the above plotted graph, it is observed that the oscillation frequency in all the corners remained low and, in the Gale,-or Technique is significantly reduced in all the corners.

From the below plotted graph, it is observed that the frequency tuning range calculated in percentage for all the corners in case of Sleep technique remained high and in the Lector Technique it is significantly reduced in all the corners.



	CSVCO	Galeor	Lector	Stack	Sleep	SleepyStack	Sleepy Keeper
SS	3.6601307	90.203761	2.0190023	6.5630898	97.113491	18.039049	86.757818
SF	16.706626	43.336355	7.3053368	22.723392	85.472673	17.064135	50.445986
FS	7.2102052	81.508875	12.191192	7.8439777	99.165551	4.9465240	49.647532
FF	17.747837	30.360472	7.8391274	22.026887	51.543624	26.711345	99.608084
NN	12.541966	56.217162	6.1324041	14.712643	11.565663	34.912548	49.708308

Fig.5.2. Corner analysis plot of Frequency Tuning Range (%) for CSVCO applied with different low leakage techniques.

6. SIMULATION AND RESULT ANALYSIS

To analyze the circuit and to perform the simulation results of the CSVCO implemented different low leakage techniques, the circuits has been implemented in virtuoso tool in Cadence Software in 45nm technology with a supply voltage of 0. 45V.The simulated output of the oscillator is obtained by initializing setting the output node to either 1 or 0 to get the proper oscillations. The parameters like average power (Pavg),delay, Oscillation frequency and gain are calculated at a room temperature of27℃ and with a control voltage of 0.45V.

Table 1. Simulation results for parameters with different low leakage power techniques in CSVCO.

S. No.	Low Leakage Power Techniques	Average Power (W)	Area (µm2)	Delay (µs)	Frequency (GHz)	Gain (Ghz /V)	Tuning Range (%)
1	Gale-or	48.20 e-9	37.5769	19.56	13.81	3.07	56.21
2	Lector	49.77 e-9	35.581225	32.25	14.34	3.19	6.07
3	Sleep	40.45 e-12	26.3169	327.8	72.11	16.02	98.76
4	Stack	49.56 e-9	56.4001	19.03	30.45	6.76	14.71
5	Sleep Stack	58.32 e-9	37.5769	0.4896	58.89	13.87	34.86

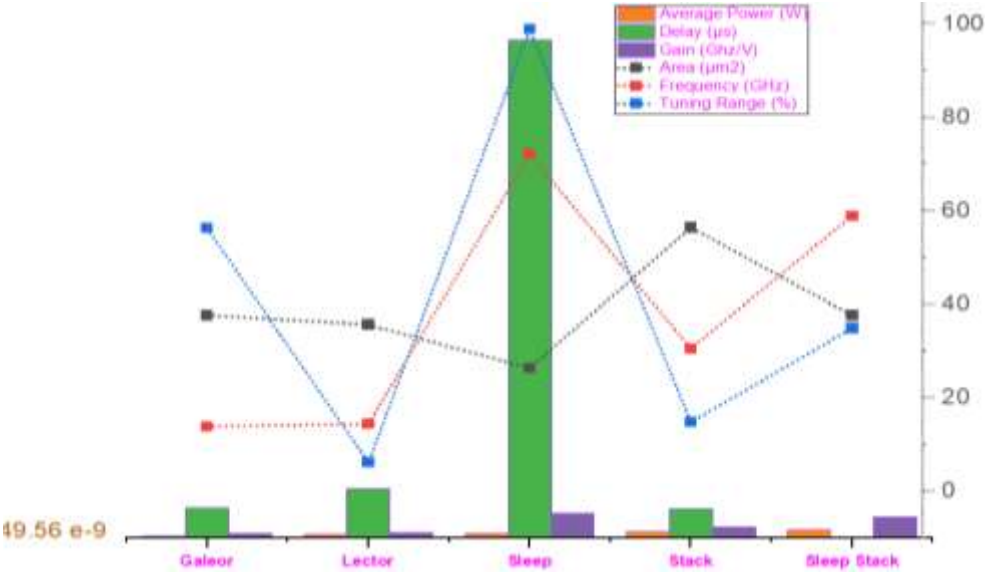


Fig. 6. Parameter analysis of CSVCO with different low leakage power techniques.

Table 2. Comparison analysis of PLL CSVCO VS sleep stack PLL CSVCO.

Parameters	PLL with basic CSVCO	Proposed work-PLL with SLEEP STACK CSVCO
VCO type	Ring	Ring
Tech (NM)	45	45
Freq (GHz)	2.592	2.759
Supply volt(v)	1	1
Power (MW)	0.002686	0.002559
P-Noise(dBc/Hz)	-72.2	-63.8
Delay(µs)	0.866	0.0006544

From the above table and simulation result of parameter analysis with low leakage power techniques, the current starved VCO with sleep stack and keeper technique overcome the challenges present in the existing VCO in wide tuning, high frequency applications. Also, these challenges include leakage power, phase noise and limited frequency range. To ensure its robustness, extensive simulations are performed under extreme conditions such as different process corners, varying control voltage, and at extreme temperatures. The proposed CSVCO PLL circuit consumes less power. It achieves 20 % improvement in oscillation frequency because of the pull-up sleepy and pull-down sleepy stack transistor arrangement. The frequency tuning range of the proposed circuit also exhibits 27 % improvement. It also achieves less delay with the phase noise and FOM improvement of 17.29 % and 10.74 % ,respectively.

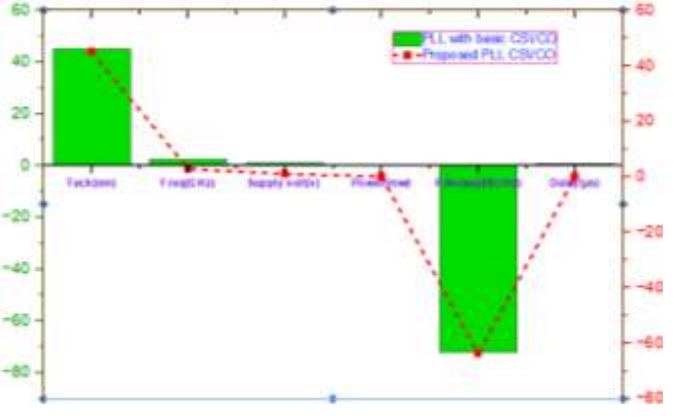


Fig. 7. Comparison analysis of PLL CSVCO & Sleep Stack PLL CSVCO.

The above figure confirms the robustness of the proposed design, making it a promising solution for high-frequency applications. These improvements are achieved at a supply voltage of 1 V. To ensure the stability of the circuit, Monte-Carlo analysis also conducted for various parameters. From the obtained results, it is concluded that the proposed design outperforms existing works in various performance parameters and it is highly suitable for PLL applications including wireless communication and radio frequency.

7.CONCLUSIONS AND FUTURE SCOPE

From the above tabular column and the graphs plotted it is observed that all the low leakage power techniques applied to the existing CSVCO are better in one or the other parameter like average power, oscillation frequency, delay and the gain. It is also observed that as the temperature is increased from corner analysis 27℃ to 80℃then the power and delay are increased and they are decreased when the temperature is decreasedto-40℃.

After comparing the various parameters of PLL implemented with Sleep Stack CSVCO and Basic CSVCO, it is observed that Sleep Stack has better performance. To achieve further, higher frequencies vary the supply voltage and the number of stages in the CSVCO from 5 stages to 7,9,11 and so on, but with increase in other parameters like area and power.

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