Signal Processing and Renewable Energy
September 2024, (pp. 1-20)
ISSN: 2588-7327
eISSN: 2588-7335

A New Non-isolated Buck-Boost DC/DC Converter Based on Cuk Topology with Single Switch for Renewable Energy Application

Mustafa Okati [1*], Mohammad Osmani-Bojd [2], Samira Samimi [3]

[1] Department of Electrical Engineering, Zabol Branch, Islamic Azad University, Zabol, Iran.
[2] Department of Electrical Engineering, Zahedan Branch, Islamic Azad University, Zahedan, Iran.
[3] Department of Mathematics Education, Farhangian University, Zahedan, Iran.

Received: 08-Apr-2024, Revised: 18-Aug-2024, Accepted: 20-Aug-2024.

Abstract

The present investigation aims to design an active switch non-isolated buck-boost DC/DC converter based on the CUK topology. In this converter, a simpler circuit topology is used to reach higher voltage gains at lower duty cycle levels. Furthermore, the mentioned converter presents a continuous input/output current with negative output polarity. Compared to the conventional method of obtaining a broader range of the voltage conversion ratio characterized by the same duty cycle, the suggested converter explains the fundamentals and prominent waveforms of the Continuous Conduction Mode (CCM). Also, the efficiency was analyzed through the substitution of the parasitic resistance effects for the steady-state circumstances. The power loss calculation, parameter design, and characteristics are completely investigated in the suggested converter, and a comparative analysis with other non-isolated converters is carried out. Eventually, by creating a working hardware prototype characterized by a 48-watt power output, the practicality of the suggested converter is confirmed by the empirical data gathered from testing.

Keywords: Cuk Converter, Buck-Boost Converter, Switching Device Power, Continuous Input/output Current, Single Switch.

1. INTRODUCTION

Numerous investigations have been conducted globally to investigate sustainable energy alternatives in response to the progressively diminishing availability of natural resources and their detrimental impact on the environment. Photovoltaic (PV) and wind power generation, among

*Corresponding Authors Email: Mu.okati@gmail.com

other renewable energy sources, have garnered considerable attention in recent years. Renewable energy sources have emerged as a highly desirable option owing to their favorable environmental and economic characteristics. Nevertheless, several challenges, including low output voltage, persist with their utilization. Distributed generation systems refer to localized, small-scale power generation systems that utilize renewable sources of energy to meet the growing electricity demand and also address environmental concerns. There are various sustainable energy technologies, including fuel cells and solar photovoltaic (PV) systems. Several renewable energy sources can be integrated within a Direct Current (DC)

microgrid, as illustrated in Fig.1. A direct current (DC) microgrid presents itself as the most feasible resolution for the assimilation of photovoltaic (PV) generation systems in combination with DC loads and alternating current (AC) power grid. The utilization of Solar Photovoltaic (PV) systems holds a significant position amongst alternative energy sources for Direct Current (DC) distributed generation systems [1], [2]. The microgrid system can operate in both grid-connected mode and islanding mode with a primary focus on maintaining system consistency and sustainability, as outlined in the source [3]. Highly significant DC-DC converters with high voltage gain are fundamental in the upward regulation and mitigation of low and variable DC voltages, ranging from 12 V to 128 V, which are derived from solar photovoltaic systems within DC microgrid contexts. The aforementioned DC microgrid systems have bus bar voltages of up to 400 V DC, as stated by various sources [4]-[7]. High voltage gain direct current/direct current (DC/DC) converters are primarily designed to offer a substantial conversion ratio and superior efficiency while occupying minimal physical space [8].

Numerous high step-up DC-DC converter topologies have been put forth in the existing literature to attain a substantial voltage gain with a reasonable duty ratio while ensuring high converter efficiency and minimal voltage stress across components [9]. By utilizing the traditional boost DC-DC converter, it is possible to attain a substantial increase in voltage. Nevertheless, the voltage stress applied to the switch corresponds to the output voltage, and the amplification in voltage is restricted by the stress in voltage/current that passes through the switch when operating at high-duty cycle levels. As per the literature [10], [32], opting for a switch with a high rating to fulfill the voltage

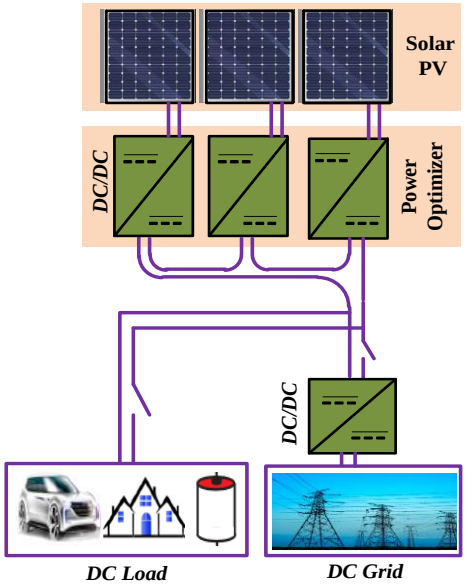


Fig.1. Structure of DC/DC converter application.

stress requirement eventually results in elevated conduction loss. To accomplish substantial voltage amplification, various converter structures, including the half/full-bridge, flyback, push/pull, and forward converters, have been proposed in the literature. Such improvement is achieved by modifying the turn ratio of the transformer or coupled inductor, as described in previous works [11]-[14]. Notwithstanding the advantages offered by converter structures, there exist certain limitations that must be acknowledged. These drawbacks include circuitry of significant size, high voltage spikes in switch operations, power dissipation, the risk of transformer core saturation, and an increased level of voltage stress for converter active switches due to the transformer leakage inductance. Moreover, the inclusion of a high-frequency transformer, non-dissipative snubber circuit, and supplementary active clamping circuit serve to amplify the monetary and dimensional expenditures of these converters [15], [16].

In situations where galvanic insulation is not deemed necessary, non-isolated DC-DC converters have been employed as a means of achieving a considerable voltage gain, thereby resulting in decreased overall dimensions, weight, and volume due to the absence of a high-frequency transformer, and consequently leading to an enhanced level of efficiency. The discussion of diverse non-isolated converter topologies in the extant literature can be classified into two categories: those equipped with broad conversion range converters and those without, as outlined in previous studies [17], in the quadratic converters, the switch voltage stress level is congruent with that of the output voltage, as established by prior studies [18]. Conversely, in the cascade boost converter, despite the possibility of amalgamating the two switches for the sake of diminishing circuit complexity, the switch remains subjected to formidable voltage and current stresses [19]. The main drawback of converter designs using switched capacitor cells and voltage lift cells is the increased stress on power switches and diode currents caused by the presence of capacitor networks. This can lead to decreased efficiency. However, incorporating the interleaved converter method along with fewer control switches and a smaller filter size can enhance efficiency and performance [20]. Nonetheless, the integration of multiple converters in a parallel configuration result in a significant surge in intricacy and the accompanying drive circuitry. Additionally, this methodology is characterized by a series of adverse implications that comprise intricate switching control reasoning, elevated voltage/current tension, and substantial energy dissipation [21]. Additionally, a new quadratic converter was unveiled [22]. To address the issue of power discontinuities in both the input and output, this converter was equipped with inductive filters at both the input and output. In addition, there were a number of components with the input and output polarities reversed. Additionally, ZETA DC-DC converters are available; they were recently proposed in [23]. Only twice as much voltage gain is present in the ZETA converter proposed here as there is in the traditional ZETA converter. Certain research suggested the use of a quadratic buck-boost converter, which

requires two gate drivers for each power switch. As a result, the converter's size and control system complexity have grown [24]. In [25], a quadratic DC/DC converter with positive output polarity was developed and examined. The converter's voltage gain ratio is modest, though, because continuous current flows through both the input and output terminals. The converter in [26] proposes a quadratic buck–boost converter with negative output. Since inductive filters are installed in the output and input ports, the structure's output and input currents are continuous. In addition to having a discontinuous input current, a lower voltage gain ratio, and less voltage stress on the components, a novel quadratic buck-boost converter was presented [27]. A mathematical analysis of various topologies has been conducted to thoroughly understand the dynamic behavior of the converter [28]. The voltage gain in the ZETA converter is twice the voltage gain provided by the typical ZETA converters. Here is a transformerless DC/DC converter design featuring dual operation modes buck/boost. The system functions as a common ground with a continuous input current between the output and input terminals due to its simple and common configuration [29]. Renewable energy (RE) systems require stable voltage and current for effective energy management. The quadratic output voltage gain of this converter allows it to handle a wider range of input voltages while ensuring optimal performance. Also, continuous input and output current ports make it particularly suitable for fluctuating power sources such as solar panels and wind turbines [30].

In addition, cascaded boost converters [31] featuring quadratic voltage gain specifications are suggested in which the voltage stress is decreased on passive devices, and the count of components is minimized. Nonetheless, compared to other models, in one such model, the voltage gain remains lower. In addition, separate control grounds are demanded by both models for the purpose of semiconductor switches that demand two control power supplies.

The present study proposes a new converter topology aimed at achieving a considerable voltage gain while reducing the current stress applied to the active switch; thereby continuous input/output current port with negative polarity is presented. The suggested configuration offers several benefits including a substantial amplification of voltage, minimal strain on the current, reduced conduction loss in the active switch, and enhanced efficiency.

The paper is structured in the following. In Section 2, the suggested converter is presented first, and then theoretical analysis and steady-state assessment are carried out. In Section 3, the benefits of the suggested converter are contrasted with those of similar converters. Section 4 discusses the results of the PLECS simulation and the experimental findings of the suggested converter's laboratory-made prototype. Lastly, Section 5 presents the key conclusions.

2. PROPOSED TOPOLOGY

The schematic diagram of the power circuit for the suggested converter is presented in Fig.2. The circuit comprises three inductors, L_1, L_2 and L_3 which possess

identical inductance values. Additionally, one switch S_1 is concurrently activated (ON) and deactivated (OFF). The circuit comprises two diodes (D_1-D_2) and four capacitors (C_1-C_3). The present discussion focuses on elucidating the operative mechanisms and conducting a comprehensive steady-state analysis of the proposed converter in Continuous Conduction Mode (CCM).

Time-domain characteristic waveforms from Fig. 3 provide a vivid representation of several of the charging and discharging stages.

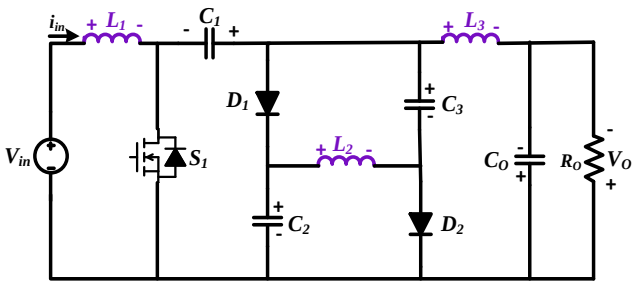


Fig.2. Proposed converter configuration.

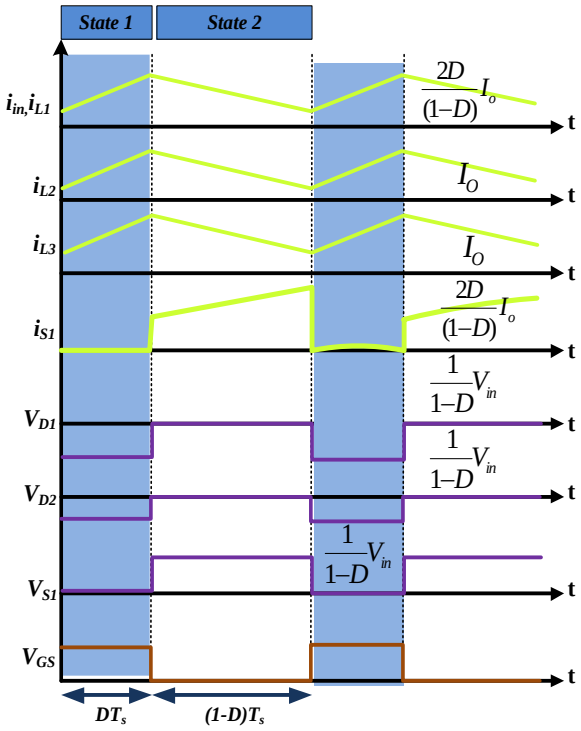


Fig.3. Charging and discharging states key waveforms in the proposed converter's CCM mode

A. Working Principle in CCM

The suggested converter comprises a switch that functions concurrently with duty cycles. Accordingly, the suggested converter functions in two distinct modes while operating in continuous conduction mode functions specifically referred to as a state1 and state 2. According to Fig. 4 and 5, there

are two major operating states assumed for the converter in the CCM.

***State* 1:** During mode, switch S_1 is maintained in the open (ON) position and both diode D_1 and D_2 are off. The schematic representation of the proposed converter for this mode is illustrated in Fig.4. The input voltage supply, denoted as V_{in}, facilitates the charging of inductor L_1 through switch S_1, while the stored energy within capacitor C_o is transferred towards the load R_o. Consequently, it is possible to formulate the voltages across the inductors L_1, L_2, and L_3, in a precise manner, as follows:

$$V_{L1} = V_{in} \quad (1)$$

$$V_{L2} = -V_{C1} + V_{C2} + V_{C3} \quad (2)$$

$$V_{L3} = V_{C1} - V_o \quad (3)$$

***State* 2**: In this mode of operation, it is noted that switch S_1 is switched to the OFF position and the Diodes are ON. The equivalent circuit of the proposed converter is illustrated in Fig.5. The input voltage supply V_{in} denoted as serves to charge several components including the inductors L_1 and capacitors C_1, and C_2 all through using of diode D_1. Simultaneously, capacitor C_3 undergoes charging through diode D_2 via the input supply voltage V_{in}, inductor L_1, capacitor C_1, hence, it is possible to determine the voltages across the inductors L_1, L_2, and L_3 through the utilization of equations (4), (5), and (6).

$$V_{L1} = V_{in} + V_{C1} - V_{C2} \quad (4)$$

$$V_{L2} = V_{C2} \quad (5)$$

$$V_{L3} = V_{C3} - V_o \quad (6)$$

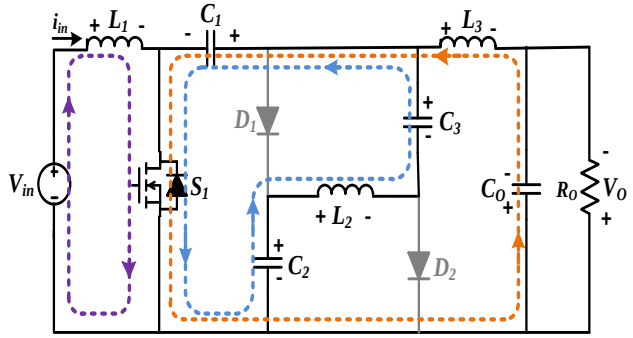


Fig. 4. Operating mode of State 1.

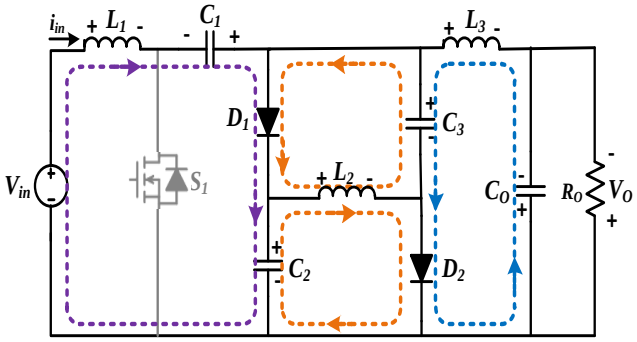


Fig. 5. Operating mode of State 2.

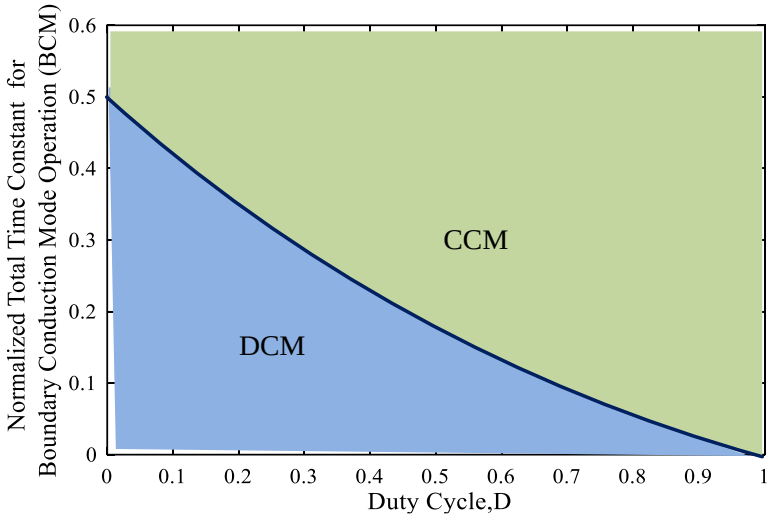


Fig. 6. Boundary condition (CCM and DCM).

The voltages of the capacitors C_3, C_2, and C_1, as well as the output voltage, are determined by using the volt-second balance on the inductors voltage as described in (1)–(6),

$$V_{C2} = V_{C3} = \frac{D}{1-D} V_{in} \tag{7}$$

$$V_{C1} = \frac{1}{D(1-D)} \tag{8}$$

It can be observed that the voltage across the output capacitor Co is equivalent to the output voltage Vo. it can be concluded that,

$$V_o = \frac{2D}{(1-D)} V_{in} \tag{9}$$

The symbol D denotes the duty cycle. The ampere-second balance principle of capacitors C_1, C_2, and C_3 is used to calculate the mean current value of all inductor currents. Therefore, I_{L1}, I_{L2} and I_{L3} currents can be calculated:

$$I_{L1} = \frac{2D}{(1-D)} \tag{10}$$

$$I_{L2} = I_{L3} = I_o \tag{11}$$

The output voltage and current can be obtained as follows,

$$V_o = \frac{2D}{(1-D)} V_{in} \tag{12}$$

$$I_o = \frac{1-D}{2D} I_{in} \tag{13}$$

In this manner, the voltage gain,

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{2D}{(1-D)} \tag{14}$$

B. Boundary Condition

The normalized time constant for the inductor, denoted as τ_L, can be defined as τ_L= L/ (RTs). Fig. 6 depicts the voltage gain deviation in the discontinuous conduction mode of the suggested converter in response to modifications in the duty cycle. One may obtain boundary conditions through the process of equating the M_{CCM} and M_{DCM}. Hence, the normalized boundary time

constant about the inductor denoted by τ_{LB}, can be derived as

$$\tau_{LB} = \frac{(1-D)^2}{2} \quad (15)$$

According to the findings obtained, it is evident that Fig. 6 illustrates the boundary condition of both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) of the suggested converter with respect to it. Furthermore, it must be noted that in cases where $\tau_{\_L}$ exceeds τ_{LB}, the converter under consideration operates in continuous conduction mode (CCM).

C. Inductors Design

We can find the same amount of electrical energy across both L_1 and L_2 by measuring the voltage produced.

$$V_{L1,2} = L_{1,2}\frac{di_{1,2}}{dt} \quad (16)$$

The inductor size is picked depending on how much electricity needs to be charged, how much it moves up and down, how often it is turned on and off, and how fast it switches. We can find out how much electric current flows through each inductor when the batteries are being charged by doing the following:

$$\Delta i_{L1,2,3} = \frac{DV_{L1,2,3}}{L_{1,2,3}f_s} \quad (17)$$

The ripple currents for two inductors, L_3, L_2 and L_1 are labeled as $\Delta i_{L3}, \Delta i_{L2}$ and Δi_{L1}. So, amount of inductors,

$$L_{2,3} \geq \frac{(1-D)V_o}{4I_o f_s} \quad (18)$$

$$L_1 \geq \frac{(1-D)^2 V_o}{8DI_o f_s} \quad (19)$$

Therefore, three inductor values can be selected based on (18)-(19). Also, $\Delta i_{L3,2,1}$ is 10-30% of the nominal inductor current value.

D. Capacitors Design

Capacitor capacitance is controlled by charging current, voltage across, charging rate, and replacement frequency. Therefore, the capacitor voltage ripple is given by:

$$\Delta V_{C1,2,3} = \frac{Di_{C1,2,3}}{C_{1,2,3}f_s}, \Delta V_{Co} = \frac{Di_{Co}}{C_o f_s} \quad (20)$$

We can find out the right amount of capacitors C_1, C_2, C_3, and we need using equations (20),

$$C_1 \geq \frac{2DV_o}{\Delta V_{C1}R_o f_s} \quad (21)$$

$$C_{2,3} \geq \frac{DV_o}{\Delta V_{C2,3}R_o f_s} \quad (22)$$

$$C_o \geq \frac{(1-D)V_o}{16L_3\Delta V_{C1}R_o f_s^2} \quad (23)$$

E. Voltage and Current Stress on Semiconductor

The voltage and current stresses of the diodes and switch of a converter contribute to its power loss and the final cost of implementation. Therefore, theses stresses must be assessed,

$$V_{S1} = \frac{1}{1-D}V_{in} \quad (24)$$

$$I_{S1} = \frac{2D}{1-D} I_o \tag{25}$$

$$V_{D1,2} = \frac{1}{1-D} V_{in} \tag{26}$$

$$I_{D1,2} = I_o \tag{27}$$

F. Efficiency Analysis

Fig. 7 shows the suggested converter circuit, taking into account the nonidealities of various circuit components. The same placement resistance (ESR) of inductors L_1, L_2, and L_3 are shown separated by an R_{L1}, R_{L2} and R_{L3}. Additionally, $R_{FD1}$and R_{FD2} are internal resistors. The forward voltage drops of diodes D_1 and D_2 are V_{FD1} and V_{FD2} respectively. The forward ON resistances of control switch S_1 are shown by R_{DS1}.

The *RMS* value of the switch current, and the diodes current, inductors current, and capacitors current, of the circuit was first calculated by equations (25), (27), (10), and (11),

$$I_{S1-rms} \approx \frac{2\sqrt{D}}{(1-D)} |I_o| \tag{28}$$

$$I_{D1,2(rms)} \approx \frac{(1+D)^{1/2}}{(1-D)^{1/2}} I_o \tag{29}$$

$$I_{L1-rms} \approx \frac{2D}{(1-D)} |I_o| \tag{30}$$

$$I_{L2,3-rms} \approx |I_o| \tag{31}$$

$$I_{C1-rms} \approx \left(\frac{4D}{1-D}\right)^{\frac{1}{2}} |I_o| \tag{32}$$

$$I_{C2,3-rms} \approx \left(\frac{2D}{1-D}\right)^{\frac{1}{2}} |I_o| \tag{33}$$

The total power loss of the switch (P_{S1}) comprises the sum of switching losses ($P_{S\text{-}L}$) and conducting power dissipation ($P_{R\text{-}DS}$), as well as the conduction resistance R_{DS} of the power switch, which is calculated as:

$$P_{S_1} = P_{R-DS} + P_{S-L} \tag{34}$$

$$\begin{cases} P_{R-DS} = R_{DS} I^2_{S-rms} = R_{DS} \dfrac{D^3}{(1-D)^4} I_o^2 \\ P_{S-L} = f_S C_S V_S^2 = f_S C_S \dfrac{1}{(1-D)^2} V_{in}^2 \end{cases} \tag{35}$$

$$\begin{aligned} P_D &= P_{FD} + P_{FR} \\ &= \sum_{i=1}^{i=2} (R_{FD} I^2_{Di-rms}) \\ &\quad + \sum_{i=1}^{i=2} (V_{FDi} I_{Di}) \end{aligned} \tag{36}$$

To calculate the power losses of inductors and capacitors, it can use their equivalent series resistance (ESR), RL, and RC values:

$$P_L = \sum_{i=1}^{i=3} (P_{Li}) = \sum_{i=1}^{i=3} (R_{Li} I^2_{Li-rms}) \tag{37}$$

$$P_{C-Total} = P_{C1} + P_{C2} + P_{C3} + P_{Co} \tag{38}$$

The total loss of the power converter may be summed up as follows:

$$P_{loss-Total} = P_C + P_L + P_S + P_D \tag{39}$$

Lastly, the following equation can be used to determine the efficiency of the proposed converter:

$$\eta = \frac{P_o}{P_{loss-Total} + P_o} \tag{40}$$

Fig. 8 displays the pie charts of the losses in step-up/down modes so that the power losses of each element's fraction can be understood. In comparison to the step-up mode, the efficiency in the step-down mode is computed as being lower.

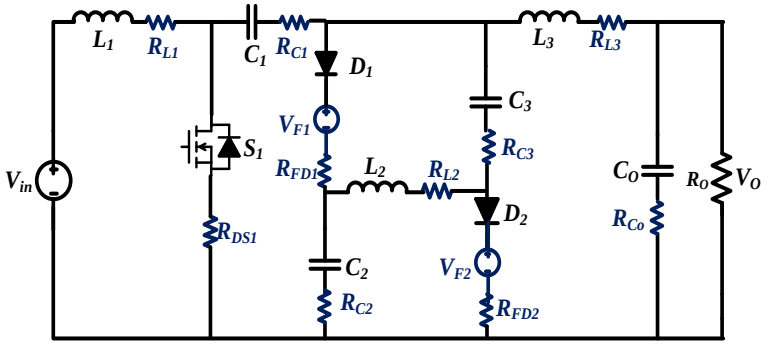
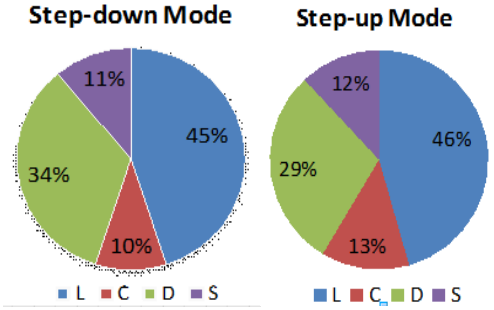


Fig. 7. Simplify the proposed converter by using parasitic parameters.



(a) ***(b)***

Fig. 8. Pie chart power loss. (a) Step-down mode, (b) Step-up mode.

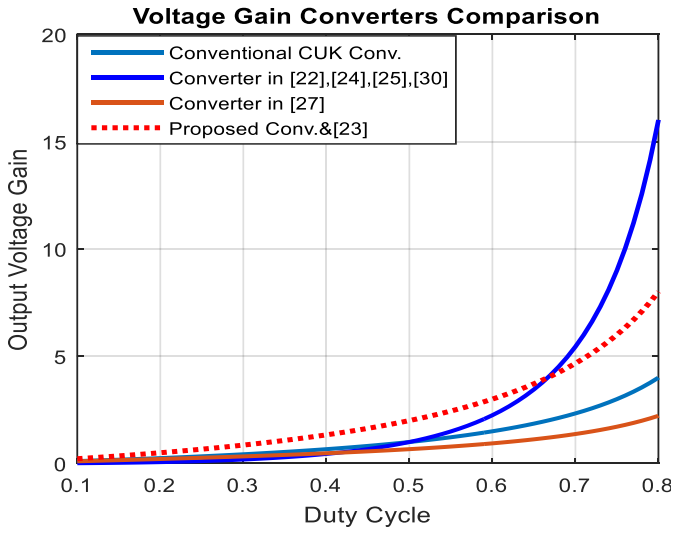


Fig. 9. Comparison of voltage gain with other similar converters.

Table 1. ***Comparative of the proposed converter with other similar converters.***

Ref.	Elements				Total Elements	V_D/V_{in}	V_S/V_{in}	M_{CCM}	Norm. SDP_{avg}/P_o	$\sum \frac{Vs}{Vin}$	Output Polarity	Continuous Input/output
	L	C	D	S								
CUK	2	2	1	1	6	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{D}{1-D}$	----------	$\frac{1}{1-D}$	Negative	YES/YES
IN [30]	2	2	3	3	10	$\frac{\frac{1}{1-D}}{\frac{D}{(1-D)^2}}$	$\frac{\frac{1}{1-D}}{\frac{D}{(1-D)^2}}$	$\left(\frac{D}{1-D}\right)^2$	$\frac{D^2-D+2}{D(1-D)}$	$\frac{1}{(1-D)^2}$	Positive	YES/YES
IN [29]	2	2	2	2	8	$\frac{1}{1-D}$ $\frac{1}{(1-D)^2}$	$\frac{1}{1-D}$ $\frac{1}{(1-D)^2}$	$\frac{D}{(1-D)^2}$	$\frac{1+D}{D(1-D)}$	$\frac{2-D}{(1-D)^2}$	Positive	YES/NO
IN [22]	3	3	5	1	12	$\frac{1}{1-D}$ $\frac{D}{(1-D)^2}$ $\frac{1}{(1-D)^2}$ $\frac{1}{1-D}$ $\frac{D}{(1-D)^2}$	$\frac{1}{1-D}$ $\frac{1}{(1-D)^2}$	$\left(\frac{D}{1-D}\right)^2$	$\frac{6D^2-8D+4}{D(1-D)^2}$	$\frac{1}{(1-D)^2}$	Negative	YES/YES
IN [23]	3	4	2	1	10	$\frac{1}{1-D}$ $\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{2D}{1-D}$	$\frac{1}{D(1-D)}$	$\frac{1}{1-D}$	Positive	NO/YES
IN [24]	3	3	2	2	10	$\frac{1}{1-D}$ $\frac{D}{(1-D)^2}$	$\frac{1}{1-D}$ $\frac{D}{(1-D)^2}$	$\left(\frac{D}{1-D}\right)^2$	$\frac{1+D}{D(1-D)}$	$\frac{1}{(1-D)^2}$	Positive	YES/YES
IN [25]	3	3	2	2	10	$\frac{1}{1-D}$ $\frac{D}{(1-D)^2}$	$\frac{1}{1-D}$ $\frac{D}{(1-D)^2}$	$\left(\frac{D}{1-D}\right)^2$	$\frac{1+D}{D(1-D)}$	$\frac{1}{(1-D)^2}$	Positive	YES/YES
IN [26]	3	3	2	2	10	$\frac{1}{1-D}$ $\frac{1}{(1-D)^2}$	$\frac{1}{1-D}$ $\frac{1}{(1-D)^2}$	$\frac{D}{(1-D)^2}$	$\frac{1+D}{D(1-D)}$	$\frac{1}{(1-D)^2}$	Negative	YES/YES
IN [27]	2	2	3	1	8	$\frac{1}{1-D^2}$ $\frac{D}{1-D^2}$ $\frac{D}{1-D^2}$	$\frac{1}{1-D}$	$\frac{D}{1-D^2}$	$\frac{1+3D^2-2D^3}{D-D^3}$	$\frac{1}{1-D}$	Negative	NO/NO
Proposed	3	3	2	1	10	$\frac{1}{1-D}$ $\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{2D}{1-D}$	$\frac{1}{D(1-D)}$	$\frac{1}{1-D}$	Negative	YES/YES

3. COMPARATIVE ANALYSIS

The proposed buck-boost converter is compared to others in references [22]-[27] and [30], with a detailed analysis of factors like component count, normalized gain voltage, stress on switches and diodes, output polarity, continuous output/input current, and switching device power. The comparison demonstrates that the proposed converter exhibits superior voltage step-up across various duty cycles compared to those in [22]-[25], [27], and [30], as illustrated in Fig. 9.

The power loss and total implementation cost of a power converter are influenced by the current and voltage stress placed on its diodes and switches. Thus, it is necessary to assess these strains. As previously indicated in [33], the switching device power, or SDP, can be used as an illustrative metric to measure the converter cost and the power

loss. The formula for calculating the overall average switching device power (SDP_{avg}) is as follows:

$$SDP_{avg} = \sum_{i=1}^{n} V_{pk\_i} I_{avg\_i} \quad (41)$$

where I_{avg_i} and V_{pk_i} represent the average current and peak voltage during a switching period of the i^{th} semiconductor used in a power converter. The peak voltage and average current are computed for the diodes and the switch in the proposed converter. Overall average SDP is calculated,

$$SDP_{avg} = \left(\frac{1}{D(1-D)} \right) P_o \quad (42)$$

where P_o represents the output power.

The overall average SDPs of the several converters are presented in Fig. 10. It is noted that the recommended converter has a lower SDP than its rivals, which essentially means that there will be less power loss and semiconductor cost.

The voltage stress on the switch:

$$V_{S1} = \frac{1}{1-D} V_{in} \quad (43)$$

In Fig. 11, there is a comparison between the normalized sum of the voltage stress across power switches of the proposed converter and other similar converters. Additionally, Table 1 provides details on the voltage stress across power switches for other competing converters.

4. EXPERIMENTAL ANALYSIS

A 48W output power prototype of the proposed converter is constructed. A listing detailing the specific circuit components of the model is provided in Table 2. Fig. 12 illustrates simulation waveforms of the proposed converter operating in both step-down and step-up modes in Continuous Conduction Mode (CCM) using PLECS software. It is plotted gate-source voltage, switch voltage, inductor currents, diodes voltage, and output voltage.

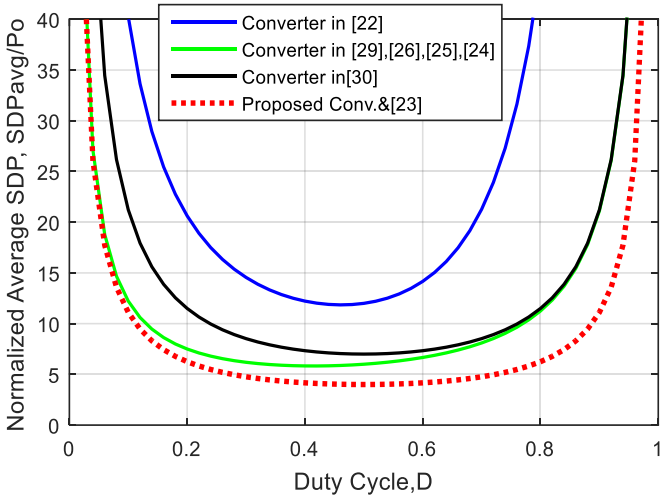


Fig. 10. Normalized total average switching device power (SDPavg/Po) of proposed converter vs other converter.

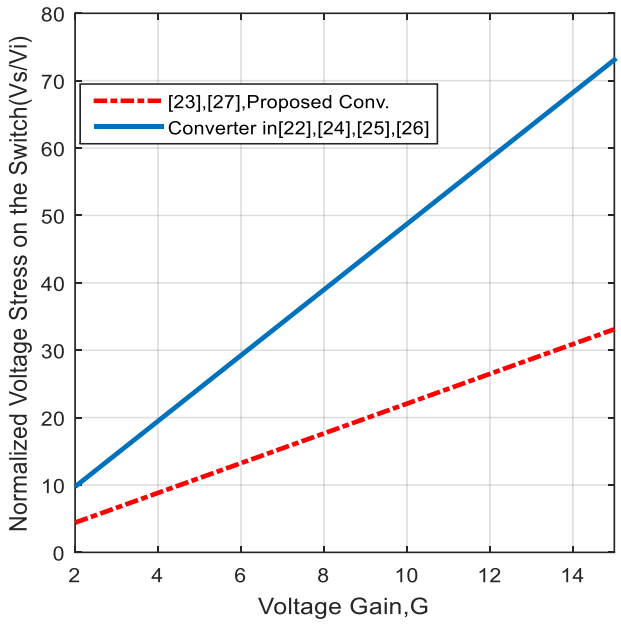


Fig. 11. Comparison of normalized switch voltage stress.

Table 2. ***Design considerations for the proposed converter***

Items	Prototype
fs	33KHZ
Duty Cycle	0.572 (step-up), 0.207 (step-down)
D_1/D_2	MBR10100 (V_F ~ 0.85V)
S_1	IRFP4668PBF (R_{DS} = 8mΩ)
C_1 / C_2 /C_o R_{C1} / R_{C2} / R_{Co}	33µF, 33µF, 160 µF 0.051Ω,0.078, 0.022Ω
L_1 / L_2 / L_3 R_{L1} / R_{L2} / R_{L3}	425µH, 860µH, 525 µH 0.035Ω, 0.157Ω,0.056 Ω
Vin	18V
V_o	48V (step-up),10V(step-down)

Fig. 13 shows a prototype created in the laboratory. The functioning of the converter and the numerical analysis have been validated using the lab prototype shown in Figs. 14 and 15. In these figures, the waveforms of the voltages and currents of the suggested converter are appeared in two modes that were measured in the laboratory. The efficiency of the proposed buck-boost converter with varying input voltages at different output powers is illustrated in Fig. 16. Since a high-duty cycle is necessary to achieve a high voltage gain by lowering the input voltage and so increasing conduction losses, the efficiency was reduced related to the input voltage drop. Since a high-duty

cycle is needed to achieve a high voltage gain by lowering the input voltage and thus increasing conduction losses, the efficiency was reduced concerning the input voltage drop. Fig. 17 shows the proposed converter's efficiency vs output power. Theoretical and experimental efficiencies are approximately the same, except for the step-up mode, which has a greater current ripple than the step-down mode.

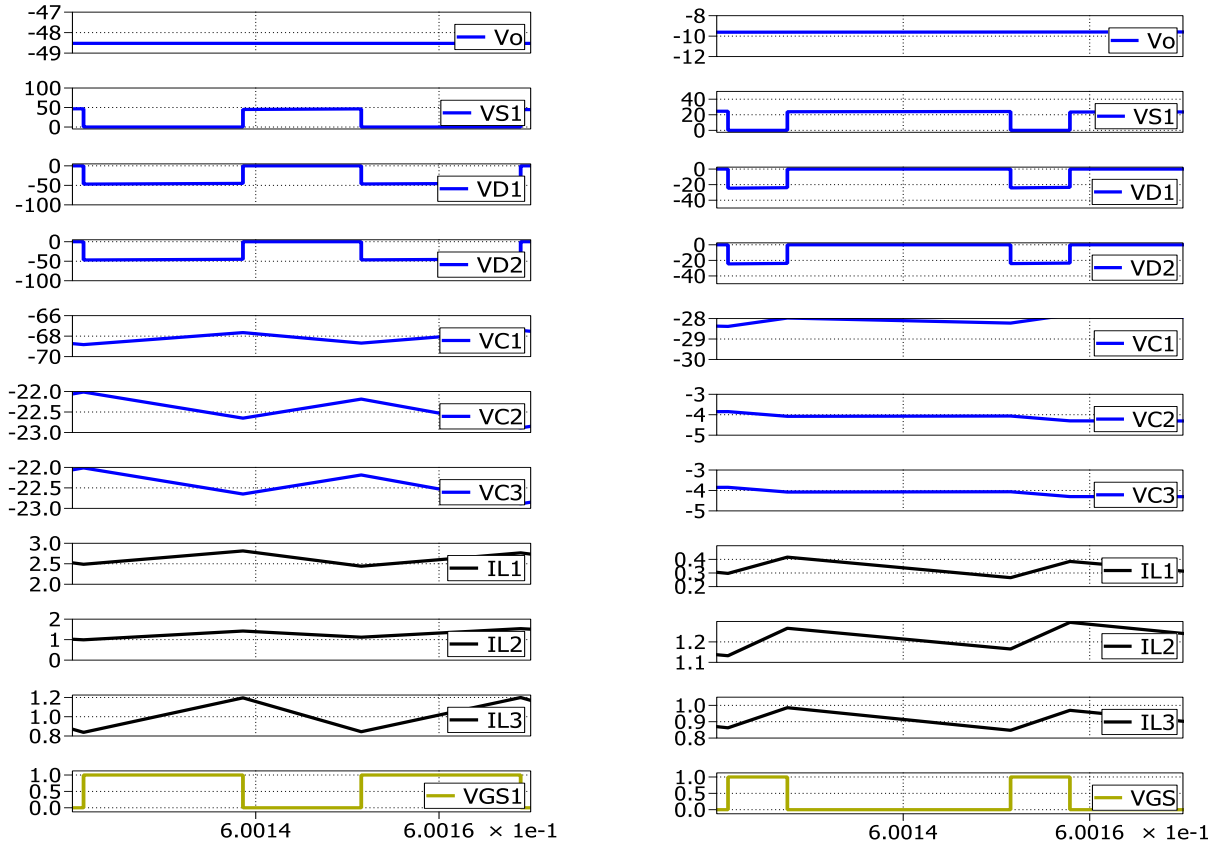


Fig.12. Simulation waveforms in PLECS of the proposed converter. (a) Step-up mode; (b) Step-down mode.

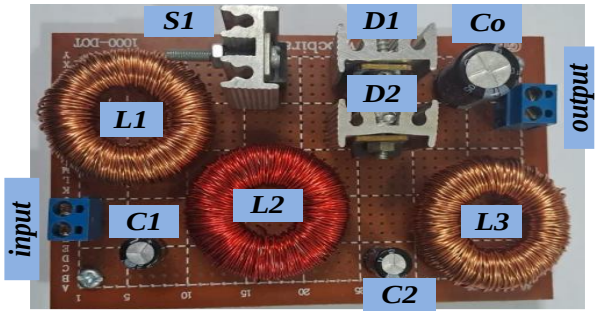
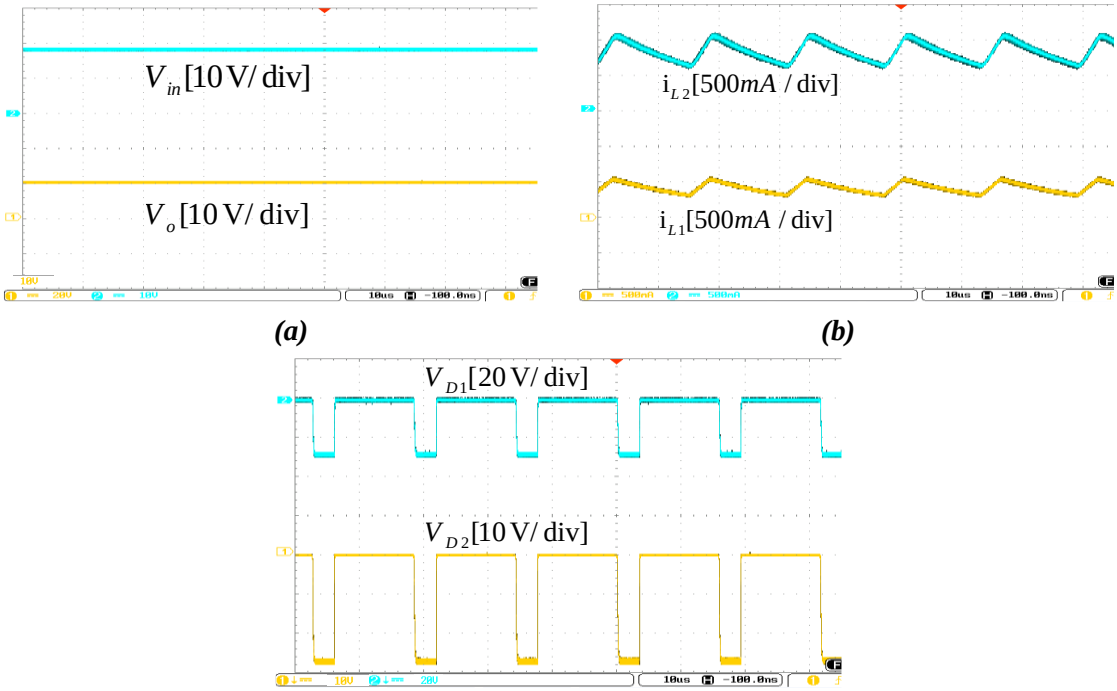


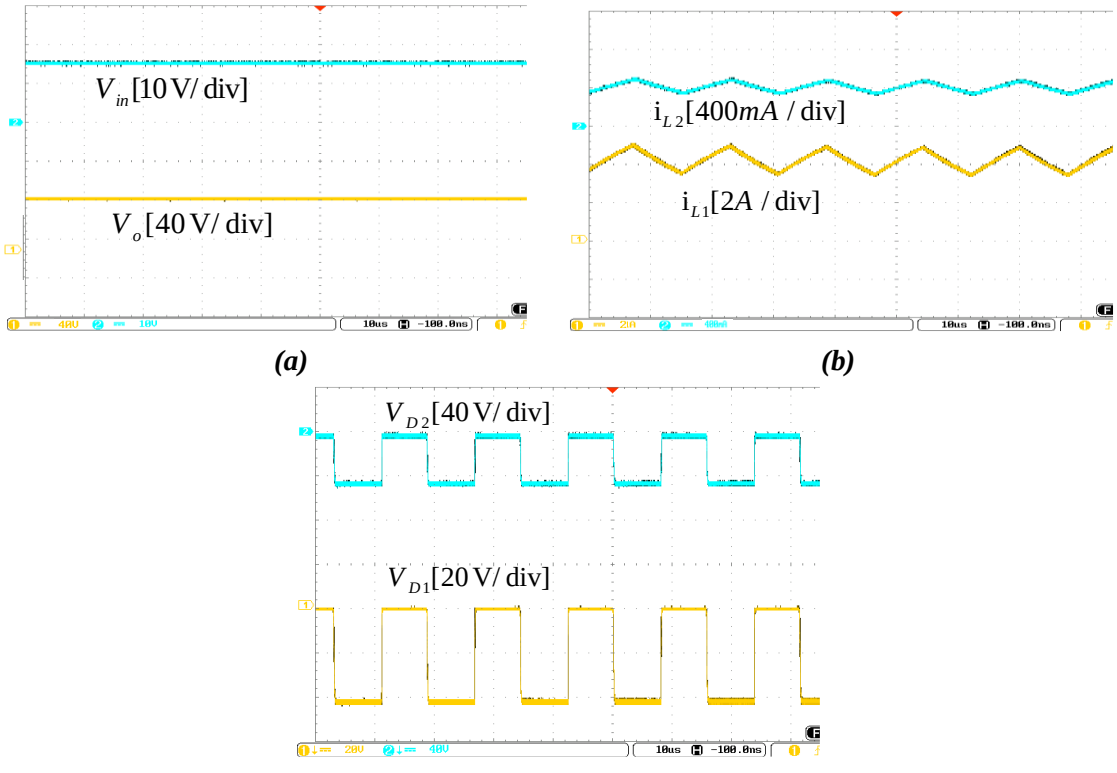
Fig. 13. Laboratory made prototype



(a) ***(b)***

(c)

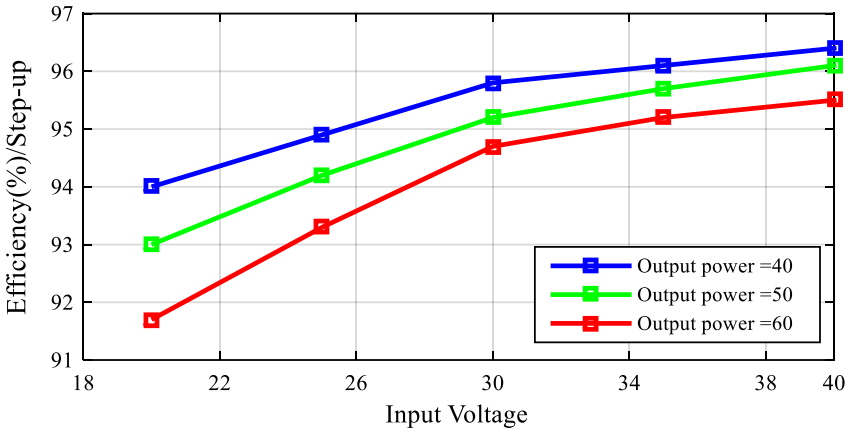
Fig. 14. Results of Laboratory in the step-down mode; (a) Vin, Vo; (b) iL1, iL2; (c) VD1, VD2.



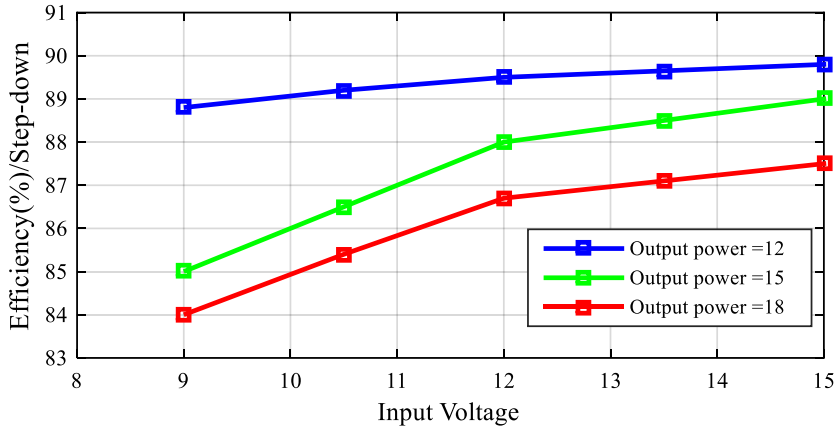
(a) ***(b)***

(c)

Fig.15. Results of Laboratory in the step-up mode; (a) Vin, Vo; (b) iL1, iL2; (c) VD1, VD2.

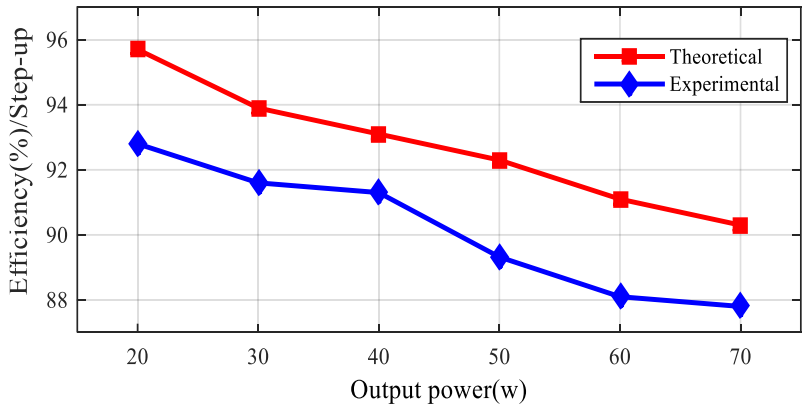


(a)

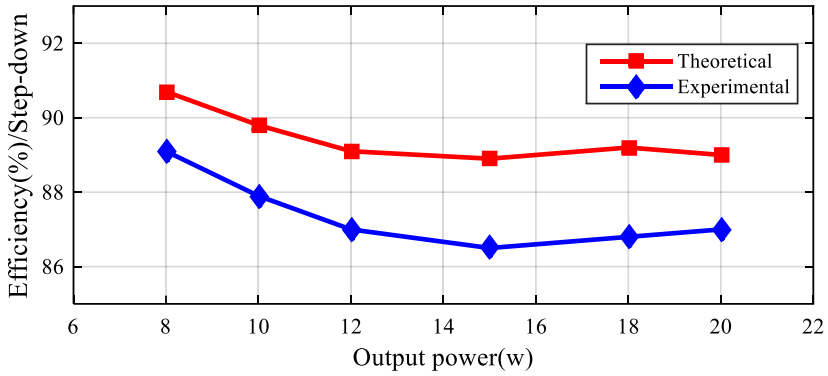


(b)

Fig. 16. Measured efficiency versus different input voltages and variable output powers (a) Step-up mode, (b) Step-down mode.



(a)



(b)

Fig. 17. Results of theoretical and experimental efficiency versus output power (a) Step-up mode (b) Step-down mode.

5. CONCLUSION

This investigation presents a DC-DC buck-boost converter characterized by negative output polarity for renewable energy purposes. In the suggested converter, a single switch is used in order to simplify the power MOSFET driving circuit and minimize the power loss. When employing the continuous input/output current port, less current ripple is observed in the output and input. A range of duty cycle values are employed for testing purposes in order to analyze and approve the functionality of the concerned converter. The efficiency of the suggested converter at an output power of 48W is 90.1%. In addition, the input/output current continuous characteristic of the suggested converter turns it into a suitable candidate for the purposes demanding a negative voltage source, e.g., multipurpose power supplies, photovoltaic systems, audio amplifiers, data transfer interfaces, and signal generators.

REFERENCES

[1] T. M. S. Bhaskar, M. Meraj, A. Iqbal, S. Padmanaban, P. K. Maroti, and R. Alammari, "High gain transformer-less double-duty-triplemode DC/DC converter for DC microgrid," IEEE Access, vol. 7, pp. 36353-36370, 2019.

[2] P. K. Maroti, S. Padmanaban, M. S. Bhaskar, M. Meraj, A. Iqbal, and R. Al-Ammari, "High gain three-state switching hybrid boost converter for DC microgrid applications," *IET Power Electron.*, vol. 12, no. 14, pp. 3656-3667, Nov. 2019.

[3] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-up DC_DC converters: A comprehensive review of voltage boosting techniques, topologies, and applications," IEEE Trans. Power Electron., vol. 32, no. 12, pp. 9143-9178, Dec. 2017.

[4] D. Kumar, F. Zare, and A. Ghosh, "DC micro grid technology: System architectures, AC grid interfaces, grounding schemes, power quality, communication networks, applications, and standardizations aspects," IEEE Access, vol. 5, pp. 12230-12256, 2017.

[5] N. Swaminathan and N.

Lakshminarasamma, "The steady-state DC gain loss model, efficiency model, and the design guidelines for high-power, high-gain, low-input voltage DC_DC converter," IEEE Trans. Ind. Appl., vol. 54, no. 2, pp. 1542-1554, Mar. 2018.

[6] R. Moradpour, H. Ardi, and A. Tavakoli, ``Design and implementation of a new SEPIC-based high step-up DC/DC converter for renewable energy applications," IEEE Trans. Ind. Electron., vol. 65, no. 2, pp. 1290-1297, Feb. 2018.

[7] P. K. Maroti, S. Esmaeili, A. Iqbal, and M. Meraj, "High step-up single switch quadratic modified SEPIC converter for DC microgrid applications," IET Power Electron., vol. 13, no. 16, pp. 3717-3726, Dec. 2020.

[8] I. Laird and D. D.-C. Lu, "High step-up DC/DC topology and MPPT algorithm for use with a thermoelectric generator," IEEE Trans. Power Electron., vol. 28, no. 7, pp. 3147-3157, Jul. 2013.

[9] E. Babaei, H. Mashinchi Maheri, M. Sabahi, and S. H. Hosseini, "Extendable nonisolated high gain DC_DC converter based on active passive inductor cells," IEEE Trans. Ind. Electron., vol. 65, no. 12, pp. 9478-9487, Dec. 2018.

[10] M. Lakshmi and S. Hemamalini, "Nonisolated high gain DC_DC converter for DC microgrids," IEEE Trans. Ind. Electron., vol. 65, no. 2, pp. 1205-1212, Feb. 2018.

[11] M. Forouzesh, K. Yari, A. Baghramian, and S. Hasanpour, "Single-switch high step-up converter based on coupled inductor and switched capacitor techniques with quasi-resonant operation," IET Power Electron., vol. 10, no. 2, pp. 240-250, Feb. 2017.

[12] H.-L. Jou, J.-J. Huang, J.-C.Wu, and K.-D.Wu, "Novel isolated multilevel DC_DC power converter," IEEE Trans. Power Electron., vol. 31, no. 4, pp. 2690-2694, Apr. 2016.

[13] G. Catona, E. Bianconi, R. Maceratini, G. Coppola, L. Fumagalli, G. Petrone, and G. Spagnuolo, "An isolated semi resonant DC/DC converter for high power applications," IEEE Trans. Ind. Appl., vol. 53, no. 3, pp. 2200-2209, May 2017.

[14] V. R. K. Kanamarlapudi, B.Wang, N. K. Kandasamy, and P. L. So, "A new ZVS full-bridge DC_DC converter for battery charging with reduced losses over full-load range," IEEE Trans. Ind. Appl., vol. 54, no. 1, pp. 571-579, Feb. 2018.

[15] S. Dwari and L. Parsa, "An efficient high-step-up interleaved DC_DC converter with a common active clamp," IEEE Trans. Power Electron., vol. 26, no. 1, pp. 66-78, Jan. 2011.

[16] G. Tibola, E. Lemmen, J. L. Duarte, and I. Barbi, "Passive regenerative and dissipative snubber cells for isolated SEPIC converters: Analysis, design, and comparison," IEEE Trans. Power Electron., vol. 32, no. 12, pp. 9210-9222, Dec. 2017.

[17] F. L. Tofoli, D. D. C. Pereira, W. J. de Paula, and D. D. S. O. Júnior, "Survey on non-isolated high- voltage step-up DC_DC topologies based on the boost

converter," IET Power Electron., vol. 8, no. 10, pp. 2044-2057, Oct. 2015.

[18] F. Mohammadzadeh Shahir, E. Babaei, and M. Farsadi, "Analysis and design of voltage-lift technique-based non-isolated boost DC-DC converter," IET Power Electron., vol. 11, no. 6, pp. 1083-1091, May 2018.

[19] Y. Tang, D. Fu, T.Wang, and Z. Xu, ``Hybrid switched-inductor converters for high step-up conversion," IEEE Trans. Ind. Electron., vol. 62, no. 3, pp. 1480-1490, Mar. 2015.

[20] N. Genc and I. Iskender, "DSP-based current sharing of average current controlled two-cell interleaved boost power factor correction converter," IET Power Electron., vol. 4, no. 9, pp. 1015-1022, Nov. 2011.

[21] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched capacitor/ switched-inductor structures for getting transformerless hybrid DC_DC PWM converters," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 2, pp. 687-696, Mar. 2008.

[22] N. Zhang, G. Zhang, K. W. See, and B. Zhang, "A Single-Switch Quadratic Buck–Boost Converter With Continuous Input Port Current and Continuous Output Port Current," *IEEE Transactions on Power Electronics*, vol. 33, pp. 4157-4166, 2018.

[23] M. R. Banaei, and H. A. F. Bonab, "A High Efficiency Non-Isolated Buck-Boost Converter Based on ZETA Converter," IEEE Transactions on Industrial Electronics, vol. 67, pp. 1991-1998, 2019.

[24] A. Sarikhani, B. Allahverdinejad, M. Hamzeh, and E. Afjei, "A continuous input and output current quadratic buck-boost converter with positive output voltage for photovoltaic applications," *Solar Energy*, vol. 188, pp. 19-27, 2019.

[25] M. Veerachary and M. R. Khuntia, "Design and Analysis of Two-Switch-Based Enhanced Gain Buck–Boost Converters," *IEEE Transactions on Industrial Electronics*, vol. 69, pp. 3577-3587, April 2022.

[26] M. Okati, M. Eslami, M. J. Shahbazzadeh, and H. Shareef, "A New Transformerless Quadratic Buck–Boost Converter with High Voltage Gain Ratio and Continuous Input/output Current Port," *IET Power Electronics*, vol. 15, pp.1280-1294, 2022.

[27] J. Li and J. Liu, "A Novel Buck–Boost Converter with Low Electric Stress on Components," *IEEE Transactions on Industrial Electronics*, vol. 66, pp. 2703-2713, 2019.

[28] J. Divya Navamani, A. Lavanya, D. Almakhles, and M. Jagabar Sathik, "A review on segregation of various high gain converter configurations for distributed energy sources, "Alexandria Engineering Journal, vol. 61, no. 1, pp. 675-700, Jan, 2022.

[29] M. Okati, M. Eslami, M. J. Shahbazzadeh, "A new transformerless DC/DC converter with dual operating modes and continuous input current port,". IET Generation, Transmission & Distribution. 2023.

[30] H. Gholizadeh, S. A. Gorji and D. Sera, "A Quadratic Buck-Boost Converter

with Continuous Input and Output Currents," in IEEE Access, vol. 11, pp. 22376-22393, 2023.

[31] N. Subhani, Z. May, M. K. Alam, I. Khan, M. A. Hossain and S. Mamun, "An Improved Non-Isolated Quadratic DC-DC Boost Converter With Ultra High Gain Ability," in IEEE Access, vol. 11, pp. 11350-11363, 2023.

[32] F. Mumtaz, N. Zaihar Yahaya, S. Tanzim Meraj, B. Singh, R. Kannan, and O. Ibrahim, "Review on non-isolated DC-DC converters and their control techniques for renewable energy applications," Ain Shams Engineering Journal, 2021.

[33] M. Shen, A. Joseph, J. Wang, F. Z. Peng, and D. J. Adams, "Comparison of Traditional Inverters and Z -Source Inverter for Fuel Cell Vehicles," IEEE Transactions on Power Electronics, vol. 22, pp. 1453-1463, 2007.