



## **LDO Optimization with Evolutionary Neural Network**

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### **Abstract**

As grid-connected Photovoltaic (PV) based inverters are being used more, these systems play a more important role in the electricity generation by distributed power generators. Power injection to the grid needs to meet predefined standards. In order to meet the harmonics requirement of standards, they need an output filter. The connection through an LCL filter offers certain advantages, but it also brings the disadvantage of having a resonance frequency. LCL filter can easily help the system to satisfy these requirements but also introduce a resonance peak which makes the system control a challenging task. In this paper, a three-level Neutral Point Clamped (NPC) inverter is connected to the grid through an LCL filter. The injected current of the inverter is controlled using Proportional-Resonant (PR) controllers. The resonant peak of the filter is also damped using capacitor current feedback. A systematic mathematical design procedure for controller and filter capacitor current feedback coefficients is investigated in details. Simulations are carried out in MATLAB/Simulink environment and results depict suitable performance of the system with designed parameters

**Keywords:** LCL Filter, Active Damping, PR Controller, NPC Inverter.

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### **1. INTRODUCTION**

Today's battery-operated portable devices require a fully integrated on-chip power management solution, providing clean and ideally ripple-free supply voltage to the noise-sensitive blocks, such as analogue and RF blocks and fast transient response blocks

for digital circuit's loads in [1-4]. Low Dropout (LDO) regulators are used separately or after the switching regulators to power many circuits block in [5-8]. There are several parameters that need to be considered while optimizing the parameters of capacitor-less regulators such as low quiescent current, low drop output voltage, low output voltage spike and the range of the output capacitor in

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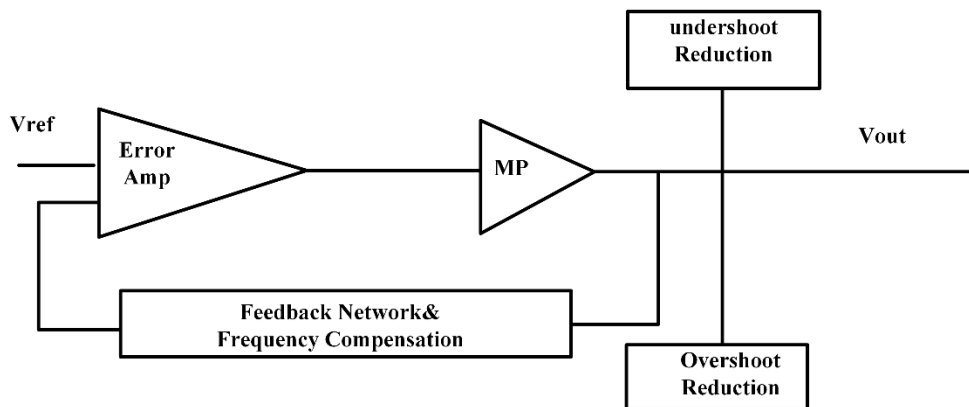
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[9-13]. In voltage-spike detection circuits in [13], extra resistors and capacitors are used that occupy a large chip area and may also depend on the process so much. The other methods employed in [14-16] involve improving the error amplifier to achieve a better slew rate and using a capacitor coupling effect for fast transient response time. These methods consume more current and need additional circuits that raise power consumption. Here in [17], the regulator draws minimum loads of 3 mA to ensure stability for CL of 50 pF. Therefore, it is not assorted for low-load (under 3 mA) current applications. In multi objective optimization problems such as CMOS circuit design using submicron technology, it is very difficult to formulate exact objective function and finding a derivative of it is even difficult. Under such circumstances, the evolutionary algorithm plays an important role. The evolutionary algorithms such as Genetic Algorithm (GA), Particle Swarm Optimization (PSO), Differential Evolution (DE), and Artificial Bee Colony (ABC) used to optimize the analog circuits[6].

In order to reduce power consumption, the rapid path of the capacitor multiplier is set in the error amplifier. Two OVSR circuits are used in the output node to reduce the output voltage undershoot and overshoot, and enhance the LDO settling time. The optimizer utilizes the H-Spice circuit simulator and optimization algorithm to design a circuit with the desired specification. The paper is organized as follows: Section 2 reviews the proposed LDO regulator in detail, Section 3 describes the automatic design of LDO using the ANN algorithm, and LDO regulator simulation results are illustrated in Section 4. Finally, the conclusions are drawn in Section 5.

## 2. PROPOSED LDO STRUCTURE

The block diagram of the proposed LDO is depicted in Fig. 1. The compensation mechanism of the pass transistor in the LDO is carried out by the capacitor multiplier that is implemented in error of the amplifier. The undershoot and overshoot reduction networks clip the spikes of the output voltage.



*Fig. 1. Proposed LDO structure.*

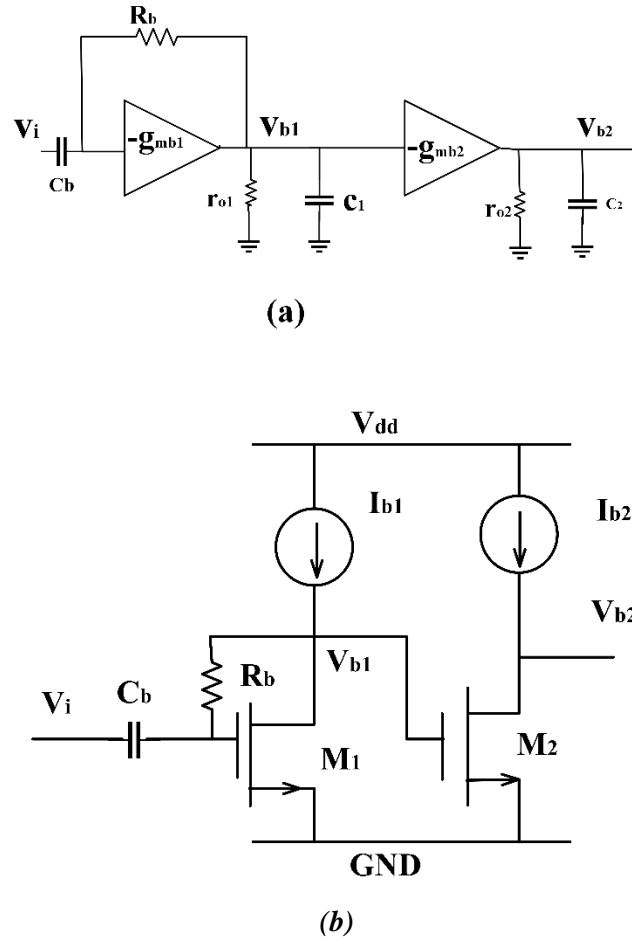


Fig. 2. Capacitor multiplier circuit (a) capacitor-multiplier structure; (b) practical circuit substantiation.

## 2.1. Compensation Network and Rapid Path

When the  $C_b$  capacitor is added, the dominant pole will be placed on Node 2 because of the Miller effect. A rapid path will be created from the output to the input. Obviously, increasing the  $C_b$  value creates an effective capacitor between the output node and the gate of  $M_p$  transistor; furthermore, increasing the  $C_b$  value provides a greater chip area. In order to save the chip area, a capacitor multiplier is used for increasing  $C_b$ .

The structure of the capacitor-multiplier circuits is illustrated in Fig. 2. The output signal is sensed by  $C_b$  and converted into the voltage by shunt–shunt feedback of  $R_b$  and returned back to current via the voltage-controlled current source  $g_{mb2}$ . The amplified capacitance is equal to  $g_{mb1}R_bC_b$ . The capacitive multiplying effect can be used for the rapid path and the pole-splitting network implementation in LDO circuits as it can be pushed into a non-dominant output pole far beyond the UGF (the outcome from the gate of the pass transistor for a large aspect ratio). To investigate the frequency

response of the capacitor-multiplier circuit, the transfer function from  $V_b$  to  $V_{b1}$  is assumed according to Eq. (1), where  $C_1$  is the stacked capacitor in the drain node  $M_{b1}$  in [18].

$$\frac{V_{b1}}{V_i} = \frac{-s(g_{mb1}R_b - 1)C_b}{g_{mb1} \left( 1 + s \frac{C_b}{g_{mb1}} + s^2 \frac{C_b R_b C_1}{g_{mb1}} \right)} \quad (1)$$

Since the LDO regulator circuits usually have a closed-loop bandwidth of less than 1 MHz, these poles can be easily pushed beyond several times the unit gain frequency thus we can simplify Eq. (1) as follows in [18, 19]:

$$\frac{V_{b1}}{V_i} = \frac{-s(g_{mb1}R_b - 1)C_b}{g_{mb1}} \quad (2)$$

The capacitor multiplier circuit can be set in the individual stage out of the main path of the feedback loop between the output and the error amplifier output node.

However, this placement can cause excessive power consumption without sufficient efficiency in the main feedback loop. If this capacitor multiplier circuit could be embedded in the error amplifier, excessive power consumption could be prevented. Therefore, in this study, a capacitor multiplier is placed in the error amplifier that improves the UGF and consumes the least current.

## 2.2. Voltage Spike Reduction Network

When the load current is suddenly decreased to  $I_{min}$ , an overshoot appears in the output voltage during the steady state; the proposed transistor  $M_{10}$  in Fig. 3 has a bias in the cutoff region when the output

voltage starts to increase [according to Eq. (4)]. The  $M_{10}$  transistor will enter into the ohmic region first and then move to the saturation region. It transfers the current from the output node to the ground; thus, it prevents overshoot as the output voltage increases.

Similar to the  $M_{10}$ , the  $M_{11}$  in Fig. 4, has a bias in the cut-off region during the steady state. In this case, when the load current jumps to  $I_{max}$ , an under-shoot will take place in the output voltage. According to Eq. (3), in the PMOS transistor, by decreasing the body voltage, the absolute value of the threshold voltage will be reduced. Therefore, the  $M_{11}$  transistor enters into the ohmic region in the beginning and later it falls into the saturation mode and prevents more undershoot in the output voltage by providing more current into the output node. For achieving steady state in the least transition time, the higher slew rate current without depression in the UGF is used.

$$|V_{th}| = \gamma \left( \sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|} \right) + |V_{tho}| \quad (3)$$

$$V_{sG} \geq |V_{th}| \quad (4)$$

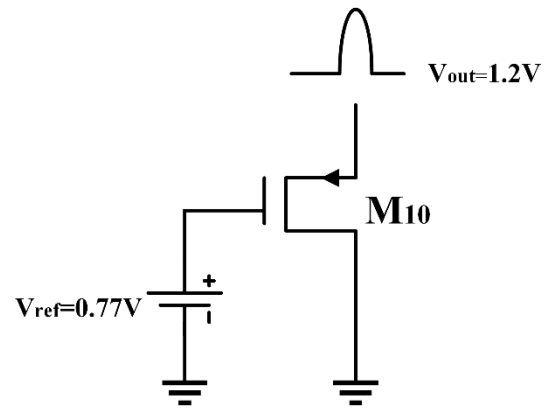
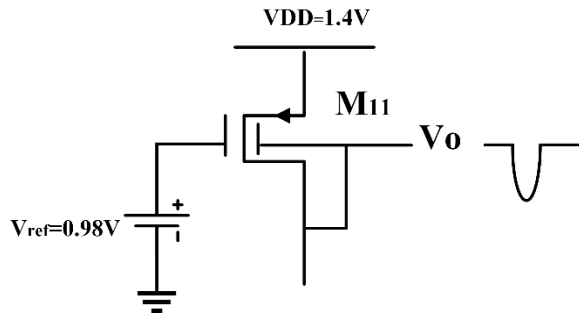


Fig. 3. Schematic of overshoot reduction circuit.



**Fig. 4. Schematic of undershoot reduction circuit.**

where  $V_{th}$  is the threshold voltage value of the transistor for  $V_{SB} \neq 0$ , and  $V_{th0}$  is the nominal threshold voltage for  $V_{SB} = 0$ ,  $\gamma$  is the body bias coefficient and  $2|\phi_F|$  is the surface potential, For PMOS transistor,  $\gamma$  is negative.

The schematic of the proposed LDO is shown in Fig. 5. The capacitor multiplier, which is used in the error amplifier, consists of  $R_b$ ,  $C_b$ ,  $M_6$  and  $M_8$  with a multiplying capability, and  $M_5$  and  $M_7$  as current sources. It is notable that the  $M_5$  and the  $M_7$  current sources are the same as the  $I_{b1}$  current source shown in Fig. 2.

### 3. AUTOMATIC DESIGN OF LDO

The optimizer utilizes the circuit simulator and optimization algorithm to design a circuit with the desired specification. The optimizer provides proper coordination between the circuit simulator and optimization algorithm by generating circuit net-list according to parameters generated by optimization algorithm, initiating circuit simulation, analyzing simulator output and provides a necessary data to optimization algorithm to generate new set parameters.

The various circuit parameters with their upper and lower bounds are estimated. Generally, for most of CMOS circuit design, the circuit parameters are the width and length of various MOS transistors. With this information, a circuit net-list is generated and it is simulated against pre-determined test cases. The simulation results are analyzed and error is calculated.

Based on the calculated error, the new circuit parameter set is generated by an optimization algorithm. The aim of the optimizer is to reduce errors.

### 3.1. Artificial Neural Network

Neural networks, also known as the artificial neural network (ANN's), are the information processing system with their design inspired by the studies of the ability of the human brain to learn from observations and to generalize by abstraction. [20] The fact that neural network can be trained to learn any arbitrary nonlinear input/output relationships from corresponding data and the acquired knowledge has resulted in their use in a number of areas such as pattern recognition, speech processing, [20, 21] control, bio medical engineering, RF and microwave etc. Recently, (ANNs) have been applied to CMOS analog circuit design and optimization problems as well. Neural networks are first trained to model the electrical behavior of passive and active components/ circuits[20-24]. These trained neural networks, often referred to as neural network models, can then be used in high level simulation and design, providing first and accurate answers to the task that they have learnt by acquiring the knowledge from their training. Neural networks are effective

and efficient alternatives to conventional methods such as numerical modeling methods, which could be highly computationally expensive, or analytical methods which could be difficult to obtain for newly achieved devices or empirical modeling solutions due to huge range and limited accuracy. [23] Neural network techniques have been used for a very wide variety of applications and modeling methods. [24] An analog system is typically characterized by a set of performance parameters used to succinctly quantify the properties of the circuit given fixed topology; circuit synthesis is the process of determining numerical values for all components in the circuit such that the circuit conforms to a set of performance constraints. Due to the high degree of nonlinearity and interdependence among design variables, the manual design of an analog circuit is often reduced to a process of trial and error in which the solution space is searched in an ad hoc manner for a circuit satisfying all constraints. [22] The numerical circuit simulator SPICE is often used as a benchmark of comparison to determine the relative accuracy of alternative schemes for evaluating the performance of analog circuits. However, the computational requirements of running SPICE limit its use when attempting to evaluate a circuit's performance parameters during circuit synthesis. Stochastic combinatorial optimization methods require the computation of performance parameters for a large number of circuit sizing alternatives [23]. It is therefore beneficial to reduce the time associated with generating performance estimates. Neural network models are used to provide robust and

accurate estimates of performance parameters for several CMOS analog circuits [25, 26]. A neural network of sufficient size can estimate functional mappings to an arbitrary precision given a finite discrete set of training data. Hyperdimensional non-linear functions are readily modeled using neural networks. Neural networks can also easily incorporate knowledge of system behavior. Course functional models can be embedded in the network structure reducing the functional complexity that must be mapped by the network. These often result in the smaller network size and reduction in training effort. [27] Once trained with a particular functional mapping, the evaluation time of a neural model is very fast. However, training algorithms can help reduce the interaction needed to determine an appropriate network size. The evaluation time for the neural models is much less than that required by a full SPICE simulation, the models can be incorporated into a circuit synthesis algorithm used to optimize a fitness function based on performance parameter constraints. Neural networks have recently gained attention as a fast, accurate and flexible tool for modeling, simulation and design. Each time a new network is trained, or an old network is retrained, the shape of the function described by the neural model changes, complicating the issue of where to place additional sample points. [28] The neural network models provide a great deal of time savings in situations where a fixed topology must be reused and re-synthesized many times which is the primary target for modeling and synthesis of analog circuits using neural network models [29].

ANN is composed of a large number of highly interconnected processing elements (neurons) working in parallel to solve a specific problem. Each connection has a weight factor and these weights are adjusted in a training process.

Consider monolithic Multilayer Perceptron (MLP) training by BP algorithm. The goal is minimizing the sum squared error (SSE).

$$J(w) = \frac{1}{2} \sum_{s=1}^P \sum_{i=1}^{N_M} (d_{s,i} - y_{s,i}^M)^2 \quad (5)$$

where  $d_{s,i}$  is the  $i$ th target and,  $y_{s,i}^M$  is the actual outputs corresponding to the  $s$ th training pattern,  $W$  is a vector constituted by all the weights and biases involved in the network, and  $N_M$  is the number of output units. In this scheme, an initial weight vector  $W_0$  is iteratively adapted according to the following recursion to find an optimal weight vector. The positive constant of  $\eta$  is the learning rate.

$$W_{k+1} = W_k - \eta \frac{\partial J(W)}{\partial W} \quad (6)$$

PSRR, transient time, ripple output voltage and line regulation are 4 input neurons and outputs  $W_{out}$ ,  $C_b$ ,  $C_{out}$ ,  $I_B$  will be optimized by the neural network.

The NN toolbox of MATLAB software is used to design the neural network architecture for determining the size of the circuit's element. Number of hidden layers,

number of neurons in the hidden layer, and the results are shown in Table 1.

#### 4. SIMULATION RESULTS

The proposed LDO has been designed and simulated by the 0.18  $\mu\text{m}$  CMOS process. The LDO is designed to source output current between 0mA and 50mA and consumes a small quiescent current of 26  $\mu\text{A}$  under a no-load condition, Fig. 5 shows the measured load transient response; the output current varies from 0 to 50mA at 1.4V supply voltage, while the rise time and the fall time of the load current are 28  $\mu\text{s}/\text{mA}$  and 56  $\mu\text{s}/\text{mA}$  respectively. The measurement shows that the load transient voltage spike is only 20 mV. Figure 6 shows the measured line transient response; the supply voltage switches between 1.4V and 2V, with 50mA output current, while the voltage spike is 6mV.

The Power Supply Ripple Rejection (PSRR) of the LDO with  $C_{out}=1\text{PF}$  at  $I_O = 50, 0\text{mA}$  is shown in Fig. 7. As observable, the measured PSRR is smaller than  $-45$  dB under 100 KZ frequency.

Table 2 provides a performance comparison between the proposed LDO and the previously published design. The use of capacitor-multiplier and the overshoot and undershoot reduction circuits can be effective in decreasing the output voltage variations and the settling time. But the value of quiescent current (IQ) and the amplitude of

**Table 1. Number of data and results.**

Network topology	Epoch	Number of samples	regression
4-11-8-6-4	2000	3456	0.996
4-13-15-4	2000	3456	0.997

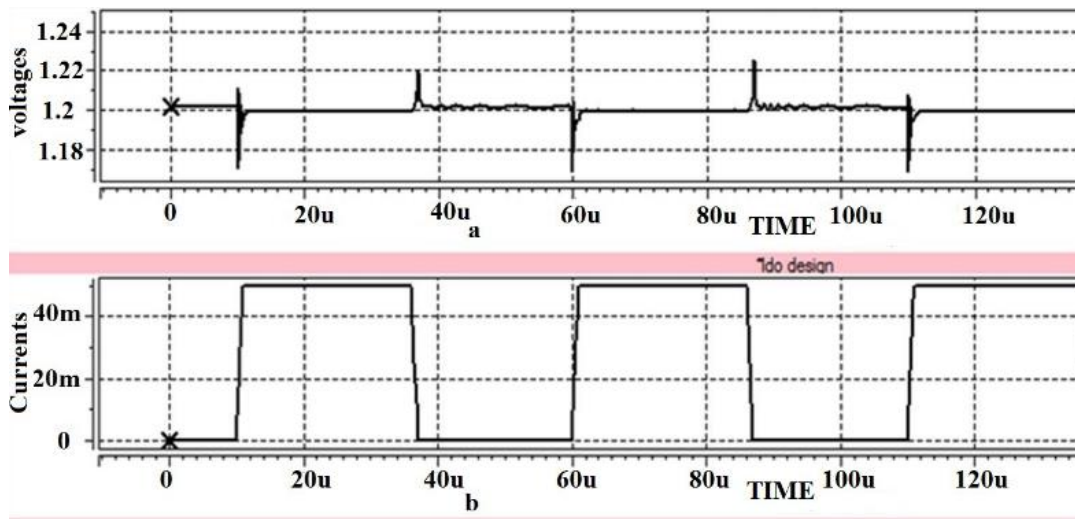


Fig. 5. Transient measurement result (a) load transient response of the proposed LDO and (b) output current variation.

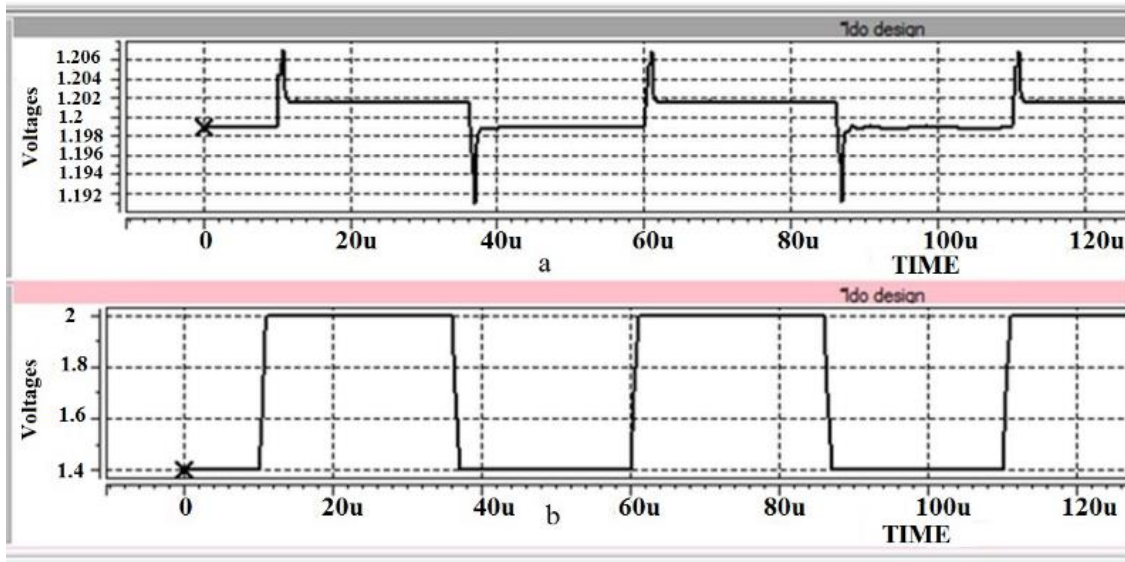


Fig. 6. Transient measurement result of the proposed LDO (a) line transient response and (b) input voltage variation.

maximum output current should also be considered to carry out a justifying comparison. Therefore, the Figure Of Merit (FOM) given in[15] can be an appropriate standard for comparison.

$$FOM = T_R \frac{I_q}{I_{out\ max}} = \frac{C_{out} \Delta V_{out}}{I_{out\ max}} \frac{I_q}{I_{out\ max}} \quad (7)$$

$I_{out\ max}$  is the maximum load current that can be sustained by LDO while  $I_q$  is the quiescent current.



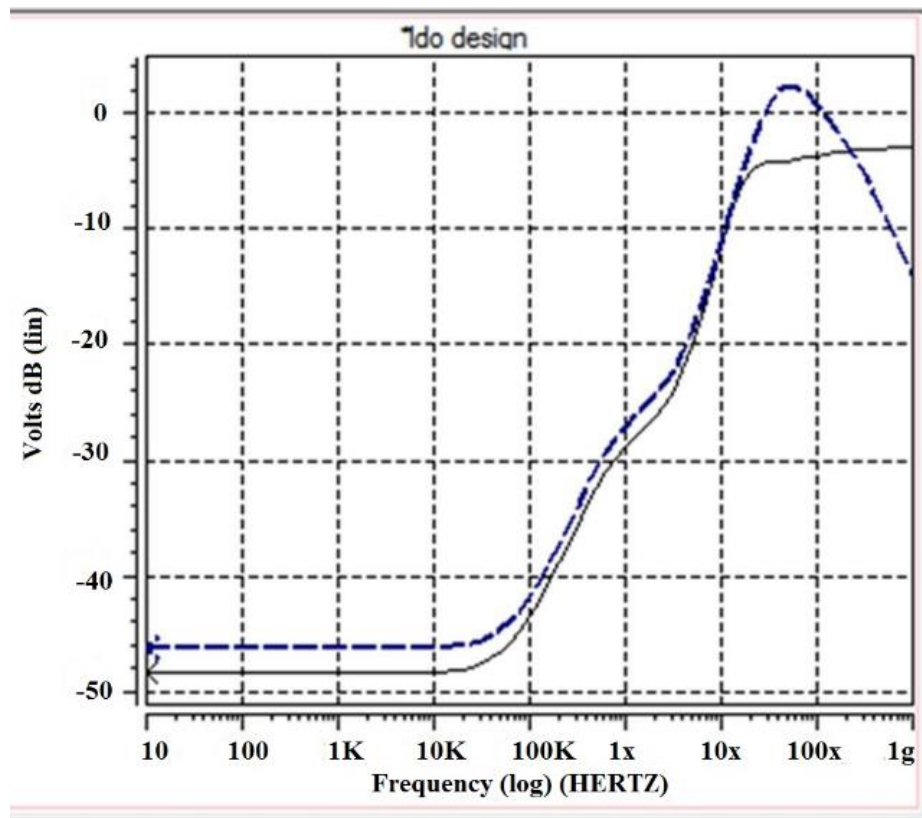


Fig. 7. Measured PSSRR of proposed LDO.

Table 2. Performance summary and comparison with previously reported LDOs.

parameter	[20] Sim.	[21] sim.	[23] Sim.	[24] Sim.	[25] Exp.	[30] Exp.	This work
Year	2010	2008	2015	2015	2016	2019	2020
Tech[ $\mu\text{m}$ ]	0.35	0.35	0.35	0.35	0.18	0.5	0.18
Vin [V]	1.2	1.2	1.4	1.2	1.4	1.5	1.4
V out [V]	1.6	1	1.2	1	1.2	1.3	1.2
I out [mA]	100	50	100	100	100	600	50
IQ [ $\mu\text{A}$ ]	20	95	130	15	141	16.5	26
C out [pF]	>20	100	100	100	100	5.1	1-100
T settle[ $\mu\text{s}$ ]	$\approx 8$	$\approx 1.4$	$\approx 2$	$\approx 1$	$\approx 1$	$\approx 1$	$\approx 2$
$\Delta\text{Vout}$ [mV]	100	200	125	80	85	514	20
FOM[fs]	20	152	89	75	18	12	20.8

As seen in Table 2, the use of reduction circuits and the capacitor multiplier circuit increase the quiescent current to 26  $\mu\text{A}$  in the proposed LDO, but the maximum output voltage variation under a load capacitor of 1–100 pF is much less than earlier designs. Comparisons of results indicate that capacitor-multipliers and reduction circuits are effective to improve LDO stability and transient response and presents acceptable results.

## 5. CONCLUSION

From the results we can conclude that the application of the ANN algorithm used to solve the problem of the device sizing of the Analog CMOS circuit. Also, observe the robustness of the optimizer for the two-stage op-amp design. A low drop-out voltage regulator without the off-chip capacitor has been presented that achieves low output voltage spikes and fast transient response by compensation network and OVSR circuits. The capacitor multiplier provides a fast path and improves the transient response. The proposed LDO regulator has been designed to create the 1.2V output voltage. The output voltage spike of the LDO with the proposed OVSR circuit decreases to 20 mV. The proposed LDO is stable for output currents between 0mA and 50 mA, and has 200mV dropout voltages. The novelty of this work is: first the very low quiescent current about 26  $\mu\text{A}$ , second the low power consumption through low input voltage and low quiescent current, third the output capacitor range is between 1 pF and 100 pF, which is wide enough compared to those capacitors used in the other mentioned works. To perform a

justifiable comparison, a number of previously reported LDOs have been simulated by HSPICE and using the reported values in the references. The results of simulation and comparison based on the FOM indicate the improvement of proposed LDO specification.

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